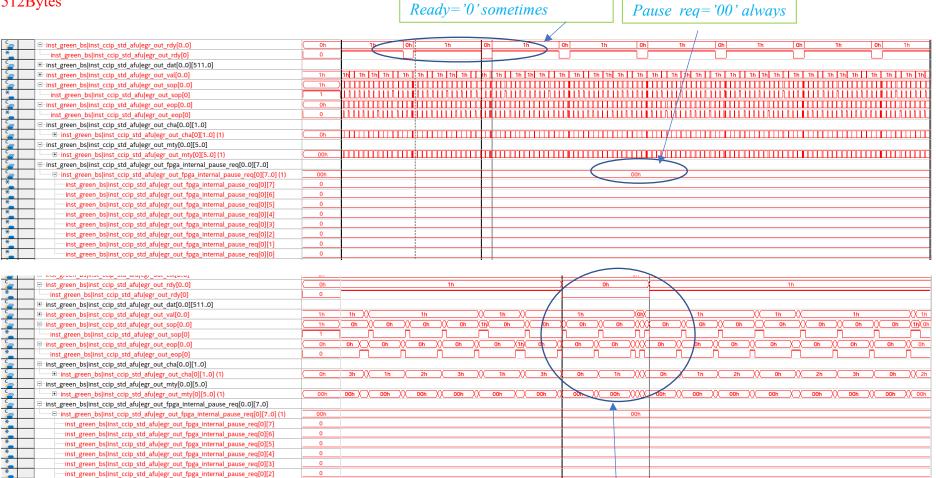
Traffic 100%@25GbE : Result = Packet loss occurs

64Bytes	I	Ready='0' sometimes							Paus	reg	/= '00' a	alway.	5				
Grinst green bslinst ccip std afu egr out rdy[00]	16	16 16	16	-	h 1h	16 T	16	1h 1	h 1h	1h	1h 1h 1	<u>ь </u>	h 1	h 1h 1h	16	16 16	1h 1h 1h
inst_green_bs/inst_ccip_std_afu/egr_out_rdy[0]	<u> </u>	_														<u> </u>	
Image: Spinst_ccip_std_adulegr_out_dat[0.0][511.0]						- 1	,	U			1 1 1			1 1 1			
Image: Selection Signed Color State and Selection			00000	000000000000000000000000000000000000000	000555500	01020	30405060708090A0B0	CODOE	001112131/	15161718101	A181C1D1E1E202	10003040506	27292024283		E36		
inst_green_bs/inst_ccip_std_afu/egr_out_val(0)	ת היו היו היו היו היו			ורדי רדי הרחרי החורי													
Section Secti			1001						10 011 111 001								
* inst group beliest sein std afulage out sep[0]			-														
Inst_green_bs inst_ccip_std_afu egr_out_sop[0.0] I			_						16								
inst_green_bs/inst_ccip_std_afu/egr_out_eop(0.0)			-							_							
See P inst_green_bs inst_ccip_std_afu egr_out_cha[00][10]																	
Imat_green_bs inst_ccip_std_afu egr_out_mty[0.0][5.0]										/							
inst_green_bs/inst_ccip_std_ard/egr_out_mty[0.5(0](1)			-						04h								
General spinst_ccip_std_afdjegr_out_ftyga_internal_pause_req[00][70]									040	-							
Image: Selection of the			-						00h								
*inst green belingt een std afvlagt out fage internal pause reg[0][7] 0			-					_	0011	\sim							
inst_green_bs/inst_ccip_std_afu/egr_out_fpga_internal_pause_req[0][6]			-														
inst_green_bsjinst_ccip_std_afulgg_out_fpga_internal_pause_req[0][7] inst_green_bsjinst_ccip_std_afulgg_out_fpga_internal_pause_req[0][6] inst_green_bsjinst_ccip_std_afulgg_out_fpga_internal_pause_req[0][5] inst_green_bsjinst_ccip_std_afulgg_out_fpga_internal_pause_req[0][5]																	
inst_green_bs/inst_ccip_std_afu/egr_out_fpga_internal_pause_req[0][4]																	
inst green bojinst ccip std afulegr out [pga_internal_pause_req[0][4] inst green_bsjinst_ccip std afulegr_out_[pga_internal_pause_req[0][3] inst green_bsjinst_ccip std afulegr_out_[pga_internal_pause_req[0][2] inst green_bsjinst_ccip std afulegr_out_[pga_internal_pause_req[0][1]																	
inst_green_bs/inst_ccip_std_afu/egr_out_fpga_internal_pause_req[0][2]																	
inst_green_bs/inst_ccip_std_ard/egr_out_fpga_internal_pause_req[0][2]																	
inst green bs/inst ccip std afu/egr out fpga internal pause req[0][0]																	
Image: Second state in the second s	XonX			h				1h		KonX				1h			
See Inst_green_bs inst_ccip_std_afu egr_out_dat[0][5110] (1)			00000	000000000000000000000000000000000000000	OFFFFOO	010203	0405060708090A0B0C			5161718191A		22232425262					
Image: Section of the section of t	Oh X	11	h	XohX1hXohX_	h (0h) 1	hioni	1h X0hX	1h	XohX	h (0h(1h(0	<u>μ</u> 1h	X		1h	() (0h) 1h	(0h)(1	<u>Ih () Oh</u>
inst_green_bs inst_ccip_std_afu egr_out_val[0]											J						
□ inst_green_bs inst_ccip_std_afu egr_out_sop[00]						_			1h		_						
inst_green_bs inst_ccip_std_afu egr_out_sop[0]																	
Image: Second									1h								
inst_green_bs inst_ccip_std_afu egr_out_eop[0]						-	/				1						
General system General system General system General s				~~~~										~~~~	~~~~		
inst_green_bs inst_ccip_std_afu egr_out_cha[0][10] (1) 0/(2ħ/(3ħ/(0ħ/(1ħ	h <u>X 2hX 3hX 0hX 1h</u> X	2hX3hX	<u>0hX1hX</u>	h\3h\0h\1h\2h\3h	<u>X OHX 111 2</u>	<u>hX 3hX</u>	h\1h\2h\3h\0h\1h\;	<u>2hX 3h</u> X	0hX 1hX 2hX 3h	(<u>0h)(1h) 2h) 3</u> 1	10hX 1hX 2hX 3hX 0)h <u>X 1hX 2hX 3h</u> X	0hX 1hX 2hX 3	h <u>X OhX 1hX 2h</u>	<u>X 3hX 0hX 1hX 2</u>	<u>hX3hX0hX1hX2h</u> X	(3h)(0h)(1h)
G = inst_green_bs inst_ccip_std_afu egr_out_mty[00][50]						\checkmark											
See Inst_green_bs inst_ccip_std_afu egr_out_mty[0][50] (1)									04h								
☐ Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[00][70]																	
- inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][70] (1)									00h								
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][7]									/								
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][6]								-									
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][5]								/									
Image: Second							/										
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][3]																	
inst_green_bs/inst_ccip_std_ard/egr_out_ipga_internat_pause_red[0][2]																	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][1]																	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][0]																	

When ready = '0', there still exists some valid packet (val = '1', sop='1', eop='1')

512Bytes



When ready = '0', there still exists some valid packet

0

0

minst_green_bs|inst_ccip_std_afu|egr_out_fpga_internal_pause_req[0][1] inst_green_bs|inst_ccip_std_afu|egr_out_fpga_internal_pause_req[0][0]

Traffic 99.9%@25GbE : Result = No packet 1	oss $Pause \ req = '1' \ always$ $Pause \ req = '00' \ always$
64Bytes	
☐ inst green bs inst ccip std afu egr out rdy[00]	16
inst_green_bs inst_ccip_std_afu egr_out_rdy[0]	
E = inst_green_bs inst_ccip_std_afu egr_out_dat[0.0][511.0]	
Image: Sinst_crip_std_ardjegr_out_dat(0.0)[S11.0] Image: Sinst_green_bs/inst_crip_std_ardjegr_out_val[0.0]	1h X0hX 1h X 0h X 1h X0hX 1h X0hX 1h X 0h X 1h X0hX 1h X 0h X 1h X0hX 1h X 0h X 1h
See Inst green bs inst ccip std afu egr out sop[00]	
Image: the second se	
	m harden ha
⊞ inst_green_bs inst_ccip_std_afu egr_out_cha[00][10]	
⊞ inst_green_bs inst_ccip_std_afu egr_out_mty[00][50]	
General procession of the set of	00h
□ inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][70] (1)	000
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][7]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][6]	
inst_green_bs[inst_ccip_std_afu]egr_out_fpga_internal_pause_req[0][5]	
- Contraction Contraction 1.8. Contraction Character Action	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][3]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][2]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][1]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][0]	
Image: State of the state o	1h
☐ □ inst_green_bs inst_ccip_std_afu egr_out_dat[0.0][511.0]	
Inst_green_bs inst_ccip_std_afu egr_out_dat[0][5110] (1)	00000000000000000000000000000000000000
argenter and the second secon	<u>(1h) (0h)(1h)(0h)(1h)(0h)(1h)(0h)(1h)(0h)(1h)(0h)(1h)(0h)(1h)(0h)(1h)</u>
inst_green_bs inst_ccip_std_afu egr_out_val[0]	
afulegr_out_sop[00] □= inst_green_bs inst_ccip_std_afu egr_out_sop[00]	1h
inst_green_bs inst_ccip_std_afu egr_out_sop[0]	
☐ inst_green_bs inst_ccip_std_afu egr_out_eop[00]	1h
inst_green_bs inst_ccip_std_afu egr_out_eop[0]	
☐ □-inst_green_bs inst_ccip_std_afu egr_out_cha[00][10]	
🖕 🔲 inst_green_bs inst_ccip_std_afu egr_out_cha[0][10] (1)	(2)(3)(3)(3)(3)(3)(3)(3)(3)(3)(3)(3)(3)(3)
☐ Inst_green_bs inst_ccip_std_afu egr_out_mty[00][50]	
Inst_green_bs inst_ccip_std_afu egr_out_mty[0][50] (1)	04h
☐ inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[00][70]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][70] (1)	00h
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][7]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][6]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][5]	
Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][70] (1) Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][7] Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][6] Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][5] Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][6] Inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][7] Inst_green_bs inst_cip_std_afu egr_out_fpga_internal_pause_req[0][7] Inst_green_bs inst_cip_std_afu egr_out_fpga_internal_pause_req[0][7] Inst_green_bs inst_cip_std_afu egr_out_fpga_internal_pause_req[0][7] Inst_green_bs inst_cip_std_afu egr_out_	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][3]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][2]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][1]	
inst_green_bs inst_ccip_std_afu egr_out_fpga_internal_pause_req[0][0]	
512Bytes	
Set and the set of	
E inst green_bs inst_ccip_std_afu egr_out_dat[00][5110]	

