Performance Test(Wire Speed) with Factory Image

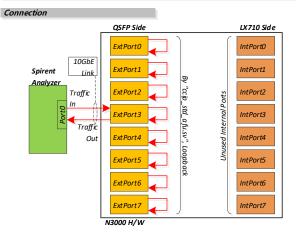
Environment: Modified "ccip_std_afu.sv"

```
assign egr_out_sop[0] = ing_in_sop[0];
assign egr_out_eop[0] = ing_in_eop[0];
assign egr_out_val[0] = ing_in_val[0];
assign egr_out_mty[0] = ing_in_mty[0];
assign egr_out_dat[0] = ing_in_dat[0];
assign egr_out_err[0] = ing_in_err[0];
assign egr_out_cha[0] = ing_in_err[0];
assign ing_in_rdy[0] = egr_out_rdy[0];

assign ing_out_sop[0] = 1'b0;
assign ing_out_eop[0] = 1'b0;
assign ing_out_wal[0] = 1'b0;
assign ing_out_mty[0] = 6'b0;
assign ing_out_dat[0] = 512'b0;
assign ing_out_err[0] = 1'b0;
assign ing_out_err[0] = 1'b0;
assign ing_out_cha[0] = 3'b0;
assign egr_in_rdy[0] = 1'b1;
assign egr_in_fpga_internal_pause_req[0] = 8'b0;
assign egr_in_fpga_internal_pause_req[0] = 8'b0;
assign egr_in_fpga_internal_pause_req[0] = 8'b0;
```

※ Unused Pause function by all req signal is low

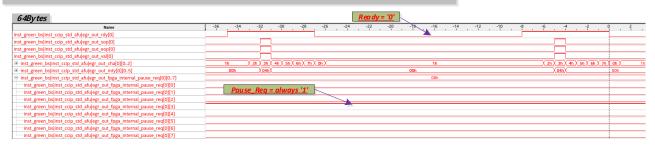
Environment: Performance Test

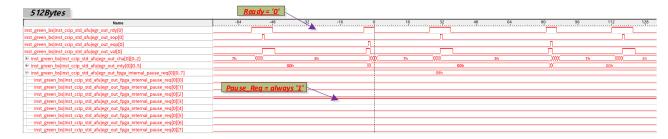


Spirent Analyzer Setup

ration (99.99						64B ytes, 99.99% Port Load		Port Load	
m	st size: 1 Duration mode: Continuous of frame gap: 12 or frame gap unt bytes Advanced Port load			Load mode © Fix © Random		Load mode © Rix			
Scheduling mode graphical e				g mode gr	aphical examp			Fixed load settings Percent (%): 99.99	
	Index	Controlled By	Traffic Pattern	Туре	Tx Port	Frame/sec (fps) :	14879464,2857142	@ Frame/sec (fos):	14880952 3809523
	0	generator	Pair	Port	Port //1/1	⊕ bos :	9999000000	no bos:	10000000000
						€ Kbøs:	9999000	⊕ Ktes :	10000000
						Mbps:	9999	Mtes:	10000
						nter burst gap (bytes) :	12,0084008400840	(inter burst gap (bytes):	12
						L2 Rate (bos) :	7618285714.28571	L2 Rate (bos) :	7619047619.04761

Traffic 100%@10GbE to ExtPort3 : Result = Packet loss occurs





Traffic 99.99%@10GbE to ExtPort3: Result = No packet loss



