



Interfacing Intel® 8255x Fast Ethernet Controllers without Magnetics

Application Note (AP-438)



Revision History

Revision	Revision Date	Description
1.1	Nov 2005	Initial Release
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1.0 Introduction

The goal of this document is to enable the construction of an interface for the 8255x without the use of the 1:1 transformer previously required. This reduces cost and size by eliminating the transformer and replacing it with low cost passive components such as resistors and capacitors.

This document, and its associated circuitry, was conceived and developed in response to many requests by our OEM customers involved in embedded designs to reduce component expense and “real estate” use on their boards. These new designs eliminate the need for the relatively large and expensive magnetics module commonly used between PHYs and the RJ45 connectors as well as in backplane and other such direct connect applications. We have developed a simple solution that can be used in a wide variety of such applications with the intent of simplifying the design cycle and reducing development time enabling products to enter the market in a shorter time frame than otherwise might be possible.

Since different LAN devices use different DC-biasing and different current source circuits, there is no single, magnetic-less circuit that will allow the LAN to work properly with every different, possible pair of LAN components. Magnetic-less LAN designs with good networking performance and extremely good Bit Error Rates (BERs), will not necessarily be fully IEEE compliant. Typically, they should comply with many, but not necessarily all, of the IEEE specifications.

Note: Magnetic-less LAN designs should not be done when the LAN signals must be routed through cables that are external to the system chassis. The isolation transformer in a magnetics module, provides some level of improved safety in the event that higher voltages or ESD gets onto the LAN cable. Magnetic-less LAN designs should only be done when the differential circuits or cables will be routed internal to the same chassis.

2.0 Circuit Design

Although the primary development and testing was done using the Intel® 82559 Fast Ethernet Controller with integrated MAC and PHY, the circuit and basic guidelines can be used with the 82550xx and the new 82551QM and 82551ER devices which are based on the 82550, which in turn was based on the 82559. All testing was performed on modified Intel network interface cards (NICs) using the 82559 controller. Thus, all of these devices can benefit from this document and can most likely be used in place of the 82559 with little or no alterations of the circuit shown below.

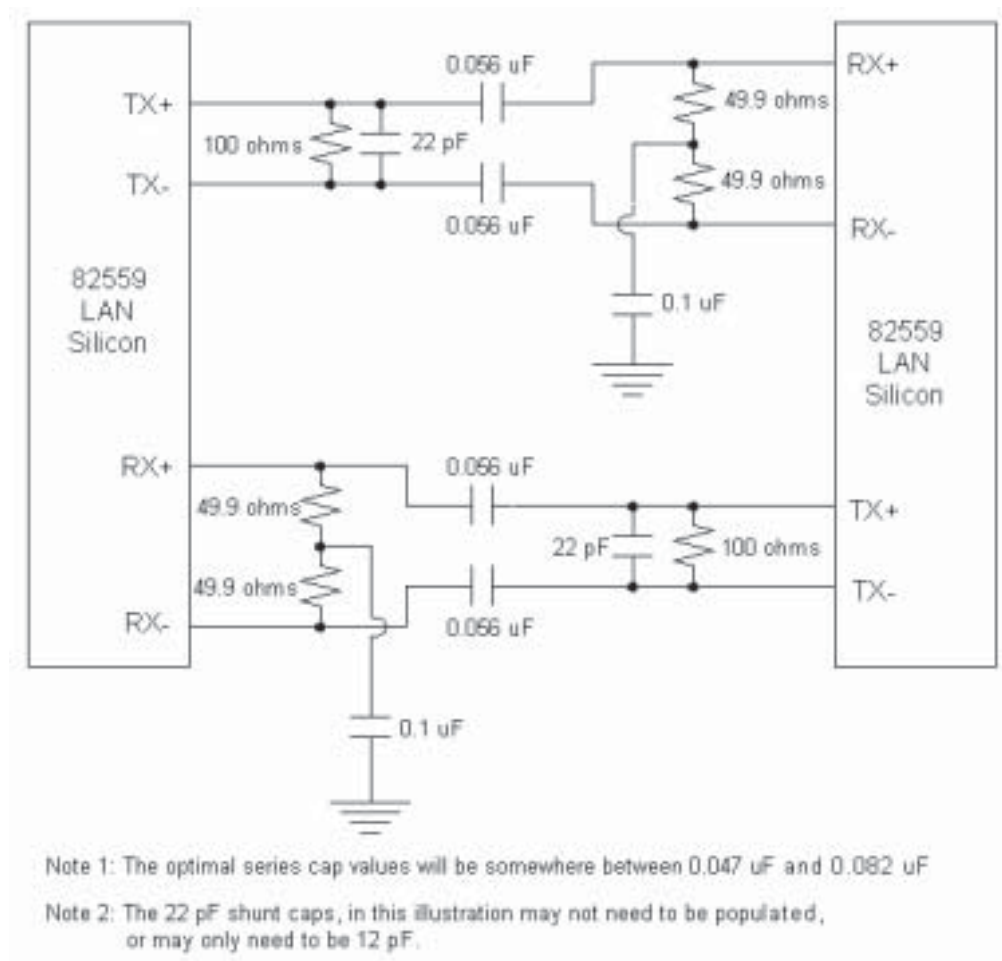


Figure 1. Basic Magnetic-Less 82559 Interface

2.1 Design and Layout Considerations

To optimize signal integrity:

- Maintain a 100 Ω differential impedance by choosing the appropriate connector and PCB layout. If possible, impedance match the connectors used in the backplane.
- Place components shown in the termination networks as close as possible to the transceiver pins.
- Allow sufficient spacing between adjacent differential pairs to minimize crosstalk. Typically, there should be about 50 mils of separation between adjacent differential pairs.
- Place differential circuits' termination components within two inches of the LAN silicon's transceiver pins.
- Keep backplane traces reasonably short.

Signal traces must:

- Use symmetric routing within each differential pair.
- Be 100 Ω differential (+/- 10-ohms).
- Equal 1 ounce (1.4 mils) or greater thickness.
- Equal greater than 5 mils (0.005 inches) thick for dielectric layers.
- Keep differential trace pairs greater than 50 mils from other pairs and more than 50 mils from digital traces to avoid crosstalk.

Additionally, the designer should:

- Minimize the number of vias.
 - Keep the trace lengths equal, within each differential pair. (The maximum delta within a differential pair should be less than or equal to 50 mils or 0.050 inches.)
 - Place the transmitter termination circuit between the series capacitors and LAN silicon to improve testability.
 - Place the series capacitors no more than two inches from the LAN silicon's transmit pins to improve testability.
 - Use reasonably tight capacitance tolerance for series capacitors, They should not exhibit large capacitance changes due to "aging":
 - NPO capacitors with "J" tolerance (+/- 5%) are a good choice because NPO capacitance does not change much with temperature and "aging." It may be harder to obtain NPO capacitor values at or above 0.056 μ F.
 - X7R capacitors with "K" tolerance (+/-10%) are also a reasonably good choice. X7R capacitance is reasonably stable with temperature and aging. X7R capacitors should be easy to obtain in capacitance values around 0.056 μ F.

2.2 Design Testing

The point-to-point interface has been tested but multi-drop and multi-point have not.

- 100BASE-TX or 10BASE-T applications are supported.
- Full-duplex and half-duplex data transmissions are supported.
- Auto-negotiation is not supported.
- Auto-MDIX is not supported. The 82559 and the 82559ER offer Auto-MDIX. However, this feature is not supported in magnetic-less applications. The Auto-MDIX feature allows automatic selection of driver and receiver pairs independent of the cable (straight-through or cross-over) used in normal LAN applications. Auto-MDIX also requires that the magnetics for both transmit and receive functions be identical to allow either pair to be a transmitter or a receiver.

Due to design variables and time limitations of a PCB-backplane evaluation board, testing was completed on modified NICs (adapters). The magnetic interface was replaced with the appropriate AC termination network, and the RJ-45 connector and Category 5 cable were used to emulate the backplane.

During validation testing, the following variables were considered:

- Variable packet length (256-byte to 1514-byte)
- Variable cable length (0 to > 2 meters)
- VCC supplies, full range of operation

The following bullet items list suggested tests that should be performed for 100BASE-TX and 10BASE-T. The expected test results are also listed.

- 100BASE-TX
 - Differential Output Amplitude: +/- 800 mV_{peak} to +/- 1100 mV_{peak}
 - Amplitude Symmetry: The ratio should be between 0.095 and 1.05
 - Rise and Fall Times: 3 ns to 5 ns, with maximum delta \leq 1.3 ns
 - Transmitter Duty Cycle Distortion (TDCD): 15.4 ns to 16.6 ns
 - Transmitter Jitter: Jitter \leq 1.6 ns
 - Transmitter Return Loss: \geq 10 dB at 30 MHz
 - \geq 7.5 dB at 60 MHz
 - \geq 5 dB at 80 MHz
 - Receiver Return Loss: \geq 12 dB at 30 MHz
 - \geq 10 dB at 60 MHz
 - \geq 8 dB at 80 MHz
- Transmit and Receive Bit Error Rate (BER) Tests: BER \leq 10⁻¹⁰
 - Additional test: Transmit Jitter measured at the receiver (within two inches) should be less than or equal to (\leq) 5 ns.

- 10BASE-T
 - Differential Output Amplitude: +/- 1.8 V_{peak} to +/- 2.7 V_{peak}
 - Transmitter Jitter: not yet defined.
 - Transmit and Receive Bit Error Rate (BER) Tests: BER ≤ 10⁻¹⁰

2.3 Design Recommendations

It is highly recommended that a minimum distance is maintained between the PHY and the actual connectors used on the PCB. Components shown in the termination networks should be placed as close as possible to the transceiver pins, thereby placing the termination networks as close to ports as possible for all circuit configurations.

It is recommended that the system layout for the PCB backplane matches the characteristics, as closely as reasonably possible, of category 5 cable as follows:

- Use a 100 Ω differential impedance across the differential pairs
- Match impedance on the connectors used in the backplane (Please note that depending on the layout, additional termination may be required at the connector)
- Allow sufficient spacing on adjacent differential pairs to minimize crosstalk. (Layout-tool design rules should be sufficient)
- Place termination circuitry close to the device
- Keep backplane traces as short as possible
- Minimize vias

3.0 Summary

Ethernet over a backplane is gaining popularity because it provides the high reliability and data integrity of Ethernet and is achieved at high speed without yet another protocol to implement. Selected Intel Fast Ethernet transceivers provide engineers that develop fast and complex proprietary bus systems with a high-performance alternative particularly suitable for the design of current systems.

Note: The circuit shown is provided as a starting point and has been used as such successfully by a number of designers. However, we do not expect it to be the final circuit in any design but expect that fine tuning, performed through alterations and modifications, will be required to match the needs of that particular design.

4.0 References

The following documents were used to help write this document. They may be obtained by contacting your Intel Sales Representative.

- Tuning the 8255x Controller's Equalizer for Capacitor-Coupled Applications, Application Note (AP-435), Intel Corporation.
- 82559 Fast Ethernet Multifunction PCI/CardBus Controller Datasheet, Intel Corporation.
- 100BASE-TX Physical Layer Conformance Test Kit
- 10/100 Mbps Ethernet Family Software Technical Reference Manual, Intel Corporation.
- 82559 Fast Ethernet Multifunction PCI/CardBus Controller Stepping Information, Intel Corporation.
- 82559ER Fast Ethernet PCI Controller Stepping Information, Intel Corporation.