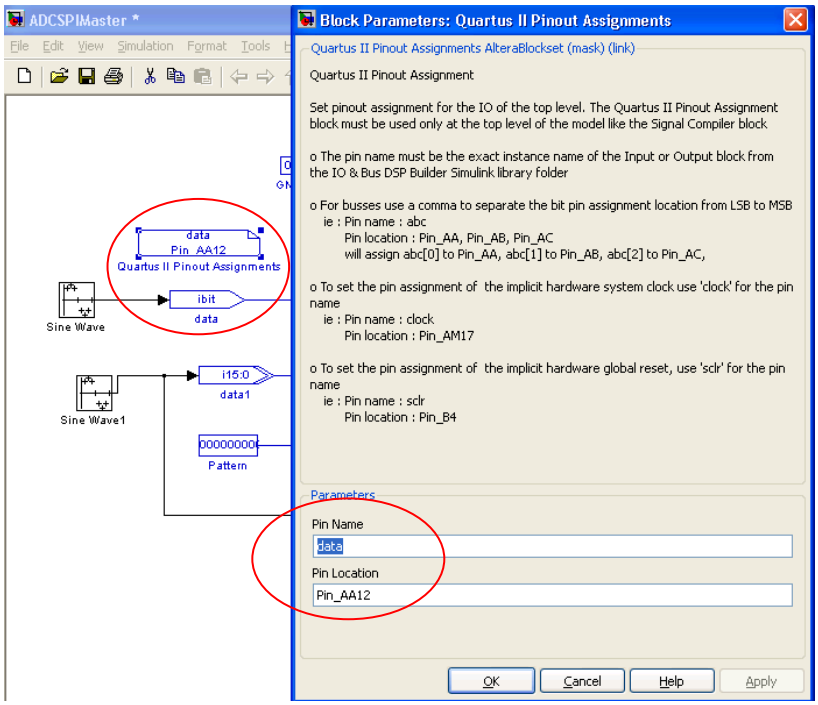
ADCSPIMaster *
File Edit View Simulation Format Tools
data
Pin_AA12
Quartus II Pinout Assignments
ibit
data
Sine Wave
i15:0
data1
Sine Wave1
00000000
Pattern
Block Parameters: Quartus II Pinout Assignments
Quartus II Pinout Assignments AlteraBlockset (mask) (link)
Quartus II Pinout Assignment
Set pinout assignment for the IO of the top level. The Quartus II Pinout Assignment block must be used only at the top level of the model like the Signal Compiler block
o The pin name must be the exact instance name of the Input or Output block from the IO & Bus DSP Builder Simulink library folder
o For busses use a comma to separate the bit pin assignment location from LSB to MSB
ie : Pin name : abc
Pin location : Pin_AA, Pin_AB, Pin_AC
will assign abc[0] to Pin_AA, abc[1] to Pin_AB, abc[2] to Pin_AC,
o To set the pin assignment of the implicit hardware system clock use 'clock' for the pin name
ie : Pin name : clock
Pin location : Pin_AM17
o To set the pin assignment of the implicit hardware global reset, use 'sclr' for the pin name
ie : Pin name : sclr
Pin location : Pin_B4
Parameters
Pin Name
data
Pin Location
Pin_AA12
OK
Cancel
Help
Apply