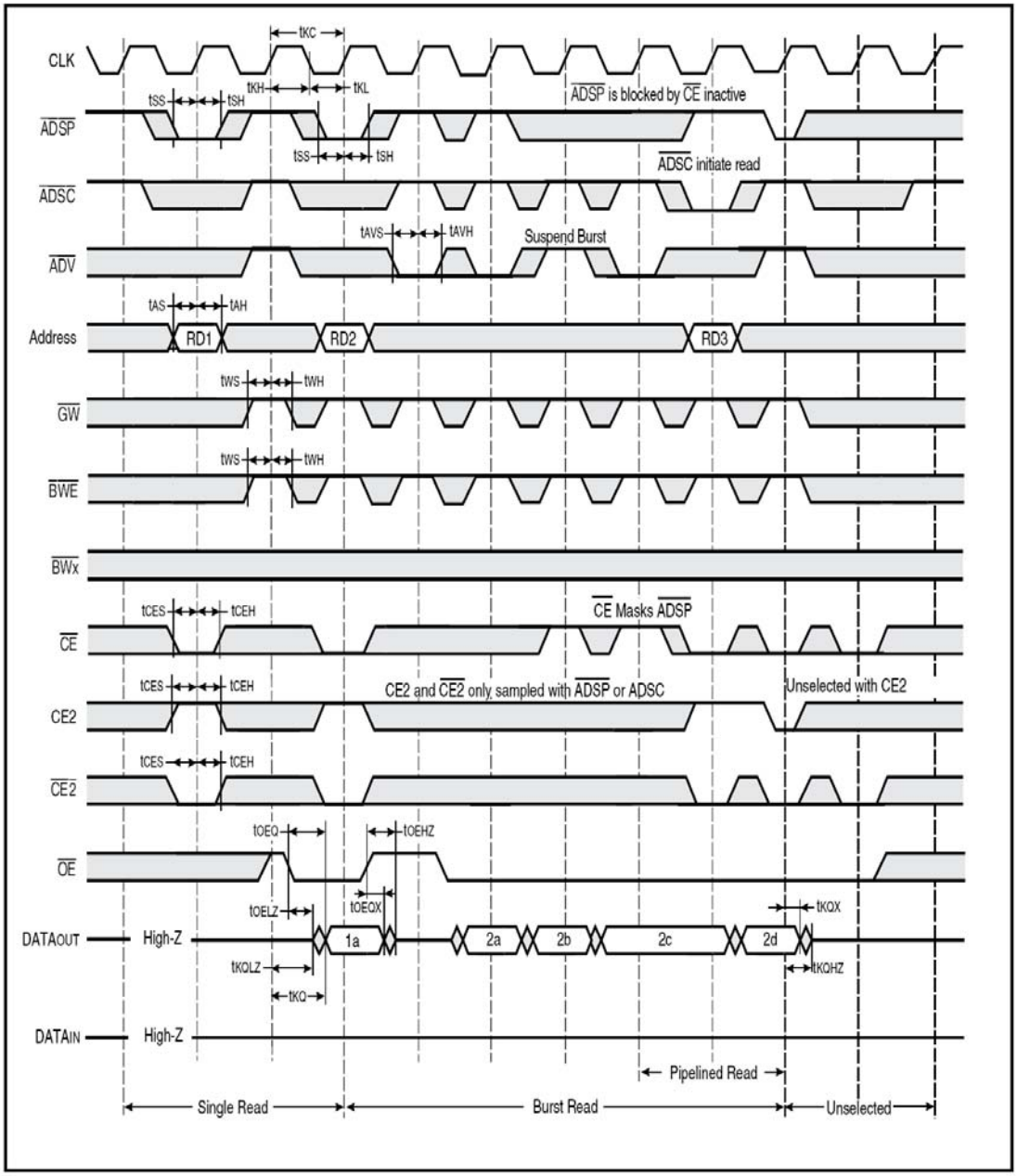
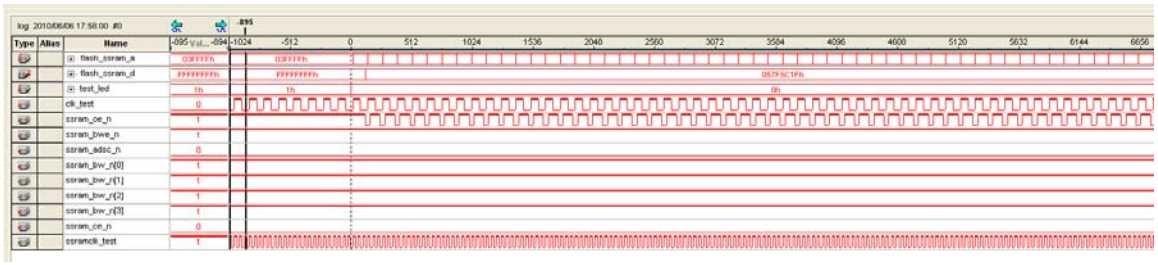
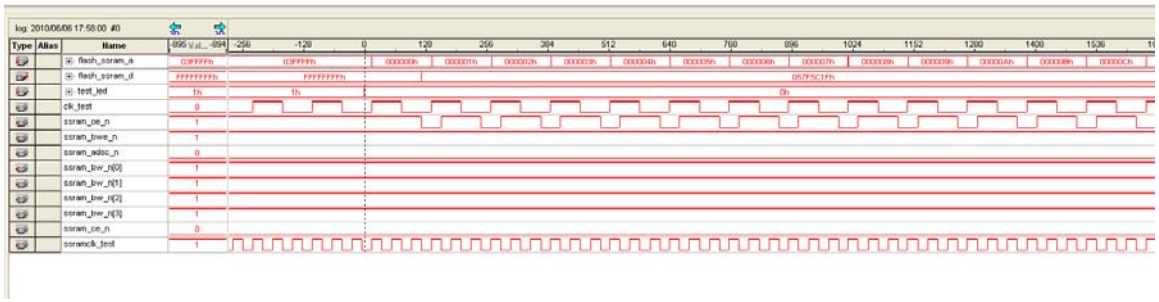
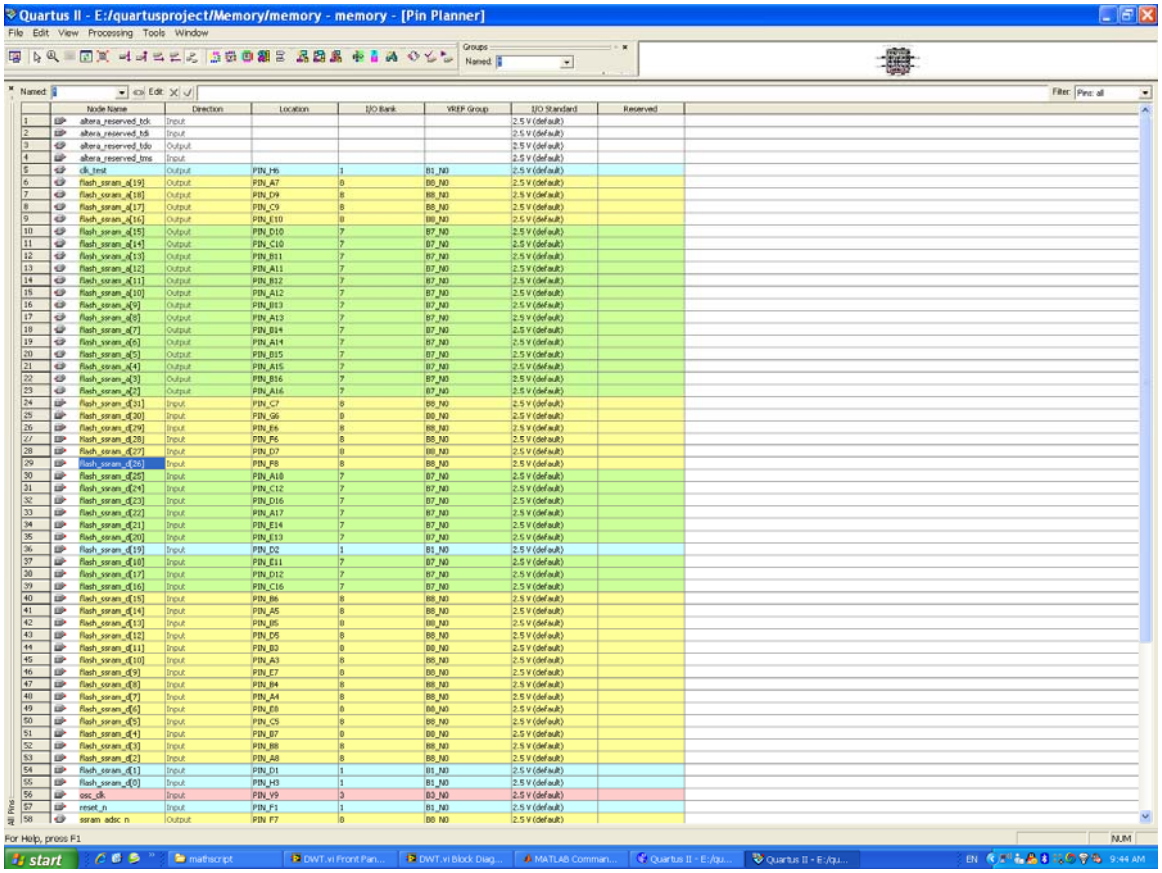
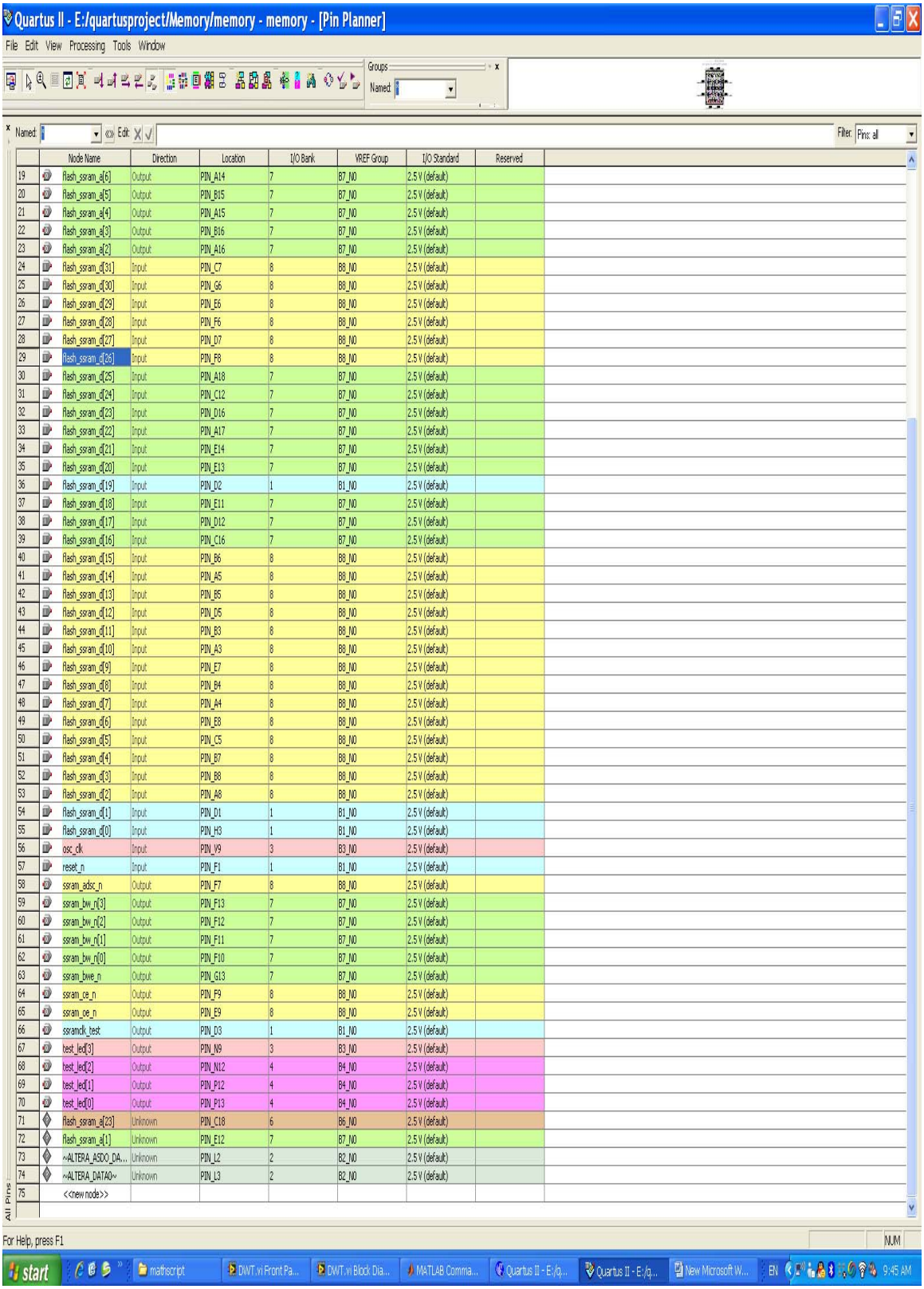
READ/WRITE CYCLE TIMING



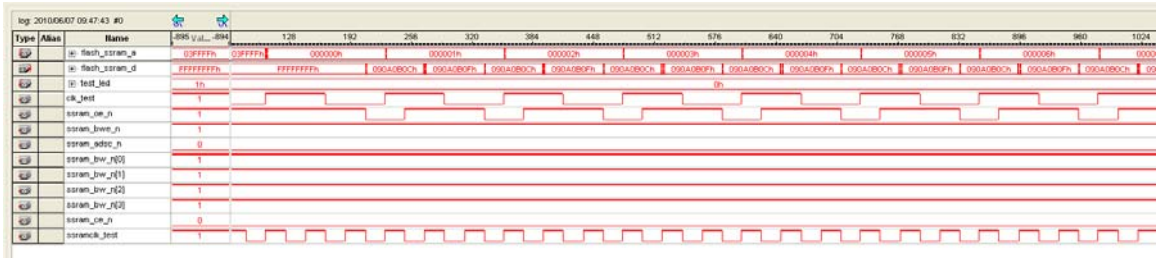


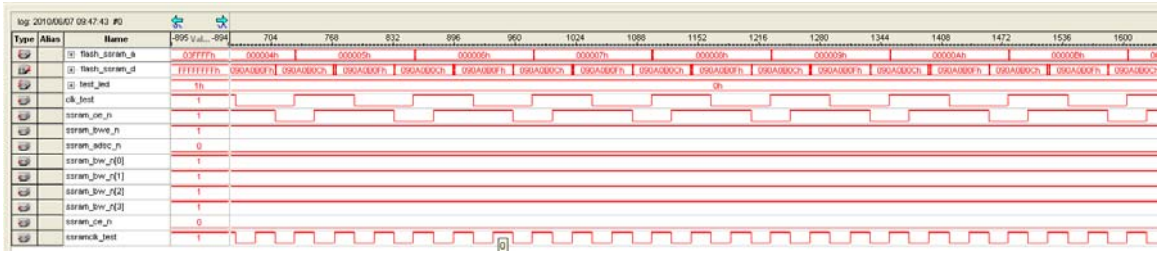


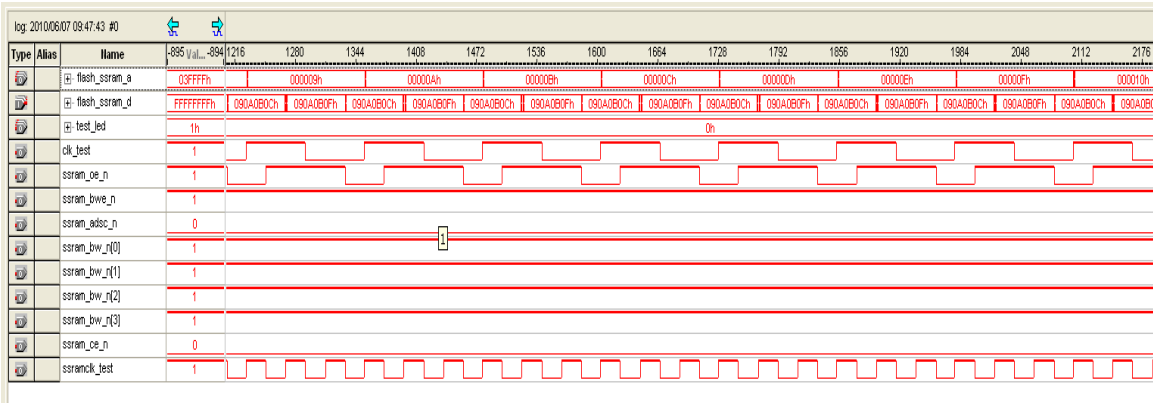

Quartus II - E:/quartusproject/Memory/memory - memory - [Pin Planner]
File Edit View Processing Tools Window
For Help, press F1
start



	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
19	flash_ssram_a[6]	Output	PIN_A14	7	B7_N0	2.5 V (default)	
20	flash_ssram_a[5]	Output	PIN_B15	7	B7_N0	2.5 V (default)	
21	flash_ssram_a[4]	Output	PIN_A15	7	B7_N0	2.5 V (default)	
22	flash_ssram_a[3]	Output	PIN_B16	7	B7_N0	2.5 V (default)	
23	flash_ssram_a[2]	Output	PIN_A16	7	B7_N0	2.5 V (default)	
24	flash_ssram_d[31]	Input	PIN_C7	8	B8_N0	2.5 V (default)	
25	flash_ssram_d[30]	Input	PIN_G6	8	B8_N0	2.5 V (default)	
26	flash_ssram_d[29]	Input	PIN_E6	8	B8_N0	2.5 V (default)	
27	flash_ssram_d[28]	Input	PIN_F6	8	B8_N0	2.5 V (default)	
28	flash_ssram_d[27]	Input	PIN_D7	8	B8_N0	2.5 V (default)	
29	flash_ssram_d[26]	Input	PIN_F8	8	B8_N0	2.5 V (default)	
30	flash_ssram_d[25]	Input	PIN_A18	7	B7_N0	2.5 V (default)	
31	flash_ssram_d[24]	Input	PIN_C12	7	B7_N0	2.5 V (default)	
32	flash_ssram_d[23]	Input	PIN_D16	7	B7_N0	2.5 V (default)	
33	flash_ssram_d[22]	Input	PIN_A17	7	B7_N0	2.5 V (default)	
34	flash_ssram_d[21]	Input	PIN_E14	7	B7_N0	2.5 V (default)	
35	flash_ssram_d[20]	Input	PIN_E13	7	B7_N0	2.5 V (default)	
36	flash_ssram_d[19]	Input	PIN_D2	1	B1_N0	2.5 V (default)	
37	flash_ssram_d[18]	Input	PIN_E11	7	B7_N0	2.5 V (default)	
38	flash_ssram_d[17]	Input	PIN_D12	7	B7_N0	2.5 V (default)	
39	flash_ssram_d[16]	Input	PIN_C16	7	B7_N0	2.5 V (default)	
40	flash_ssram_d[15]	Input	PIN_B6	8	B8_N0	2.5 V (default)	
41	flash_ssram_d[14]	Input	PIN_A5	8	B8_N0	2.5 V (default)	
42	flash_ssram_d[13]	Input	PIN_B5	8	B8_N0	2.5 V (default)	
43	flash_ssram_d[12]	Input	PIN_D5	8	B8_N0	2.5 V (default)	
44	flash_ssram_d[11]	Input	PIN_B3	8	B8_N0	2.5 V (default)	
45	flash_ssram_d[10]	Input	PIN_A3	8	B8_N0	2.5 V (default)	
46	flash_ssram_d[9]	Input	PIN_E7	8	B8_N0	2.5 V (default)	
47	flash_ssram_d[8]	Input	PIN_B4	8	B8_N0	2.5 V (default)	
48	flash_ssram_d[7]	Input	PIN_A4	8	B8_N0	2.5 V (default)	
49	flash_ssram_d[6]	Input	PIN_E8	8	B8_N0	2.5 V (default)	
50	flash_ssram_d[5]	Input	PIN_C5	8	B8_N0	2.5 V (default)	
51	flash_ssram_d[4]	Input	PIN_B7	8	B8_N0	2.5 V (default)	
52	flash_ssram_d[3]	Input	PIN_B8	8	B8_N0	2.5 V (default)	
53	flash_ssram_d[2]	Input	PIN_A8	8	B8_N0	2.5 V (default)	
54	flash_ssram_d[1]	Input	PIN_D1	1	B1_N0	2.5 V (default)	
55	flash_ssram_d[0]	Input	PIN_H3	1	B1_N0	2.5 V (default)	
56	osc_clk	Input	PIN_V9	3	B3_N0	2.5 V (default)	
57	reset_n	Input	PIN_F1	1	B1_N0	2.5 V (default)	
58	ssram_adsc_n	Output	PIN_F7	8	B8_N0	2.5 V (default)	
59	ssram_bw_n[3]	Output	PIN_F13	7	B7_N0	2.5 V (default)	
60	ssram_bw_n[2]	Output	PIN_F12	7	B7_N0	2.5 V (default)	
61	ssram_bw_n[1]	Output	PIN_F11	7	B7_N0	2.5 V (default)	
62	ssram_bw_n[0]	Output	PIN_F10	7	B7_N0	2.5 V (default)	
63	ssram_bwe_n	Output	PIN_G13	7	B7_N0	2.5 V (default)	
64	ssram_ce_n	Output	PIN_F9	8	B8_N0	2.5 V (default)	
65	ssram_oe_n	Output	PIN_E9	8	B8_N0	2.5 V (default)	
66	ssramclk_test	Output	PIN_D3	1	B1_N0	2.5 V (default)	
67	test_led[3]	Output	PIN_N9	3	B3_N0	2.5 V (default)	
68	test_led[2]	Output	PIN_N12	4	B4_N0	2.5 V (default)	
69	test_led[1]	Output	PIN_P12	4	B4_N0	2.5 V (default)	
70	test_led[0]	Output	PIN_P13	4	B4_N0	2.5 V (default)	
71	flash_ssram_a[23]	Unknown	PIN_C18	6	B6_N0	2.5 V (default)	
72	flash_ssram_a[1]	Unknown	PIN_E12	7	B7_N0	2.5 V (default)	
73	~ALTERA_ASDO_DA...	Unknown	PIN_L2	2	B2_N0	2.5 V (default)	
74	~ALTERA_DATA0~	Unknown	PIN_L3	2	B2_N0	2.5 V (default)	
75	<<new node>>						


log: 2010/06/07 09:47:43 #0
Type
Alias
Name
flash_ssram_a
flash_ssram_d
test_led
clk_test
ssram_oe_n
ssram_bwe_n
ssram_adsc_n
ssram_bw_n[0]
ssram_bw_n[1]
ssram_bw_n[2]
ssram_bw_n[3]
ssram_ce_n
ssramclk_test


log: 2010/06/07 09:47:43 #0
Type
Alias
Name
flash_ssram_a
flash_ssram_d
test_led
clk_test
ssram_oe_n
ssram_bwe_n
ssram_adsc_n
ssram_bw_n[0]
ssram_bw_n[1]
ssram_bw_n[2]
ssram_bw_n[3]
ssram_ce_n
ssramclk_test


log: 2010/06/07 09:47:43 #0
Type
Alias
Name
flash_ssram_a
flash_ssram_d
test_led
clk_test
ssram_oe_n
ssram_bwe_n
ssram_adsc_n
ssram_bw_n[0]
ssram_bw_n[1]
ssram_bw_n[2]
ssram_bw_n[3]
ssram_ce_n
ssramclk_test

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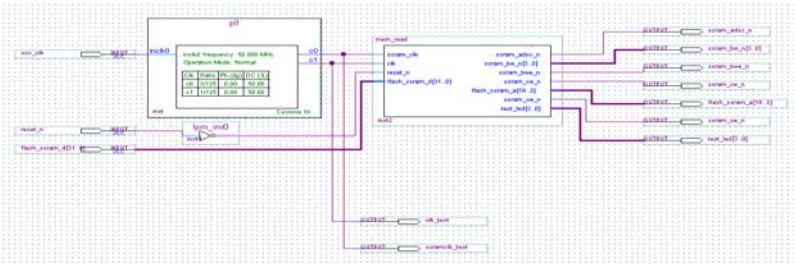
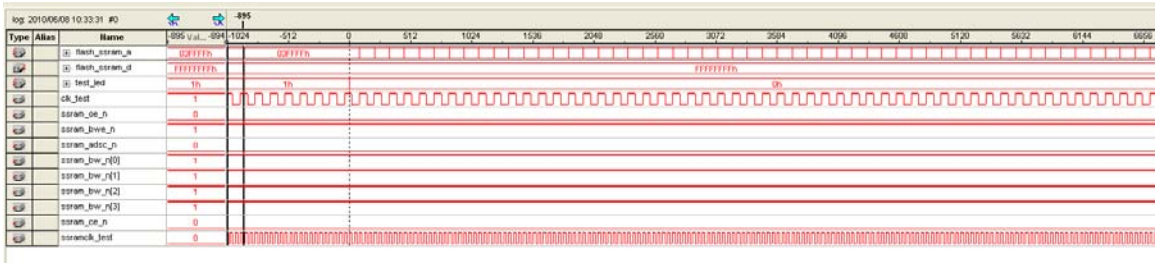


If making ssram_oe_n to be 0 always, the output will be



If making flash_oe/ce_n to be 1 always, the error output will be

Can't place multiple pins assigned to pin location Pin_E2