NOTES:

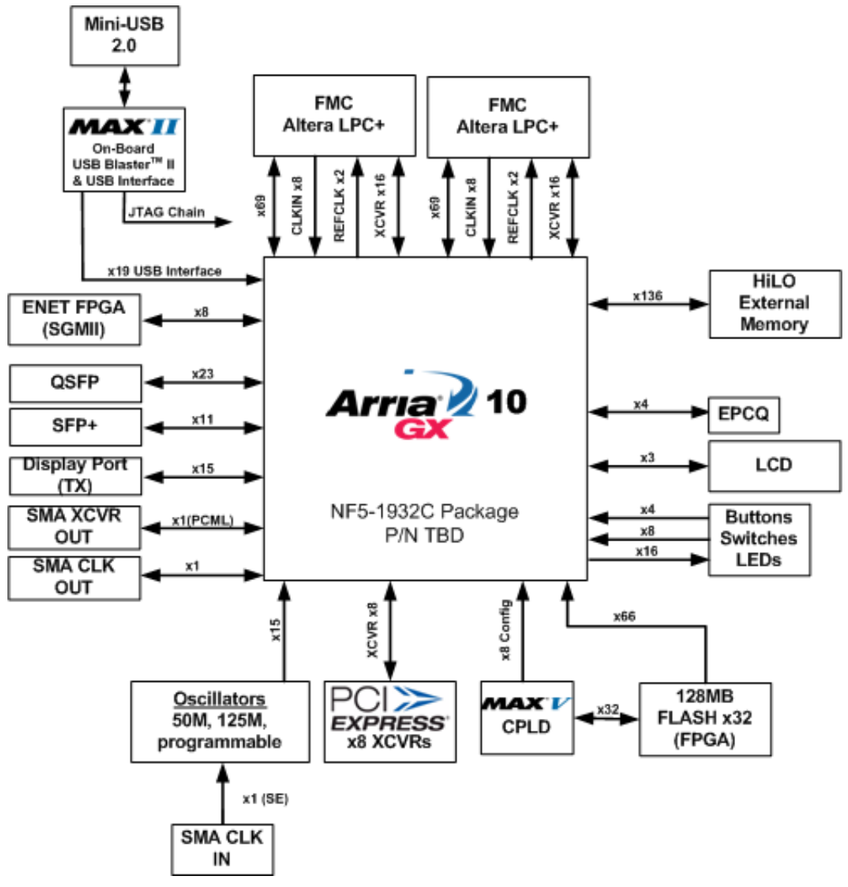
1. Project Drawing Numbers:

Raw PCB	100-0321301-E1
Gerber Files	110-0321301-E1
PCB Design Files	120-0321301-E1
Assembly Drawing	130-0321301-E1
Fab Drawing	140-0321301-E1
Schematic Drawing	150-0321301-E1
PCB Film	160-0321301-E1
Bill of Materials	170-0321301-E1
Schematic Design Files	180-0321301-E1
Functional Specification	210-0321301-E1
PCB Layout Guidelines	220-0321301-E1
Assembly Rework	320-0321301-E1

2. 1516 Parts, 84 Library Parts, 1524 Nets, 7856 Pins

Pre-Release Schematic
DO NOT COPY

Arria 10 FPGA Development Kit



REV	DATE	PAGES	DESCRIPTION
A1	12/26/2013	All	Initial
B1	02/23/2014	All	Rev B bug fixes
C1	07/25/2014	All	Rev C enhancements
D1	11/5/2014	All	Rev D bug fixes
E1	5/5/2015	All	Change from Enpirion 12V power to 5V power
E1.1	5/12/2015	All	Change U85 LDO input from 12V to 5V output from U19 for reduced power dissipation
E1.2	5/15/2015	All	Swap VDD_1.3V_SET and VDD_1.35V_SET. Fix ET4040 SDL and SDA swap

Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: **Arria 10 GX FPGA Development Kit**
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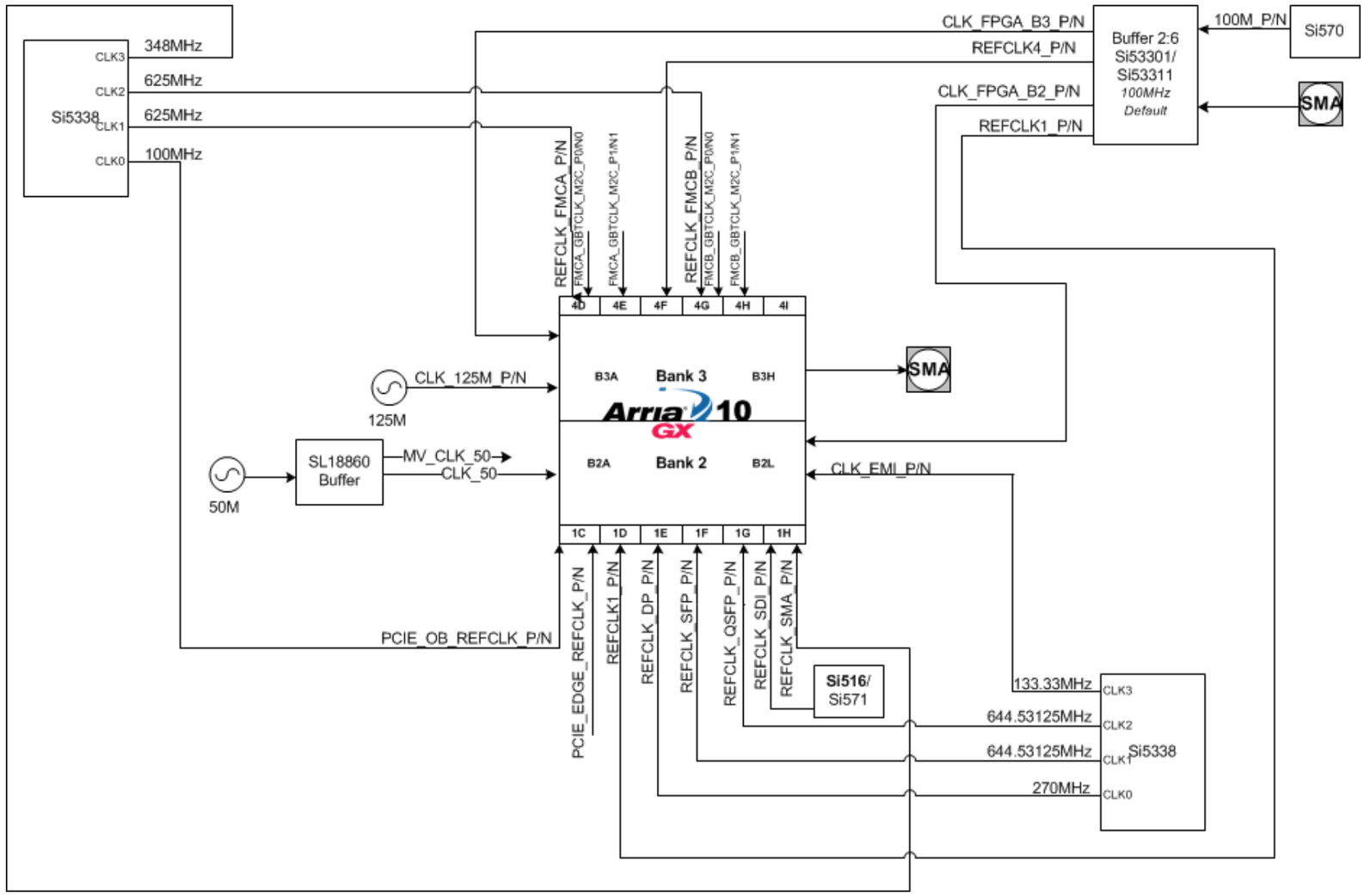
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 1 of 49

Clock Diagram



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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 2 of 49

PCI Express Edge Connector

11 PCIE_TX_P[7:0]
11 PCIE_TX_N[7:0]
11 PCIE_RX_P[7:0]
11 PCIE_RX_N[7:0]

3.3V_PCIE 12V_PCIE 12V_PCIE 3.3V_PCIE

J22

B1	+12V	PRSNT1_N	A1
B2	+12V	+12V	A2
B3	+12V	+12V	A3
B4	GND	GND	A4
B5	SMCLK	JTAG_TCK	A5
B6	SMDAT	JTAG_TDI	A6
B7	GND	JTAG_TDO	A7
B8	+3_3V	JTAG_TMS	A8
B9	JTAG_TRSTN	+3_3V	A9
B10	+3_3VAUX	+3_3V	A10
B11	WAKE_N	PERST_N	A11
	KEY		
B12	RSVD1	GND	A12
B13	GND	REFCLK+	A13
B14	PET0P	REFCLK-	A14
B15	PET0N	GND	A15
B16	GND	PER0P	A16
B17	PRSNT2_N_X1	PER0N	A17
B18	GND	GND	A18
B19	PET1P X4	RSVD2	A19
B20	PET1N	GND	A20
B21	GND	PER1P	A21
B22	GND	PER1N	A22
B23	PET2P	GND	A23
B24	PET2N	GND	A24
B25	GND	PER2P	A25
B26	GND	PER2N	A26
B27	PET3P	GND	A27
B28	PET3N	GND	A28
B29	GND	PER3P	A29
B30	RSVD3	PER3N	A30
B31	PRSNT2_N_X4	GND	A31
B32	GND	RSVD4	A32
B33	PET4P X8	RSVD5	A33
B34	PET4N	GND	A34
B35	GND	PER4P	A35
B36	GND	PER4N	A36
B37	PET5P	GND	A37
B38	PET5N	GND	A38
B39	GND	PER5P	A39
B40	GND	PER5N	A40
B41	PET6P	GND	A41
B42	PET6N	GND	A42
B43	GND	PER6P	A43
B44	GND	PER6N	A44
B45	PET7P	GND	A45
B46	PET7N	GND	A46
B47	GND	PER7P	A47
B48	PRSNT2_N_X8	PER7N	A48
B49	GND	GND	A49

PCIE_Slot

PCIE_EDGE_SMBCLK
PCIE_EDGE_SMBDAT
R552 DNI 3.3V_PCIE_AUX
PCIE_EDGE_WAKEn R546 DNI PCIE_WAKEn_R
PCIE_PRSNT1n
PCIE_EDGE_PERSTn
11 PCIE_EDGE_REFCLK_P
11 PCIE_EDGE_REFCLK_N

PCIE_RX_P0 PCIE_RX_N0 PCIE_PRSNT2n_x1
PCIE_RX_P1 PCIE_RX_N1
PCIE_RX_P2 PCIE_RX_N2
PCIE_RX_P3 PCIE_RX_N3
PCIE_PRSNT2n_x4
PCIE_RX_P4 PCIE_RX_N4
PCIE_RX_P5 PCIE_RX_N5
PCIE_RX_P6 PCIE_RX_N6
PCIE_RX_P7 PCIE_RX_N7
PCIE_PRSNT2n_x8

PCIE_TX_CP0	0.22uF	C722	PCIE_TX_P0	
PCIE_TX_CN0	0.22uF	C721	PCIE_TX_N0	
PCIE_TX_CP1	0.22uF	C720	PCIE_TX_P1	
PCIE_TX_CN1	0.22uF	C719	PCIE_TX_N1	
PCIE_TX_CP2	0.22uF	C718	PCIE_TX_P2	
PCIE_TX_CN2	0.22uF	C717	PCIE_TX_N2	
PCIE_TX_CP3	0.22uF	C716	PCIE_TX_P3	
PCIE_TX_CN3	0.22uF	C715	PCIE_TX_N3	
PCIE_TX_CP4	0.22uF	C714	PCIE_TX_P4	
PCIE_TX_CN4	0.22uF	C713	PCIE_TX_N4	
PCIE_TX_CP5	0.22uF	C712	PCIE_TX_P5	
PCIE_TX_CN5	0.22uF	C711	PCIE_TX_N5	
PCIE_TX_CP6	0.22uF	C710	PCIE_TX_P6	
PCIE_TX_CN6	0.22uF	C709	PCIE_TX_N6	
PCIE_TX_CP7	0.22uF	C708	PCIE_TX_P7	
PCIE_TX_CN7	0.22uF	C707	PCIE_TX_N7	

Link Width DIP Switch

SW3 DIPSWITCH4

1	8	PCIE_PRSNT2n_x1
2	7	PCIE_PRSNT2n_x4
3	6	PCIE_PRSNT2n_x8
4	5	17,34 VDD_1.35V_SET
		34 VDD_1.3V_SET

QDRIV needs 1.3V VDD.
SW3.4 allows changing of
1.35V to 1.3V for QDRIV.

3.3V
U75 SN74LVC1G08_6PIN
A VCC
A&B=Y
B Y
GND NC
PB_PERSTn
PCIE_3P3V_PERSTn

S8 PB Switch
PB_PERSTn R544 10.0K

3.3V C692 1uF C693 0.1uF
1.8V C706 0.1uF

U74 MAX3378_UCSP

PCIE_3P3V_PERSTn	C1	A1	7 PCIE_PERSTn
PCIE_EDGE_SMBCLK	C2	A2	7 PCIE_SMBCLK
PCIE_EDGE_SMBDAT	C3	A3	4 PCIE_SMBDAT
PCIE_EDGE_WAKEn	C4	A4	7 PCIE_WAKEn

VCC IO VCC1 IO VCC2 IO VCC3 IO VCC4
VL IO VL1 IO VL2 IO VL3 IO VL4
1.8V B1 B2 B3 B4 TS GND

75-ohm to 100-ohm XCVR traces.

12V_PCIE
C254 0.1uF C255 0.1uF C256 0.1uF C725 0.1uF C724 0.1uF

3.3V_PCIE
C258 0.1uF C257 0.1uF C723 0.1uF

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 3 of 49

Arria 10 GX Bank 2

U28C

ARRIA 10 - BANK 2I-2L

	QSFP_LP_MODE	AK34	IO,LVDS2I_1P,DQ12L	BANK-2I	IO,LVDS2K_1P,DQ4L	D32	MEM_DQ_ADDR_CMD3
	QSFP_INTERRUPTn	AL34	IO,LVDS2I_1N,DQ12L		IO,LVDS2K_1N,DQ4L	C33	MEM_DQ_ADDR_CMD4
	DP_HOT_PLUG	AM30	IO,LVDS2I_2P,DQ12L		IO,LVDS2K_2P,DQ4L	B32	MEM_DQ_ADDR_CMD2
	CLOCK_SDA	AN30	IO,LVDS2I_2N,DQ12L		IO,LVDS2K_2N,DQ4L	A32	MEM_DQ_ADDR_CMD0
		AL32	IO,LVDS2I_3P,DQ12L		IO,LVDS2K_3P,DQ4L	B33	MEM_DQ_ADDR_CMD5
	DP_RETURN	AL33	IO,LVDS2I_3N,DQ12L		IO,LVDS2K_3N,DQ4L	A33	MEM_DQ_ADDR_CMD1
	DP_CONFIG2	AK32	IO,LVDS2I_5P,DQ12L		IO,LVDS2K_5P,DQ4L	C35	MEM_DQ_ADDR_CMD7
	DP_CONFIG1	AK31	IO,LVDS2I_5N,DQ12L		IO,LVDS2K_5N,DQ4L	D34	MEM_DQ_ADDR_CMD6
		AM31	IO,LVDS2I_6P,DQ12L		IO,LVDS2K_6P,DQ4L	E35	MEM_ADDR_CMD29
		AM32	IO,LVDS2I_6N,DQ12L		IO,LVDS2K_6N,DQ4L	E34	MEM_DQ_ADDR_CMD8
	DP_AUX_CH_P	AN34	IO,LVDS2I_4P,DQS12L		IO,LVDS2K_4P,DQS4L	D33	MEM_DQS_ADDR_CMD_P
ENABLE ARRIA 10 OCT ->	DP_AUX_CH_N	AM35	IO,LVDS2I_4N,DQSN12L		IO,LVDS2K_4N,DQSN4L	C34	MEM_DQS_ADDR_CMD_N
		AR32	IO,LVDS2I_7P,DQ13L		IO,LVDS2K_7P,DQ5L	G35	MEM_ADDR_CMD17
		AP32	IO,LVDS2I_7N,DQ13L		IO,LVDS2K_7N,DQ5L	H35	MEM_ADDR_CMD18
		AT37	IO,LVDS2I_8P,DQ13L		IO,LVDS2K_8P,DQ5L	G33	MEM_ADDR_CMD19
	PCIE_SMBDAT	AU37	IO,LVDS2I_8N,DQ13L		IO,LVDS2K_8N,DQ5L	F33	MEM_ADDR_CMD16
		AP34	IO,LVDS2I_9P,DQ13L		IO,LVDS2K_9P,DQ5L	E32	MEM_ADDR_CMD15
		AP33	IO,LVDS2I_9N,DQ13L		IO,LVDS2K_9N,DQ5L	F32	MEM_ADDR_CMD26
100, 1%	R449 RZQ_B2I	AR34	IO,RZQ_2I,LVDS2I_11P,DQ13L		IO,RZQ_2K,LVDS2K_11P,DQ5L	J34 24	RZQ_B2K
	SFP_TX_DISABLE	AR35	IO,LVDS2I_11N,DQ13L		IO,LVDS2K_11N,DQ5L	H34	MEM_ADDR_CMD12
	SFP_MOD0_PRSNTn	AT30	IO,LVDS2I_14P,DQ14L		IO,LVDS2K_14P,DQ6L	J33	MEM_ADDR_CMD8
	SFP_MOD2_SDA	AR31	IO,LVDS2I_14N,DQ14L		IO,LVDS2K_14N,DQ6L	J32	MEM_ADDR_CMD9
	SFP_RS1	AT34	IO,LVDS2I_16P,DQS14L		IO,LVDS2K_17P,DQ6L	N34	MEM_ADDR_CMD2
	SFP_TX_FAULT	AT35	IO,LVDS2I_16N,DQSN14L		IO,LVDS2K_17N,DQ6L	M35	MEM_ADDR_CMD3
	SFP_RS0	AN31	IO,LVDS2I_17P,DQ14L		IO,LVDS2K_18P,DQ6L	M32	MEM_ADDR_CMD0
	SFP_MOD1_SCL	AP31	IO,LVDS2I_17N,DQ14L		IO,LVDS2K_18N,DQ6L	L32	MEM_ADDR_CMD1
	QSFP_SDA	AU31	IO,LVDS2I_18P,DQ14L		IO,LVDS2K_16P,DQS6L	L34	MEM_ADDR_CMD4
	SFP_RX_LOS	AU30	IO,LVDS2I_18N,DQ14L		IO,LVDS2K_16N,DQSN6L	K34	MEM_ADDR_CMD5
	QSFP_MOD_PRSn	AU36	IO,LVDS2I_19P,DQ15L		IO,LVDS2K_19P,DQ7L	U32	MEM_ADDR_CMD30
	QSFP_MOD_SELn	AU35	IO,LVDS2I_19N,DQ15L		IO,LVDS2K_19N,DQ7L	T32	MEM_ADDR_CMD31
	QSFP_SCL	AV34	IO,LVDS2I_20P,DQ15L		IO,LVDS2K_20P,DQ7L	R30	MEM_CLK_P
	QSFP_RSTn	AV35	IO,LVDS2I_20N,DQ15L		IO,LVDS2K_20N,DQ7L	R31	MEM_CLK_N
	SDI_MF2_MUTE	AY35	IO,LVDS2I_21P,DQ15L		IO,LVDS2K_21P,DQ7L	U33	MEM_ADDR_CMD20
	SDI_TX_SD_HDn	AW34	IO,LVDS2I_21N,DQ15L		IO,LVDS2K_21N,DQ7L	T33	MEM_ADDR_CMD21
	DISP_I2C_SCL	AW33	IO,LVDS2I_23P,DQ15L		IO,LVDS2K_23P,DQ7L	R34	MEM_ADDR_CMD22
	CLOCK_SCL	AV33	IO,LVDS2I_23N,DQ15L		IO,LVDS2K_23N,DQ7L	P34	MEM_ADDR_CMD23
	DISP_I2C_SDA	AY34	IO,LVDS2I_24P,DQ15L		IO,LVDS2K_24P,DQ7L	T34	MEM_ADDR_CMD28
	DISP_SPISS	BA35	IO,LVDS2I_24N,DQ15L		IO,LVDS2K_24N,DQ7L	T35	MEM_ADDR_CMD27
	SDI_MF0_BYPASS	AW32	IO,LVDS2I_22P,DQS15L		IO,LVDS2K_22P,DQS7L	N33	MEM_ADDR_CMD24
	SDI_MF1_AUTO_SLEEP	AY32	IO,LVDS2I_22N,DQSN15L		IO,LVDS2K_22N,DQSN7L	P33	MEM_ADDR_CMD25
	MEM_DQB0	AC31	IO,LVDS2J_1P,DQ8L	BANK-2J	IO,LVDS2L_1P,DQ0L	D26	MEM_DQA6
	MEM_DQB4	AD31	IO,LVDS2J_1N,DQ8L		IO,LVDS2L_1N,DQ0L	E26	MEM_DMA0
	MEM_DQB6	AD33	IO,LVDS2J_2P,DQ8L		IO,LVDS2L_2P,DQ0L	A28	MEM_DQA1
	MEM_DQB5	AD32	IO,LVDS2J_2N,DQ8L		IO,LVDS2L_2N,DQ0L	A27	MEM_DQA2
	MEM_DMB0	AB32	IO,LVDS2J_3P,DQ8L		IO,LVDS2L_3P,DQ0L	B28	MEM_DQA0
	MEM_DQB1	AB31	IO,LVDS2J_3N,DQ8L		IO,LVDS2L_3N,DQ0L	B27	MEM_DQA3
	MEM_DQB3	Y31	IO,LVDS2J_5P,DQ8L		IO,LVDS2L_5P,DQ0L	D27	MEM_DQA4
	MEM_DQB2	W31	IO,LVDS2J_5N,DQ8L		IO,LVDS2L_5N,DQ0L	E27	MEM_DQA5
	MEM_QKB_P0	Y30	IO,LVDS2J_6P,DQ8L		IO,LVDS2L_6P,DQ0L	C28	MEM_QKA_P0
QDR4 QKB_P0 ->	MEM_DQB7	AA30	IO,LVDS2J_6N,DQ8L		IO,LVDS2L_6N,DQ0L	D28	MEM_DQA7 <- QDR4 QKA_P0
	MEM_DQSB_P0	Y32	IO,LVDS2J_4P,DQS8L		IO,LVDS2L_4P,DQS0L	B26	MEM_DQSA_P0
	MEM_DQSB_N0	AA32	IO,LVDS2J_4N,DQSN8L		IO,LVDS2L_4N,DQSN0L	C26	MEM_DQSA_N0
	MEM_DQB8	AE31	IO,LVDS2J_7P,DQ9L		IO,LVDS2L_7P,DQ1L	F28	MEM_DQA15
	MEM_DQB9	AE32	IO,LVDS2J_7N,DQ9L		IO,LVDS2L_7N,DQ1L	F27	MEM_DQA13
	MEM_DQB10	AE30	IO,LVDS2J_8P,DQ9L		IO,LVDS2L_8P,DQ1L	G28	MEM_DQA12
	MEM_DQB11	AF30	IO,LVDS2J_8N,DQ9L		IO,LVDS2L_8N,DQ1L	G27	MEM_DMA1
	MEM_DQB12	AG33	IO,LVDS2J_9P,DQ9L		IO,LVDS2L_9P,DQ1L	H25	MEM_DQA9
	MEM_DQB14	AH33	IO,LVDS2J_9N,DQ9L		IO,LVDS2L_9N,DQ1L	G25	MEM_DQA8
	MEM_DQB32	AF32	IO,RZQ_2J,LVDS2J_11P,DQ9L		IO,RZQ_2L,LVDS2L_11P,DQ1L	J28	MEM_DQA32
	MEM_DQB13	AG32	IO,LVDS2J_11N,DQ9L		IO,LVDS2L_11N,DQ1L	K27	MEM_DQA14
	MEM_DQB18	W32	IO,LVDS2J_14P,DQ10L		IO,LVDS2L_14P,DQ2L	D31	MEM_DQA16
	MEM_DQB17	W33	IO,LVDS2J_14N,DQ10L		IO,LVDS2L_14N,DQ2L	C31	MEM_DQA19
	MEM_DQB21	W35	IO,LVDS2J_17P,DQ10L		IO,LVDS2L_17P,DQ2L	E30	MEM_DQA21
	MEM_DMB2	Y35	IO,LVDS2J_17N,DQ10L		IO,LVDS2L_17N,DQ2L	E31	MEM_DQA17
	MEM_QKB_P1	V33	IO,LVDS2J_18P,DQ10L		IO,LVDS2L_18P,DQ2L	E29	MEM_QKA_P1
QDR4 QKB_P1 ->	MEM_DQB23	V34	IO,LVDS2J_18N,DQ10L		IO,LVDS2L_18N,DQ2L	D29	MEM_DQA23 <- QDR4 QKA_P1
	MEM_DQSB_P2	AA34	IO,LVDS2J_16P,DQS10L		IO,LVDS2L_16P,DQS2L	C30	MEM_DQSA_P2
	MEM_DQSB_N2	AA33	IO,LVDS2J_16N,DQSN10L		IO,LVDS2L_16N,DQSN2L	C29	MEM_DQSA_N2
	MEM_DQB31	AD34	IO,LVDS2J_19P,DQ11L		IO,LVDS2L_19P,DQ3L	F30	MEM_DMA3
	MEM_DMB3	AC34	IO,LVDS2J_19N,DQ11L		IO,LVDS2L_19N,DQ3L	F29	MEM_DQA31
	MEM_DQB33	AB33	IO,LVDS2J_20P,DQ11L		IO,LVDS2L_20P,DQ3L	K29	MEM_DQA29
	MEM_DQB30	AC33	IO,LVDS2J_20N,DQ11L		IO,LVDS2L_20N,DQ3L	J29	MEM_DQA30
	MEM_DQB28	AD35	IO,LVDS2J_21P,DQ11L		IO,LVDS2L_21P,DQ3L	K31	MEM_DQA27
	MEM_DQB29	AE34	IO,LVDS2J_21N,DQ11L		IO,LVDS2L_21N,DQ3L	K30	MEM_DQA24
	MEM_DQB26	AJ33	IO,LVDS2J_23P,DQ11L		IO,LVDS2L_23P,DQ3L	G30	MEM_DQA26
	MEM_DQB25	AJ34	IO,LVDS2J_23N,DQ11L		IO,LVDS2L_23N,DQ3L	G31	MEM_DQA33
	MEM_DQB27	AH34	IO,LVDS2J_24P,DQ11L		IO,LVDS2L_24P,DQ3L	H29	MEM_DQA28
	MEM_DQB24	AH35	IO,LVDS2J_24N,DQ11L		IO,LVDS2L_24N,DQ3L	H30	MEM_DQA25
	MEM_DQSB_P3	AF33	IO,LVDS2J_22P,DQS11L		IO,LVDS2L_22P,DQS3L	L30	MEM_DQSA_P3
	MEM_DQSB_N3	AF34	IO,LVDS2J_22N,DQSN11L		IO,LVDS2L_22N,DQSN3L	L29	MEM_DQSA_N3

VCCIO = 1.8V

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

10AX115F1932C

Stratix 5 RZQ
100-ohm for 50-ohm RT or 25-ohm RS.

CLOCK INTERFACE
- 9 CLOCK_SDA
- 9 CLOCK_SCL

DISPLAYPORT INTERFACE
- 18 DP_HOT_PLUG
- 18 DP_RETURN
- 18 DP_AUX_CH_P
- 18 DP_AUX_CH_N
- 18 DP_CONFIG1
- 18 DP_CONFIG2
- 24 DISP_I2C_SCL
- 24 DISP_I2C_SDA
- 24 DISP_SPISS

QSFP INTERFACE
- 21 QSFP_MOD_SELn
- 21 QSFP_RSTn
- 21 QSFP_SCL
- 21 QSFP_SDA
- 21 QSFP_INTERRUPTn
- 21 QSFP_MOD_PRSn
- 21 QSFP_LP_MODE

SFP+ INTERFACE
- 22 SFP_RS0
- 22 SFP_RS1
- 22 SFP_TX_DISABLE
- 22 SFP_RX_LOS
- 22 SFP_TX_FAULT
- 22 SFP_MOD0_PRSNTn
- 22 SFP_MOD1_SCL
- 22 SFP_MOD2_SDA

SDI INTERFACE
- 13,23 SDI_MF2_MUTE
- 13,23 SDI_MF0_BYPASS
- 13,23 SDI_MF1_AUTO_SLEEP
- 13,23 SDI_TX_SD_HDn

PCIe INTERFACE
- 3 PCIE_SMBDAT

MEMORY INTERFACE
- 8,17 MEM_ADDR_CMD[31:0]
- 17 MEM_CLK_P
- 17 MEM_CLK_N
- 17 MEM_DQ_ADDR_CMD[8:0]
- 17 MEM_DQS_ADDR_CMD_P
- 17 MEM_DQS_ADDR_CMD_N
- 8,17 MEM_DMA[3:0]
- 8,17 MEM_DQA[33:0]
- 8,17 MEM_DQSA_P[3:0]
- 8,17 MEM_DQSA_N[3:0]
- 17 MEM_QKA_P[1:0]
- 8,17 MEM_DMB[3:0]
- 8,17 MEM_DQB[33:0]
- 8,17 MEM_DQSB_P[3:0]
- 8,17 MEM_DQSB_N[3:0]
- 17 MEM_QKB_P[1:0]

Title: Arria 10 GX FPGA Development Kit

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 4 of 49

Arria 10 Bank 3A-3D

U28D

ARRIA 10 - BANK 3A-3D

		BANK-3A	BANK-3C	BANK-3D	BANK-3B
		VCCIO = 1.8V	FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)	VCCIO = 1.8V	FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)
FM_D28	AP22	IO,LVDS3A_1P,DQ60R	IO,LVDS3C_1P,DQ52R	IO,LVDS3D_1P,DQ48R	IO,LVDS3B_1P,DQ56R
FM_D20	AP23	IO,LVDS3A_1N,DQ60R	IO,LVDS3C_1N,DQ52R	IO,LVDS3D_1N,DQ48R	IO,LVDS3B_1N,DQ56R
FM_D16	AT25	IO,LVDS3A_2P,DQ60R	IO,LVDS3C_2P,DQ52R	IO,LVDS3D_2P,DQ48R	IO,LVDS3B_2P,DQ56R
FM_D27	AR25	IO,LVDS3A_2N,DQ60R	IO,LVDS3C_2N,DQ52R	IO,LVDS3D_2N,DQ48R	IO,LVDS3B_2N,DQ56R
FM_D26	AT23	IO,LVDS3A_3P,DQ60R	IO,LVDS3C_3P,DQ52R	IO,LVDS3D_3P,DQ48R	IO,LVDS3B_3P,DQ56R
FM_D22	AT24	IO,LVDS3A_3N,DQ60R	IO,LVDS3C_3N,DQ52R	IO,LVDS3D_3N,DQ48R	IO,LVDS3B_3N,DQ56R
FM_D12	AP26	IO,LVDS3A_5P,DQ60R	IO,LVDS3C_5P,DQ52R	IO,LVDS3D_5P,DQ48R	IO,LVDS3B_5P,DQ56R
FM_D15	AR26	IO,LVDS3A_5N,DQ60R	IO,LVDS3C_5N,DQ52R	IO,LVDS3D_5N,DQ48R	IO,LVDS3B_5N,DQ56R
FM_D24	AU23	IO,LVDS3A_6P,DQ60R	IO,LVDS3C_6P,DQ52R	IO,LVDS3D_6P,DQ48R	IO,LVDS3B_6P,DQ56R
FM_D30	AU22	IO,LVDS3A_6N,DQ60R	IO,LVDS3C_6N,DQ52R	IO,LVDS3D_6N,DQ48R	IO,LVDS3B_6N,DQ56R
FM_D25	AR24	IO,LVDS3A_4P,DQS60R	IO,LVDS3C_4P,DQS52R	IO,LVDS3D_4P,DQS48R	IO,LVDS3B_4P,DQS56R
FM_D19	AP24	IO,LVDS3A_4N,DQSN60R	IO,LVDS3C_4N,DQSN52R	IO,LVDS3D_4N,DQSN48R	IO,LVDS3B_4N,DQSN56R
FM_D14	BA25	IO,LVDS3A_7P,DQ61R	IO,LVDS3C_7P,DQ53R	IO,LVDS3D_7P,DQ49R	IO,LVDS3B_7P,DQ57R
FM_D4	AY25	IO,LVDS3A_7N,DQ61R	IO,LVDS3C_7N,DQ53R	IO,LVDS3D_7N,DQ49R	IO,LVDS3B_7N,DQ57R
FM_D6	AY24	IO,LVDS3A_8P,DQ61R	IO,LVDS3C_8P,DQ53R	IO,LVDS3D_8P,DQ49R	IO,LVDS3B_8P,DQ57R
FM_D13	BA24	IO,LVDS3A_8N,DQ61R	IO,LVDS3C_8N,DQ53R	IO,LVDS3D_8N,DQ49R	IO,LVDS3B_8N,DQ57R
FM_D2	AU25	IO,LVDS3A_9P,DQ61R	IO,LVDS3C_9P,DQ53R	IO,LVDS3D_9P,DQ49R	IO,LVDS3B_9P,DQ57R
FM_D7	AV25	IO,LVDS3A_9N,DQ61R	IO,LVDS3C_9N,DQ53R	IO,LVDS3D_9N,DQ49R	IO,LVDS3B_9N,DQ57R
FM_D11	AW22	RZQ_3A,LVDS3A_11P,DQ61R	IO,RZQ_3C,LVDS3C_11P,DQ53R	IO,RZQ_3D,LVDS3D_11P,DQ49R	IO,RZQ_3B,LVDS3B_11P,DQ57R
FLASH_RDYBSYn0	AY22	IO,LVDS3A_11N,DQ61R	IO,LVDS3C_11N,DQ53R	IO,LVDS3D_11N,DQ49R	IO,LVDS3B_11N,DQ57R
FLASH_ADVn	BC25	IO,LVDS3A_14P,DQ62R	IO,LVDS3C_14P,DQ54R	IO,LVDS3D_14P,DQ50R	IO,LVDS3B_14P,DQ58R
FLASH_CLK	BB25	IO,LVDS3A_14N,DQ62R	IO,LVDS3C_14N,DQ54R	IO,LVDS3D_14N,DQ50R	IO,LVDS3B_14N,DQ58R
FLASH_WEn	BD26	IO,LVDS3A_17P,DQ62R	IO,LVDS3C_17P,DQ54R	IO,LVDS3D_17P,DQ50R	IO,LVDS3B_17P,DQ58R
FLASH_OEn	BC26	IO,LVDS3A_17N,DQ62R	IO,LVDS3C_17N,DQ54R	IO,LVDS3D_17N,DQ50R	IO,LVDS3B_17N,DQ58R
FM_D1	BA22	IO,LVDS3A_18P,DQ62R	IO,LVDS3C_18P,DQ54R	IO,LVDS3D_18P,DQ50R	IO,LVDS3B_18P,DQ58R
FLASH_CEn0	BB22	IO,LVDS3A_18N,DQ62R	IO,LVDS3C_18N,DQ54R	IO,LVDS3D_18N,DQ50R	IO,LVDS3B_18N,DQ58R
FLASH_CEn1	BB23	IO,LVDS3A_16P,DQS62R	IO,LVDS3C_16P,DQS54R	IO,LVDS3D_16P,DQS50R	IO,LVDS3B_16P,DQS58R
FLASH_RESETn	BA23	IO,LVDS3A_16N,DQSN62R	IO,LVDS3C_16N,DQSN54R	IO,LVDS3D_16N,DQSN50R	IO,LVDS3B_16N,DQSN58R
FM_D3	BD21	IO,LVDS3A_19P,DQ63R	IO,LVDS3C_19P,DQ55R	IO,LVDS3D_19P,DQ51R	IO,LVDS3B_19P,DQ59R
FM_D5	BD22	IO,LVDS3A_19N,DQ63R	IO,LVDS3C_19N,DQ55R	IO,LVDS3D_19N,DQ51R	IO,LVDS3B_19N,DQ59R
FM_D29	BC19	IO,LVDS3A_20P,DQ63R	IO,LVDS3C_20P,DQ55R	IO,LVDS3D_20P,DQ51R	IO,LVDS3B_20P,DQ59R
FM_D23	BD19	IO,LVDS3A_20N,DQ63R	IO,LVDS3C_20N,DQ55R	IO,LVDS3D_20N,DQ51R	IO,LVDS3B_20N,DQ59R
FM_D17	BA19	IO,LVDS3A_21P,DQ63R	IO,LVDS3C_21P,DQ55R	IO,LVDS3D_21P,DQ51R	IO,LVDS3B_21P,DQ59R
FM_D18	BA20	IO,LVDS3A_21N,DQ63R	IO,LVDS3C_21N,DQ55R	IO,LVDS3D_21N,DQ51R	IO,LVDS3B_21N,DQ59R
FM_D8	BC21	IO,LVDS3A_23P,DQ63R	IO,LVDS3C_23P,DQ55R	IO,LVDS3D_23P,DQ51R	IO,LVDS3B_23P,DQ59R
FM_D9	BB21	IO,LVDS3A_23N,DQ63R	IO,LVDS3C_23N,DQ55R	IO,LVDS3D_23N,DQ51R	IO,LVDS3B_23N,DQ59R
FM_D10	BC20	IO,LVDS3A_24P,DQ63R	IO,LVDS3C_24P,DQ55R	IO,LVDS3D_24P,DQ51R	IO,LVDS3B_24P,DQ59R
FM_D0	BB20	IO,LVDS3A_24N,DQ63R	IO,LVDS3C_24N,DQ55R	IO,LVDS3D_24N,DQ51R	IO,LVDS3B_24N,DQ59R
FM_D31	BA17	IO,LVDS3A_22P,DQS63R	IO,LVDS3C_22P,DQS55R	IO,LVDS3D_22P,DQS51R	IO,LVDS3B_22P,DQS59R
FM_D21	BA18	IO,LVDS3A_22N,DQSN63R	IO,LVDS3C_22N,DQSN55R	IO,LVDS3D_22N,DQSN51R	IO,LVDS3B_22N,DQSN59R
FMCA_LA_RX_P4	AR16				
FMCA_LA_RX_N4	AP16				
FMCA_LA_TX_P11	AU18				
FMCA_LA_TX_N11	AT18				
FMCA_LA_TX_P3	AT17				
FMCA_LA_TX_N3	AU17				
FMCA_LA_TX_P5	AT14				
FMCA_LA_TX_N5	AR14				
FMCA_LA_RX_P3	AR15				
FMCA_LA_RX_N3	AT15				
FMCA_LA_TX_P6	AR17				
FMCA_LA_TX_N6	AP17				
FMCA_LA_RX_P14	AY17				
FMCA_LA_RX_N14	AW17				
FMCA_LA_RX_P1	AV14				
FMCA_LA_RX_N1	AW14				
FMCA_LA_TX_P14	AY16				
FMCA_LA_TX_N14	AW16				
FMCA_LA_RX_P10	AY15				
FMCA_LA_RX_N10	AY14				
FMCA_LA_RX_P5	AW18				
FMCA_LA_RX_N5	AV18				
FMCA_LA_TX_P8	AV19				
FMCA_LA_TX_N8	AW19				
FMCA_LA_TX_P16	AV20				
FMCA_LA_TX_N16	AU20				
FMCA_LA_RX_P7	AU21				
FMCA_LA_RX_N7	AV21				
FMCA_LA_TX_P13	AT19				
FMCA_LA_TX_N13	AT20				
FMCA_LA_RX_P11	AP21				
FMCA_LA_RX_N11	AR21				
FMCA_LA_RX_P2	AP18				
FMCA_LA_RX_N2	AN19				
FMCA_LA_RX_P0	AR20				
FMCA_LA_RX_N0	AR19				
FMCA_LA_TX_P0	AR22				
FMCA_LA_TX_N0	AT22				
FMCA_LA_TX_P1	AN20				
FMCA_LA_TX_N1	AP19				

10AX115F1932C

AU10	FMCA_SCL		
AV10	FMCA_SDA		
AU11	FMCA_LA_TX_P9		
AU12	FMCA_LA_TX_N9		
AW13	FMCA_LA_TX_P4		
AV13	FMCA_LA_TX_N4		
AV11	FMCA_LA_TX_P2		
AW11	FMCA_LA_TX_N2		
AY10	FMCA_LA_TX_P10		
AY11	FMCA_LA_TX_N10		
AW12	FMCA_LA_RX_P9		
AY12	FMCA_LA_RX_N9		
AR9	FMCA_LA_TX_P7		
AT9	FMCA_LA_TX_N7		
AT13	FMCA_LA_RX_P6		
AU13	FMCA_LA_RX_N6		
AU8	FMCA_LA_RX_P8		
AT8	FMCA_LA_RX_N8		
AP14	RZQ_B3C	R352	100, 1%
AP13			
BD13			
BD12			
BC14			
BD14			
BC13			
BB13			
BB12			
BB11			
BC16	FMCA_GA0		
BB16			
BD17			
BD16	FMCA_GA1		
BA15	FMCA_LA_RX_P12		
BA14	FMCA_LA_RX_N12		
BC18	FMCA_LA_TX_P15		
BD18	FMCA_LA_TX_N15		
BB17	FMCA_LA_RX_P13		
BB18	FMCA_LA_RX_N13		
BB15	FMCA_LA_TX_P12		
BC15	FMCA_LA_TX_N12		
AJ11	USB_DATA0		
AK12	USB_DATA1		
AL12	FM_A3		
AL13	FM_A11		
AK14	FM_A25		
AJ14	FM_A20		
AH10	FM_A15		
AH11	FM_A12		
AJ12	FM_A19		
AJ13	FM_A23		
AH13	FM_A21		
AH14	FM_A18		
AF12	FM_A24		
AE12	FM_A6		
AG12	FM_A22		
AG11	FM_A14		
AF14	FM_A16		
AF15	FM_A17		
AE14	USB_RESETn		
AE15	USB_WRn		
AL15	USB_OEn		
AK15	USB_RDn		
AL19	USB_DATA6		
AL20	USB_DATA7		
AM17	USB_DATA4		
AL17	USB_DATA5		
AM15	USB_ADDR0		
AL14	USB_ADDR1		
AN11	USB_DATA2		
AN10	USB_DATA3		
AL10	FM_A8		
AK11	FM_A26		
AN13	FM_A4		
AM13	FM_A5		
AP11	FM_A10		
AR10	FM_A9		
AM12	FM_A2		
AM11	FM_A1		
AN15	FM_A7		
AN14	FM_A13		

FLASH/FM BUS

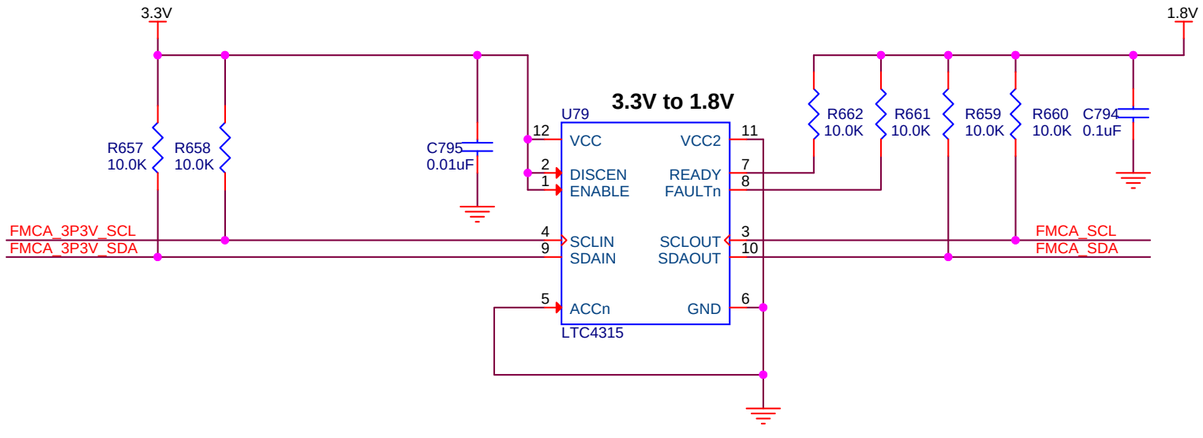
13,14 FM_D[31:0]
13,14 FM_A[26:1]
13,14 FLASH_CLK
13,14 FLASH_RESETn
13,14 FLASH_CEn0
13,14 FLASH_CEn1
13,14 FLASH_OEn
13,14 FLASH_WEn
13,14 FLASH_ADVn
13,14 FLASH_RDYBSYn0

FMC PORT A INTERFACE

19 FMCA_LA_RX_P[14:0]
19 FMCA_LA_RX_N[14:0]
19 FMCA_LA_TX_P[16:0]
19 FMCA_LA_TX_N[16:0]
19 FMCA_GA[1:0]
19 FMCA_3P3V_SDA
19 FMCA_3P3V_SCL

ARRIA 10 USB INTERFACE

26 USB_DATA[7:0]
26 USB_ADDR[1:0]
26 USB_RESETn
26 USB_OEn
26 USB_RDn
26 USB_WRn



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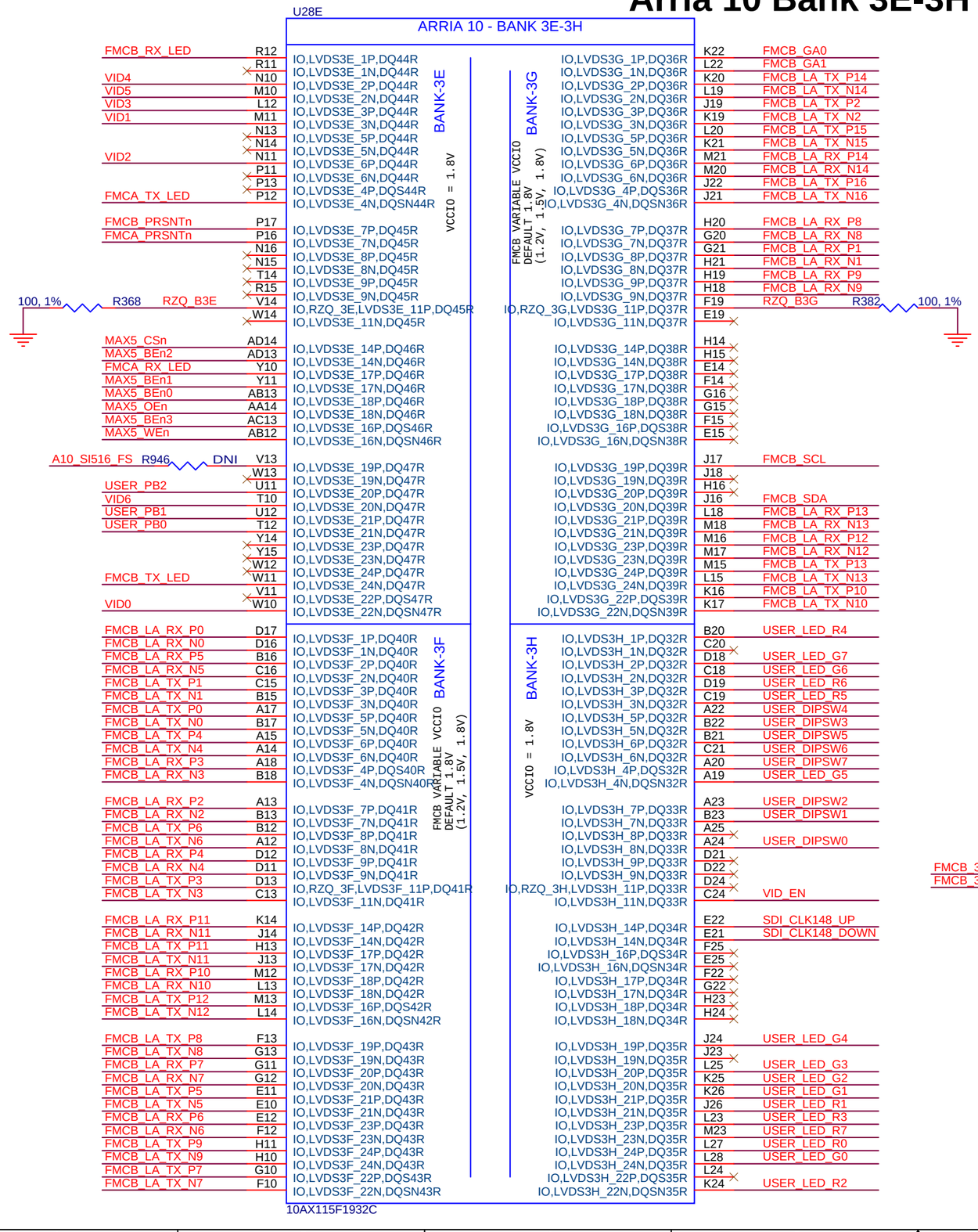
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 5 of 49

Arria 10 Bank 3E-3H



USER IO INTERFACE

24 USER_DIPSW[7:0]
24 USER_LED_G[7:0]
24 USER_LED_R[7:0]
24 USER_PB[2:0]
35 VID[6:0]
7,35 VID_EN
9 A10_SI516_FS

MAX V INTERFACE

13 MAX5_BEn[3:0]
13 MAX5_OEn
13 MAX5_CSn
13 MAX5_WEn

FMC PORT A INTERFACE

13,19,24,26 FMCA_PRSNTn

FMC PORT B INTERFACE

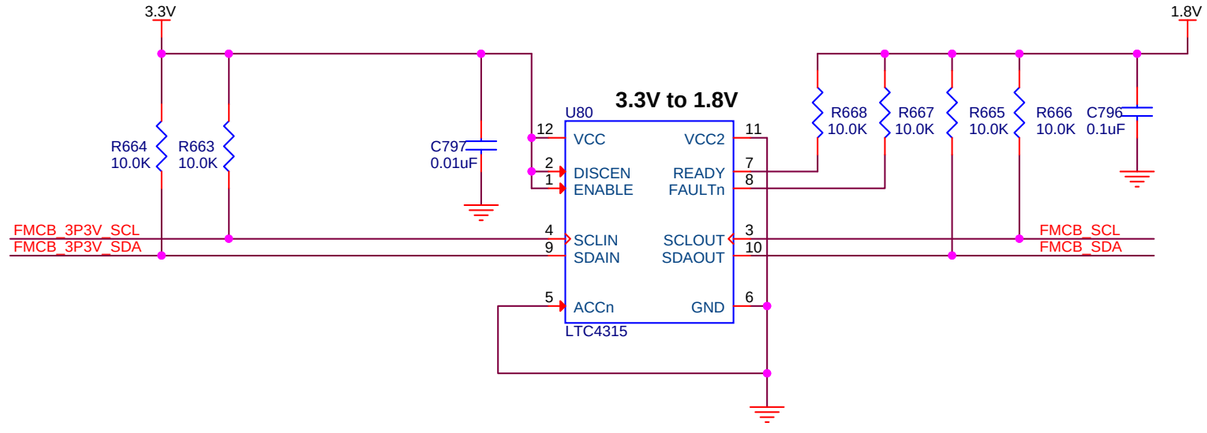
20 FMCB_LA_RX_P[14:0]
20 FMCB_LA_RX_N[14:0]
20 FMCB_LA_TX_P[16:0]
20 FMCB_LA_TX_N[16:0]
20 FMCB_GA[1:0]
13,20,24,26 FMCB_PRSNTn
20 FMCB_3P3V_SDA
20 FMCB_3P3V_SCL

USER I/O INTERFACE

24 FMCA_RX_LED
24 FMCA_TX_LED
24 FMCB_RX_LED
24 FMCB_TX_LED

ARRIA 10 CLOCKS

9 SDI_CLK148_UP
9 SDI_CLK148_DOWN



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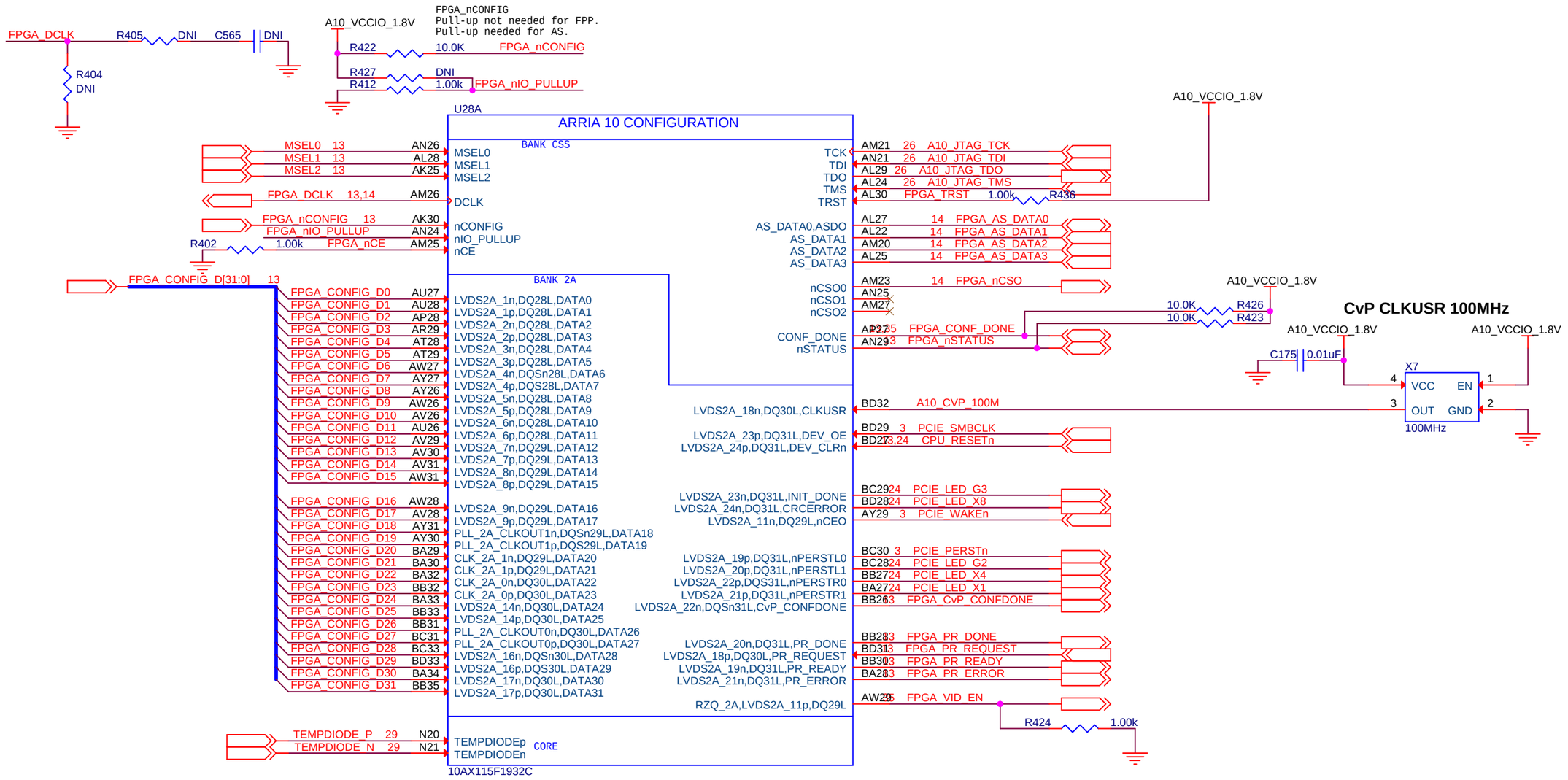
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 6 of 49

Arria 10 Configuration



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Date: Thursday, May 28, 2015 Sheet 7 of 49

Arria 10 Clocks

U28B

ARRIA 10 CONFIGURATION

BANK-2I

VCCIO = 1.8V

CLK_50	AU33	CLK_2I_0P,DQ14L	PLL_2I_CLKOUT0P,DQ14L	AT32	
	AT33	CLK_2I_0N,DQ14L	PLL_2I_CLKOUT0N,DQ14L	AU32	
R450 100, 1% CLK_FPGA_B2_P	AR36	CLK_2I_1P,DQ13L	PLL_2I_CLKOUT1P,DQS13L	AN33	
CLK_FPGA_B2_N	AR37	CLK_2I_1N,DQ13L	PLL_2I_CLKOUT1N,DQSn13L	AM33	

CAN BE REMOVED FOR ARRIA 10 AND USE OCT ->

BANK-2J

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

MEM_DQB16	U31	CLK_2J_0P,DQ10L	PLL_2J_CLKOUT0P,DQ10L	W34	MEM_DQB22
MEM_DQB19	V31	CLK_2J_0N,DQ10L	PLL_2J_CLKOUT0N,DQ10L	Y34	MEM_DQB20
MEM_DMB1	AG31	CLK_2J_1P,DQ9L	PLL_2J_CLKOUT1P,DQS9L	AJ32	MEM_DQSB_P1
MEM_DQB15	AH31	CLK_2J_1N,DQ9L	PLL_2J_CLKOUT1N,DQSn9L	AJ31	MEM_DQSB_N1

BANK-2K

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

MEM_ADDR_CMD10	H31	CLK_2K_0P,DQ6L	PLL_2K_CLKOUT0P,DQ6L	M33	MEM_ADDR_CMD6
MEM_ADDR_CMD11	J31	CLK_2K_0N,DQ6L	PLL_2K_CLKOUT0N,DQ6L	L33	MEM_ADDR_CMD7
R448 100, 1% CLK_EMI_P	F34	CLK_2K_1P,DQ5L	PLL_2K_CLKOUT1P,DQS5L	H33	MEM_ADDR_CMD13
CLK_EMI_N	F35	CLK_2K_1N,DQ5L	PLL_2K_CLKOUT1N,DQSn5L	G32	MEM_ADDR_CMD14

BANK-2L

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

MEM_DQA20	A30	CLK_2L_0P,DQ2L	PLL_2L_CLKOUT0P,DQ2L	B31	MEM_DQA18
MEM_DMA2	A29	CLK_2L_0N,DQ2L	PLL_2L_CLKOUT0N,DQ2L	B30	MEM_DQA22
MEM_DQA10	G26	CLK_2L_1P,DQ1L	PLL_2L_CLKOUT1P,DQS1L	H28	MEM_DQSA_P1
MEM_DQA11	H26	CLK_2L_1N,DQ1L	PLL_2L_CLKOUT1N,DQSn1L	J27	MEM_DQSA_N1

BANK-3A

VCCIO = 1.8V

R403 100, 1% CLK_125_P	BD24	CLK_3A_0P,DQ62R	PLL_3A_CLKOUT0P,DQ62R	BC23	ENET_TX_P
CAN BE REMOVED FOR ARRIA 10 AND USE OCT -> CLK_125_N	BC24	CLK_3A_0N,DQ62R	PLL_3A_CLKOUT0N,DQ62R	BD23	ENET_TX_N
R406 100, 1% ENET_RX_P	AV24	CLK_3A_1P,DQ61R	PLL_3A_CLKOUT1P,DQS61R	AW23	ENET_RESETn
CAN BE REMOVED FOR ARRIA 10 AND USE OCT -> ENET_RX_N	AW24	CLK_3A_1N,DQ61R	PLL_3A_CLKOUT1N,DQSn61R	AV23	FLASH_RDYBSYn1

BANK-3B

FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R383 100, 1% FMCA_CLK_M2C_P0	AY20	CLK_3B_0P,DQ58R	PLL_3B_CLKOUT0P,DQ58R	AW21	
FMCA_CLK_M2C_N0	AY19	CLK_3B_0N,DQ58R	PLL_3B_CLKOUT0N,DQ58R	AY21	
R369 100, 1% FMCA_LA_RX_CLK_P0	AV15	CLK_3B_1P,DQ57R	PLL_3B_CLKOUT1P,DQS57R	AV16	
FMCA_LA_RX_CLK_N0	AU15	CLK_3B_1N,DQ57R	PLL_3B_CLKOUT1N,DQSn57R	AU16	

BANK-3C

FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R353 100, 1% FMCA_CLK_M2C_P1	BA12	CLK_3C_0P,DQ54R	PLL_3C_CLKOUT0P,DQ54R	BB10	
FMCA_CLK_M2C_N1	BA13	CLK_3C_0N,DQ54R	PLL_3C_CLKOUT0N,DQ54R	BA10	
R336 100, 1% FMCA_LA_RX_CLK_P1	AT10	CLK_3C_1P,DQ53R	PLL_3C_CLKOUT1P,DQS53R	AP12	
FMCA_LA_RX_CLK_N1	AR11	CLK_3C_1N,DQ53R	PLL_3C_CLKOUT1N,DQSn53R	AR12	

BANK-3D

VCCIO = 1.8V

USB_FPGA_CLK	AM18	CLK_3D_0P,DQ50R	PLL_3D_CLKOUT0P,DQ50R	AM16	USB_FULL
ENET_MDIO	AL18	CLK_3D_0N,DQ50R	PLL_3D_CLKOUT0N,DQ50R	AN16	USB_EMPTY
ENET_MDC	AF13	CLK_3D_1P,DQ49R	PLL_3D_CLKOUT1P,DQS49R	AE11	USB_SCL
ENET_INTn	AG13	CLK_3D_1N,DQ49R	PLL_3D_CLKOUT1N,DQSn49R	AD12	USB_SDA

BANK-3E

VCCIO = 1.8V

MAX5_CLK	AB11	CLK_3E_0P,DQ46R	PLL_3E_CLKOUT0P,DQ46R	AA13	S5_MSEL4
S5_MSEL3	AC11	CLK_3E_0N,DQ46R	PLL_3E_CLKOUT0N,DQ46R	Y12	STRATIX V MSEL PINS.
R14		CLK_3E_1P,DQ45R	PLL_3E_CLKOUT1P,DQS45R	U13	CAN BE DELETED IN REV B
P14		CLK_3E_1N,DQ45R	PLL_3E_CLKOUT1N,DQSn45R	T13	

BANK-3F

FMCB VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R349 100, 1% FMCB_CLK_M2C_P0	J12	CLK_3F_0P,DQ42R	PLL_3F_CLKOUT0P,DQ42R	K11	
FMCB_CLK_M2C_N0	K12	CLK_3F_0N,DQ42R	PLL_3F_CLKOUT0N,DQ42R	J11	
R333 100, 1% FMCB_LA_RX_CLK_P0	C11	CLK_3F_1P,DQ41R	PLL_3F_CLKOUT1P,DQS41R	C14	
FMCB_LA_RX_CLK_N0	C10	CLK_3F_1N,DQ41R	PLL_3F_CLKOUT1N,DQSn41R	D14	

BANK-3G

FMCB VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R378 100, 1% FMCB_CLK_M2C_P1	F17	CLK_3G_0P,DQ38R	PLL_3G_CLKOUT0P,DQ38R	E16	
FMCB_CLK_M2C_N1	G17	CLK_3G_0N,DQ38R	PLL_3G_CLKOUT0N,DQ38R	E17	
R379 100, 1% FMCB_LA_RX_CLK_P1	G18	CLK_3G_1P,DQ37R	PLL_3G_CLKOUT1P,DQS37R	E20	
FMCB_LA_RX_CLK_N1	F18	CLK_3G_1N,DQ37R	PLL_3G_CLKOUT1N,DQSn37R	F20	

BANK-3H

VCCIO = 1.8V

R391 100, 1% CLK_FPGA_B3_P	F23	CLK_3H_0P,DQ34R	PLL_3H_CLKOUT0P,DQ34R	E24	SMA_CLK_OUT
CAN BE REMOVED FOR ARRIA 10 AND USE OCT -> CLK_FPGA_B3_N	G23	CLK_3H_0N,DQ34R	PLL_3H_CLKOUT0N,DQ34R	F24	
C23		CLK_3H_1P,DQ33R	PLL_3H_CLKOUT1P,DQS33R	C25	
D23		CLK_3H_1N,DQ33R	PLL_3H_CLKOUT1N,DQSn33R	B25	

10AX115F1932C

A10_VCCIO_1.8V

S5_MSEL3 — R305 DNI / R307 1.00k

R306 1.00k / R308 DNI

1 J7 2 3 4 5

ETHERNET INTERFACE

15 ENET_RX_P
15 ENET_RX_N
15 ENET_TX_P
15 ENET_TX_N
15 ENET_RESETn
15 ENET_MDIO
15 ENET_MDC
15 ENET_INTn

MEMORY INTERFACE

4,17 MEM_ADDR_CMD[31:0]
4,17 MEM_DMA[3:0]
4,17 MEM_DQA[33:0]
4,17 MEM_DQSA_P[3:0]
4,17 MEM_DQSA_N[3:0]
4,17 MEM_DMB[3:0]
4,17 MEM_DQB[33:0]
4,17 MEM_DQSB_P[3:0]
4,17 MEM_DQSB_N[3:0]

ARRIA 10 CLOCKS

9 CLK_50
9 CLK_125_P
9 CLK_125_N
9 CLK_FPGA_B2_P
9 CLK_FPGA_B2_N
9 CLK_FPGA_B3_P
9 CLK_FPGA_B3_N
10 CLK_EMI_P
10 CLK_EMI_N

FLASH INTERFACE

13,14 FLASH_RDYBSYn1

FMC PORT A INTERFACE

19 FMCA_CLK_M2C_P[1:0]
19 FMCA_CLK_M2C_N[1:0]
19 FMCA_LA_RX_CLK_P[1:0]
19 FMCA_LA_RX_CLK_N[1:0]

FMC PORT B INTERFACE

20 FMCB_CLK_M2C_P[1:0]
20 FMCB_CLK_M2C_N[1:0]
20 FMCB_LA_RX_CLK_P[1:0]
20 FMCB_LA_RX_CLK_N[1:0]

ARRIA 10 USB INTERFACE

25 USB_FPGA_CLK
26 USB_FULL
26 USB_EMPTY
26 USB_SCL
26 USB_SDA

MAX V INTERFACE

13 MAX5_CLK

Title: Arria 10 GX FPGA Development Kit

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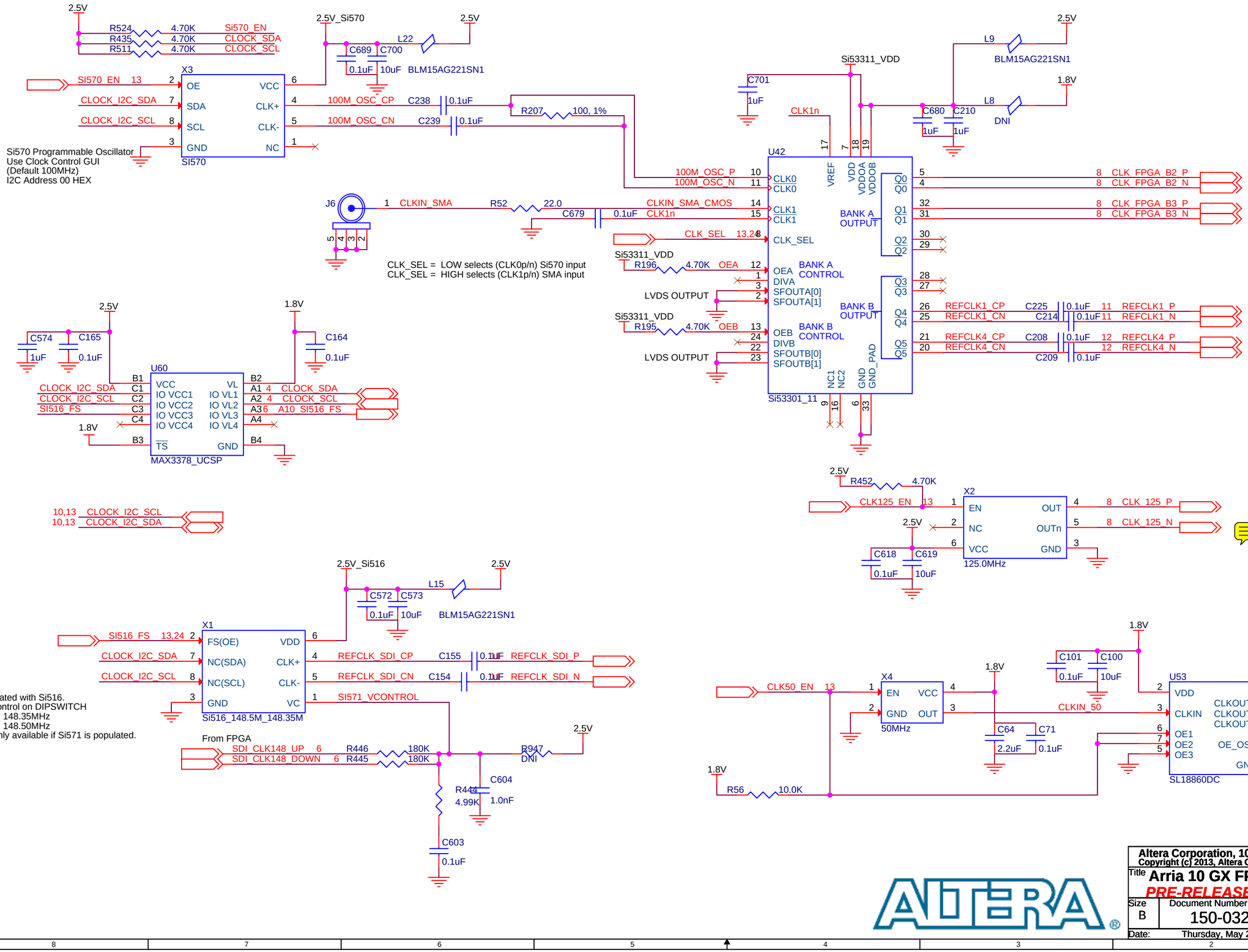
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 8 of 49

Clocks



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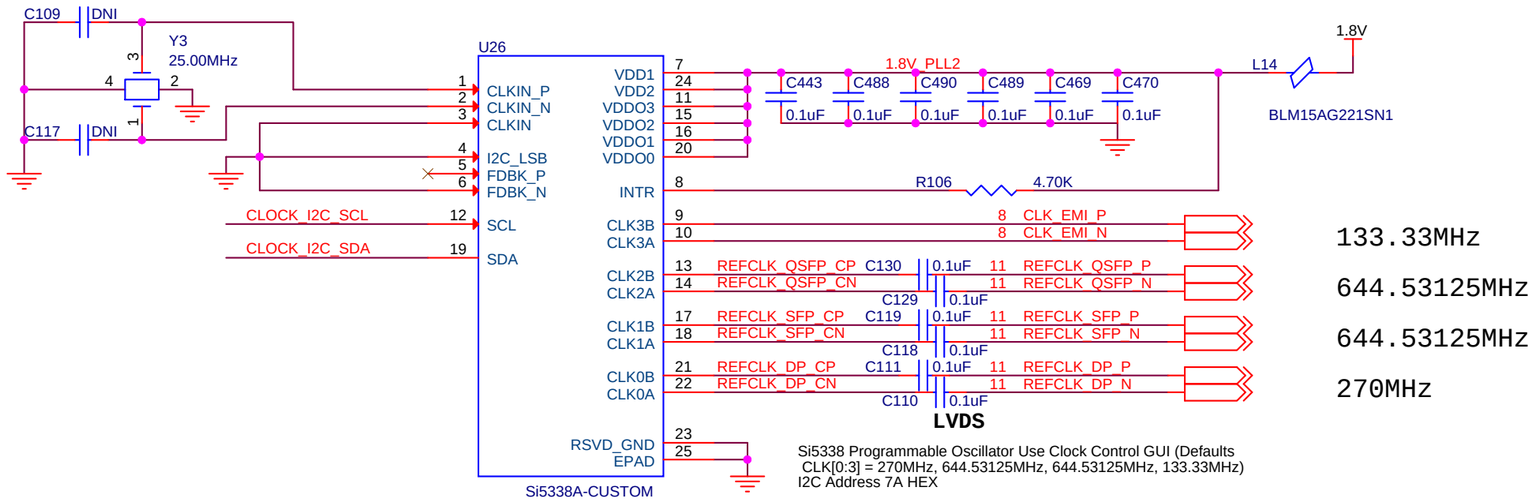
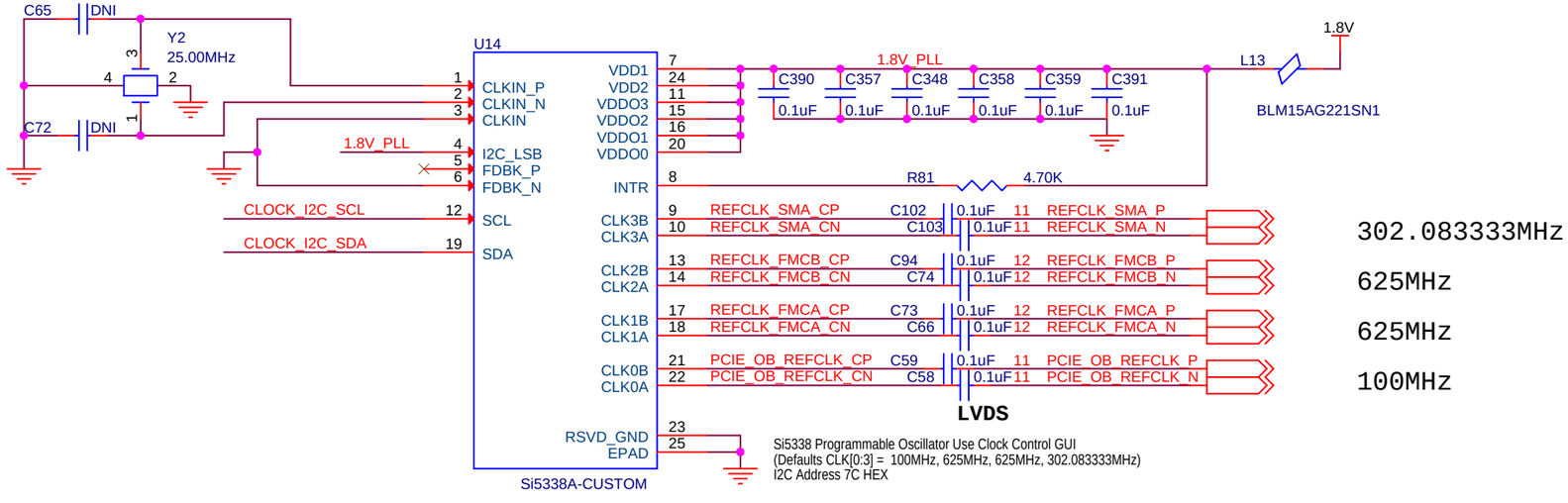
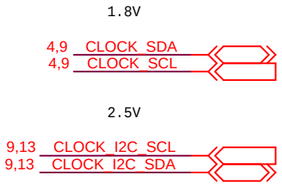
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 9 of 49

PLL (2)







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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 10 of 49

Arria 10 Transceivers Left

U28F — ARRIA 10 - LEFT TRANSCEIVER BANK-1C

AW38	GXBL1C_RX_CH0P,GXBL1C_REFCLK0P	GXBL1C_TX_CH0P	BC38
AW37	GXBL1C_RX_CH0N,GXBL1C_REFCLK0N	GXBL1C_TX_CH0N	BC37
BA38	GXBL1C_RX_CH1P,GXBL1C_REFCLK1P	GXBL1C_TX_CH1P	BD40
BA37	GXBL1C_RX_CH1N,GXBL1C_REFCLK1N	GXBL1C_TX_CH1N	BD39
AY40	GXBL1C_RX_CH2P,GXBL1C_REFCLK2P	GXBL1C_TX_CH2P	BB40
AY39	GXBL1C_RX_CH2N,GXBL1C_REFCLK2N	GXBL1C_TX_CH2N	BB39
AV40	GXBL1C_RX_CH3P,GXBL1C_REFCLK3P	GXBL1C_TX_CH3P	BC42
AV39	GXBL1C_RX_CH3N,GXBL1C_REFCLK3N	GXBL1C_TX_CH3N	BC41
PCIE_RX_P0 AT40	GXBL1C_RX_CH4P,GXBL1C_REFCLK4P	GXBL1C_TX_CH4P	BB44 PCIE_TX_P0
PCIE_RX_N0 AT39	GXBL1C_RX_CH4N,GXBL1C_REFCLK4N	GXBL1C_TX_CH4N	BB43 PCIE_TX_N0
PCIE_RX_P1 AP40	GXBL1C_RX_CH5P,GXBL1C_REFCLK5P	GXBL1C_TX_CH5P	BA42 PCIE_TX_P1
PCIE_RX_N1 AP39	GXBL1C_RX_CH5N,GXBL1C_REFCLK5N	GXBL1C_TX_CH5N	BA41 PCIE_TX_N1
PCIE_EDGE_REFCLK_P AL37	REFCLK_GXBL1C_CHTP		
PCIE_EDGE_REFCLK_N AL38	REFCLK_GXBL1C_CHTN		
PCIE_OB_REFCLK_P AN37	REFCLK_GXBL1C_CHBP		
PCIE_OB_REFCLK_N AN38	REFCLK_GXBL1C_CHBN		

10AX115F1932C

U28G — ARRIA 10 - LEFT TRANSCEIVER BANK-1D

PCIE_RX_P2 AN42	GXBL1D_RX_CH0P,GXBL1D_REFCLK0P	GXBL1D_TX_CH0P	AY44 PCIE_TX_P2
PCIE_RX_N2 AN41	GXBL1D_RX_CH0N,GXBL1D_REFCLK0N	GXBL1D_TX_CH0N	AY43 PCIE_TX_N2
PCIE_RX_P3 AM40	GXBL1D_RX_CH1P,GXBL1D_REFCLK1P	GXBL1D_TX_CH1P	AW42 PCIE_TX_P3
PCIE_RX_N3 AM39	GXBL1D_RX_CH1N,GXBL1D_REFCLK1N	GXBL1D_TX_CH1N	AW41 PCIE_TX_N3
PCIE_RX_P4 AL42	GXBL1D_RX_CH2P,GXBL1D_REFCLK2P	GXBL1D_TX_CH2P	AV44 PCIE_TX_P4
PCIE_RX_N4 AL41	GXBL1D_RX_CH2N,GXBL1D_REFCLK2N	GXBL1D_TX_CH2N	AV43 PCIE_TX_N4
PCIE_RX_P5 AK40	GXBL1D_RX_CH3P,GXBL1D_REFCLK3P	GXBL1D_TX_CH3P	AU42 PCIE_TX_P5
PCIE_RX_N5 AK39	GXBL1D_RX_CH3N,GXBL1D_REFCLK3N	GXBL1D_TX_CH3N	AU41 PCIE_TX_N5
PCIE_RX_P6 AJ42	GXBL1D_RX_CH4P,GXBL1D_REFCLK4P	GXBL1D_TX_CH4P	AT44 PCIE_TX_P6
PCIE_RX_N6 AJ41	GXBL1D_RX_CH4N,GXBL1D_REFCLK4N	GXBL1D_TX_CH4N	AT43 PCIE_TX_N6
PCIE_RX_P7 AH40	GXBL1D_RX_CH5P,GXBL1D_REFCLK5P	GXBL1D_TX_CH5P	AR42 PCIE_TX_P7
PCIE_RX_N7 AH39	GXBL1D_RX_CH5N,GXBL1D_REFCLK5N	GXBL1D_TX_CH5N	AR41 PCIE_TX_N7
REFCLK1_P AG37	REFCLK_GXBL1D_CHTP		
REFCLK1_N AG38	REFCLK_GXBL1D_CHTN		
10.0K R464 AJ37	REFCLK_GXBL1D_CHBP		
AJ38	REFCLK_GXBL1D_CHBN		

10AX115F1932C

U28H — ARRIA 10 - LEFT TRANSCEIVER BANK-1E

AG42	GXBL1E_RX_CH0P,GXBL1E_REFCLK0P	GXBL1E_TX_CH0P	AP44 DP_ML_LANE_P0
AG41	GXBL1E_RX_CH0N,GXBL1E_REFCLK0N	GXBL1E_TX_CH0N	AP43 DP_ML_LANE_N0
AF40	GXBL1E_RX_CH1P,GXBL1E_REFCLK1P	GXBL1E_TX_CH1P	AM44 DP_ML_LANE_P1
AF39	GXBL1E_RX_CH1N,GXBL1E_REFCLK1N	GXBL1E_TX_CH1N	AM43 DP_ML_LANE_N1
AE42	GXBL1E_RX_CH2P,GXBL1E_REFCLK2P	GXBL1E_TX_CH2P	AK44
AE41	GXBL1E_RX_CH2N,GXBL1E_REFCLK2N	GXBL1E_TX_CH2N	AK43
AD40	GXBL1E_RX_CH3P,GXBL1E_REFCLK3P	GXBL1E_TX_CH3P	AH44 DP_ML_LANE_P2
AD39	GXBL1E_RX_CH3N,GXBL1E_REFCLK3N	GXBL1E_TX_CH3N	AH43 DP_ML_LANE_N2
AC42	GXBL1E_RX_CH4P,GXBL1E_REFCLK4P	GXBL1E_TX_CH4P	AF44 DP_ML_LANE_P3
AC41	GXBL1E_RX_CH4N,GXBL1E_REFCLK4N	GXBL1E_TX_CH4N	AF43 DP_ML_LANE_N3
AB40	GXBL1E_RX_CH5P,GXBL1E_REFCLK5P	GXBL1E_TX_CH5P	AD44
AB39	GXBL1E_RX_CH5N,GXBL1E_REFCLK5N	GXBL1E_TX_CH5N	AD43
REFCLK_DP_P AC37	REFCLK_GXBL1E_CHTP		
REFCLK_DP_N AC38	REFCLK_GXBL1E_CHTN		
10.0K R463 AE37	REFCLK_GXBL1E_CHBP		
AE38	REFCLK_GXBL1E_CHBN		

10AX115F1932C

U28I — ARRIA 10 - LEFT TRANSCEIVER BANK-1F

SFP_RX_P AA42	GXBL1F_RX_CH0P,GXBL1F_REFCLK0P	GXBL1F_TX_CH0P	AB44 SFP_TX_P
SFP_RX_N AA41	GXBL1F_RX_CH0N,GXBL1F_REFCLK0N	GXBL1F_TX_CH0N	AB43 SFP_TX_N
W42	GXBL1F_RX_CH1P,GXBL1F_REFCLK1P	GXBL1F_TX_CH1P	Y44
W41	GXBL1F_RX_CH1N,GXBL1F_REFCLK1N	GXBL1F_TX_CH1N	Y43
Y40	GXBL1F_RX_CH2P,GXBL1F_REFCLK2P	GXBL1F_TX_CH2P	V44
Y39	GXBL1F_RX_CH2N,GXBL1F_REFCLK2N	GXBL1F_TX_CH2N	V43
V40	GXBL1F_RX_CH3P,GXBL1F_REFCLK3P	GXBL1F_TX_CH3P	T44
V39	GXBL1F_RX_CH3N,GXBL1F_REFCLK3N	GXBL1F_TX_CH3N	T43
U42	GXBL1F_RX_CH4P,GXBL1F_REFCLK4P	GXBL1F_TX_CH4P	P44
U41	GXBL1F_RX_CH4N,GXBL1F_REFCLK4N	GXBL1F_TX_CH4N	P43
T40	GXBL1F_RX_CH5P,GXBL1F_REFCLK5P	GXBL1F_TX_CH5P	M44
T39	GXBL1F_RX_CH5N,GXBL1F_REFCLK5N	GXBL1F_TX_CH5N	M43
W37	REFCLK_GXBL1F_CHTP		
10.0K R462 W38	REFCLK_GXBL1F_CHTN		
REFCLK_SFP_P AA37	REFCLK_GXBL1F_CHBP		
REFCLK_SFP_N AA38	REFCLK_GXBL1F_CHBN		

10AX115F1932C

U28J — ARRIA 10 - LEFT TRANSCEIVER BANK-1G

QSFP_RX_P0 R42	GXBL1G_RX_CH0P,GXBL1G_REFCLK0P	GXBL1G_TX_CH0P	K44 QSFP_TX_P0
QSFP_RX_N0 R41	GXBL1G_RX_CH0N,GXBL1G_REFCLK0N	GXBL1G_TX_CH0N	K43 QSFP_TX_N0
QSFP_RX_P1 P40	GXBL1G_RX_CH1P,GXBL1G_REFCLK1P	GXBL1G_TX_CH1P	J42 QSFP_TX_P1
QSFP_RX_N1 P39	GXBL1G_RX_CH1N,GXBL1G_REFCLK1N	GXBL1G_TX_CH1N	J41 QSFP_TX_N1
N42	GXBL1G_RX_CH2P,GXBL1G_REFCLK2P	GXBL1G_TX_CH2P	H44
N41	GXBL1G_RX_CH2N,GXBL1G_REFCLK2N	GXBL1G_TX_CH2N	H43
QSFP_RX_P2 M40	GXBL1G_RX_CH3P,GXBL1G_REFCLK3P	GXBL1G_TX_CH3P	G42 QSFP_TX_P2
QSFP_RX_N2 M39	GXBL1G_RX_CH3N,GXBL1G_REFCLK3N	GXBL1G_TX_CH3N	G41 QSFP_TX_N2
QSFP_RX_P3 L42	GXBL1G_RX_CH4P,GXBL1G_REFCLK4P	GXBL1G_TX_CH4P	F44 QSFP_TX_P3
QSFP_RX_N3 L41	GXBL1G_RX_CH4N,GXBL1G_REFCLK4N	GXBL1G_TX_CH4N	F43 QSFP_TX_N3
K40	GXBL1G_RX_CH5P,GXBL1G_REFCLK5P	GXBL1G_TX_CH5P	E42
K39	GXBL1G_RX_CH5N,GXBL1G_REFCLK5N	GXBL1G_TX_CH5N	E41
REFCLK_QSFP_P R37	REFCLK_GXBL1G_CHTP		
REFCLK_QSFP_N R38	REFCLK_GXBL1G_CHTN		
10.0K R461 U37	REFCLK_GXBL1G_CHBP		
U38	REFCLK_GXBL1G_CHBN		

10AX115F1932C

U28K — ARRIA 10 - LEFT TRANSCEIVER BANK-1H

SDI_RX_P H40	GXBL1H_RX_CH0P,GXBL1H_REFCLK0P	GXBL1H_TX_CH0P	D44 SDI_TX_P
SDI_RX_N H39	GXBL1H_RX_CH0N,GXBL1H_REFCLK0N	GXBL1H_TX_CH0N	D43 SDI_TX_N
G38	GXBL1H_RX_CH1P,GXBL1H_REFCLK1P	GXBL1H_TX_CH1P	C42 SMA_TX_P
G37	GXBL1H_RX_CH1N,GXBL1H_REFCLK1N	GXBL1H_TX_CH1N	C41 SMA_TX_N
F40	GXBL1H_RX_CH2P,GXBL1H_REFCLK2P	GXBL1H_TX_CH2P	B44
F39	GXBL1H_RX_CH2N,GXBL1H_REFCLK2N	GXBL1H_TX_CH2N	B43
E38	GXBL1H_RX_CH3P,GXBL1H_REFCLK3P	GXBL1H_TX_CH3P	A42
E37	GXBL1H_RX_CH3N,GXBL1H_REFCLK3N	GXBL1H_TX_CH3N	A41
D40	GXBL1H_RX_CH4P,GXBL1H_REFCLK4P	GXBL1H_TX_CH4P	B40
D39	GXBL1H_RX_CH4N,GXBL1H_REFCLK4N	GXBL1H_TX_CH4N	B39
C38	GXBL1H_RX_CH5P,GXBL1H_REFCLK5P	GXBL1H_TX_CH5P	A38
C37	GXBL1H_RX_CH5N,GXBL1H_REFCLK5N	GXBL1H_TX_CH5N	A37
REFCLK_SDI_P L37	REFCLK_GXBL1H_CHTP		
REFCLK_SDI_N L38	REFCLK_GXBL1H_CHTN		
REFCLK_SMA_P N37	REFCLK_GXBL1H_CHBP		
REFCLK_SMA_N N38	REFCLK_GXBL1H_CHBN		

10AX115F1932C

J16, J15

Connectors

- REFCLK1_P, REFCLK1_N
- **PCIe INTERFACE**: PCIE_RX_P[7:0], PCIE_RX_N[7:0], PCIE_TX_P[7:0], PCIE_TX_N[7:0], PCIE_EDGE_REFCLK_P, PCIE_EDGE_REFCLK_N, PCIE_OB_REFCLK_P, PCIE_OB_REFCLK_N
- **DISPLAYPORT INTERFACE**: DP_ML_LANE_P[3:0], DP_ML_LANE_N[3:0], REFCLK_DP_P, REFCLK_DP_N
- **SDI INTERFACE**: REFCLK_SDI_P, REFCLK_SDI_N, SDI_RX_P, SDI_RX_N, SDI_TX_P, SDI_TX_N
- **QSFP INTERFACE**: QSFP_RX_P[3:0], QSFP_RX_N[3:0], QSFP_TX_P[3:0], QSFP_TX_N[3:0], REFCLK_QSFP_P, REFCLK_QSFP_N
- **SFP+ INTERFACE**: SFP_RX_P, SFP_RX_N, SFP_TX_P, SFP_TX_N, REFCLK_SFP_P, REFCLK_SFP_N
- **SMA INTERFACE**: REFCLK_SMA_P, REFCLK_SMA_N

Title: **Arria 10 GX FPGA Development Kit**

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 11 of 49

Arria 10 Transceivers Right

U28L — ARRIA 10 - RIGHT TRANSCEIVER BANK-4C

FMCA_DP_M2C_P0	AW7	GXBR4C_RX_CH0P, GXBR4C_REFCLK0P	GXBR4C_TX_CH0P	BC7	FMCA_DP_C2M_P0
FMCA_DP_M2C_N0	AW8	GXBR4C_RX_CH0N, GXBR4C_REFCLK0N	GXBR4C_TX_CH0N	BC8	FMCA_DP_C2M_N0
FMCA_DP_M2C_P1	BA7	GXBR4C_RX_CH1P, GXBR4C_REFCLK1P	GXBR4C_TX_CH1P	BD5	FMCA_DP_C2M_P1
FMCA_DP_M2C_N1	BA8	GXBR4C_RX_CH1N, GXBR4C_REFCLK1N	GXBR4C_TX_CH1N	BD6	FMCA_DP_C2M_N1
FMCA_DP_M2C_P2	AY5	GXBR4C_RX_CH2P, GXBR4C_REFCLK2P	GXBR4C_TX_CH2P	BB5	FMCA_DP_C2M_P2
FMCA_DP_M2C_N2	AY6	GXBR4C_RX_CH2N, GXBR4C_REFCLK2N	GXBR4C_TX_CH2N	BB6	FMCA_DP_C2M_N2
FMCA_DP_M2C_P3	AV5	GXBR4C_RX_CH3P, GXBR4C_REFCLK3P	GXBR4C_TX_CH3P	BC3	FMCA_DP_C2M_P3
FMCA_DP_M2C_N3	AV6	GXBR4C_RX_CH3N, GXBR4C_REFCLK3N	GXBR4C_TX_CH3N	BC4	FMCA_DP_C2M_N3
FMCA_DP_M2C_P4	AT5	GXBR4C_RX_CH4P, GXBR4C_REFCLK4P	GXBR4C_TX_CH4P	BB1	FMCA_DP_C2M_P4
FMCA_DP_M2C_N4	AT6	GXBR4C_RX_CH4N, GXBR4C_REFCLK4N	GXBR4C_TX_CH4N	BB2	FMCA_DP_C2M_N4
FMCA_DP_M2C_P5	AP5	GXBR4C_RX_CH5P, GXBR4C_REFCLK5P	GXBR4C_TX_CH5P	BA3	FMCA_DP_C2M_P5
FMCA_DP_M2C_N5	AP6	GXBR4C_RX_CH5N, GXBR4C_REFCLK5N	GXBR4C_TX_CH5N	BA4	FMCA_DP_C2M_N5
FMCA_GBTCLK_M2C_P0	AL8	REFCLK_GXBR4C_CHTP			
FMCA_GBTCLK_M2C_N0	AL7	REFCLK_GXBR4C_CHTN			
REFCLK_FMCA_P	AN8	REFCLK_GXBR4C_CHBP			
REFCLK_FMCA_N	AN7	REFCLK_GXBR4C_CHBN			

10AX115F1932C

U28O — ARRIA 10 - RIGHT TRANSCEIVER BANK-4F

FMCB_DP_M2C_P0	AA3	GXBR4F_RX_CH0P, GXBR4F_REFCLK0P	GXBR4F_TX_CH0P	AB1	FMCB_DP_C2M_P0
FMCB_DP_M2C_N0	AA4	GXBR4F_RX_CH0N, GXBR4F_REFCLK0N	GXBR4F_TX_CH0N	AB2	FMCB_DP_C2M_N0
FMCB_DP_M2C_P1	W3	GXBR4F_RX_CH1P, GXBR4F_REFCLK1P	GXBR4F_TX_CH1P	Y1	FMCB_DP_C2M_P1
FMCB_DP_M2C_N1	W4	GXBR4F_RX_CH1N, GXBR4F_REFCLK1N	GXBR4F_TX_CH1N	Y2	FMCB_DP_C2M_N1
FMCB_DP_M2C_P2	Y5	GXBR4F_RX_CH2P, GXBR4F_REFCLK2P	GXBR4F_TX_CH2P	V1	FMCB_DP_C2M_P2
FMCB_DP_M2C_N2	Y6	GXBR4F_RX_CH2N, GXBR4F_REFCLK2N	GXBR4F_TX_CH2N	V2	FMCB_DP_C2M_N2
FMCB_DP_M2C_P3	V5	GXBR4F_RX_CH3P, GXBR4F_REFCLK3P	GXBR4F_TX_CH3P	T1	FMCB_DP_C2M_P3
FMCB_DP_M2C_N3	V6	GXBR4F_RX_CH3N, GXBR4F_REFCLK3N	GXBR4F_TX_CH3N	T2	FMCB_DP_C2M_N3
FMCB_DP_M2C_P4	U3	GXBR4F_RX_CH4P, GXBR4F_REFCLK4P	GXBR4F_TX_CH4P	P1	FMCB_DP_C2M_P4
FMCB_DP_M2C_N4	U4	GXBR4F_RX_CH4N, GXBR4F_REFCLK4N	GXBR4F_TX_CH4N	P2	FMCB_DP_C2M_N4
FMCB_DP_M2C_P5	T5	GXBR4F_RX_CH5P, GXBR4F_REFCLK5P	GXBR4F_TX_CH5P	M1	FMCB_DP_C2M_P5
FMCB_DP_M2C_N5	T6	GXBR4F_RX_CH5N, GXBR4F_REFCLK5N	GXBR4F_TX_CH5N	M2	FMCB_DP_C2M_N5
FMCB_GBTCLK_M2C_P0	W8	REFCLK_GXBR4F_CHTP			
FMCB_GBTCLK_M2C_N0	W7	REFCLK_GXBR4F_CHTN			
REFCLK_FMCB_P	AA8	REFCLK_GXBR4F_CHBP			
REFCLK_FMCB_N	AA7	REFCLK_GXBR4F_CHBN			

10AX115F1932C

9 REFCLK4_P
9 REFCLK4_N

FMC INTERFACE

19 FMCA_DP_M2C_P[15:0]
19 FMCA_DP_M2C_N[15:0]
19 FMCA_DP_C2M_P[15:0]
19 FMCA_DP_C2M_N[15:0]
19 FMCA_GBTCLK_M2C_P[1:0]
19 FMCA_GBTCLK_M2C_N[1:0]

20 FMCB_DP_M2C_P[15:0]
20 FMCB_DP_M2C_N[15:0]
20 FMCB_DP_C2M_P[15:0]
20 FMCB_DP_C2M_N[15:0]
20 FMCB_GBTCLK_M2C_P[1:0]
20 FMCB_GBTCLK_M2C_N[1:0]

U28M — ARRIA 10 - RIGHT TRANSCEIVER BANK-4D

FMCA_DP_M2C_P6	AN3	GXBR4D_RX_CH0P, GXBR4D_REFCLK0P	GXBR4D_TX_CH0P	AY1	FMCA_DP_C2M_P6
FMCA_DP_M2C_N6	AN4	GXBR4D_RX_CH0N, GXBR4D_REFCLK0N	GXBR4D_TX_CH0N	AY2	FMCA_DP_C2M_N6
FMCA_DP_M2C_P7	AM5	GXBR4D_RX_CH1P, GXBR4D_REFCLK1P	GXBR4D_TX_CH1P	AW3	FMCA_DP_C2M_P7
FMCA_DP_M2C_N7	AM6	GXBR4D_RX_CH1N, GXBR4D_REFCLK1N	GXBR4D_TX_CH1N	AW4	FMCA_DP_C2M_N7
FMCA_DP_M2C_P8	AL3	GXBR4D_RX_CH2P, GXBR4D_REFCLK2P	GXBR4D_TX_CH2P	AV1	FMCA_DP_C2M_P8
FMCA_DP_M2C_N8	AL4	GXBR4D_RX_CH2N, GXBR4D_REFCLK2N	GXBR4D_TX_CH2N	AV2	FMCA_DP_C2M_N8
FMCA_DP_M2C_P9	AK5	GXBR4D_RX_CH3P, GXBR4D_REFCLK3P	GXBR4D_TX_CH3P	AU3	FMCA_DP_C2M_P9
FMCA_DP_M2C_N9	AK6	GXBR4D_RX_CH3N, GXBR4D_REFCLK3N	GXBR4D_TX_CH3N	AU4	FMCA_DP_C2M_N9
FMCA_DP_M2C_P10	AJ3	GXBR4D_RX_CH4P, GXBR4D_REFCLK4P	GXBR4D_TX_CH4P	AT1	FMCA_DP_C2M_P10
FMCA_DP_M2C_N10	AJ4	GXBR4D_RX_CH4N, GXBR4D_REFCLK4N	GXBR4D_TX_CH4N	AT2	FMCA_DP_C2M_N10
FMCA_DP_M2C_P11	AH5	GXBR4D_RX_CH5P, GXBR4D_REFCLK5P	GXBR4D_TX_CH5P	AR3	FMCA_DP_C2M_P11
FMCA_DP_M2C_N11	AH6	GXBR4D_RX_CH5N, GXBR4D_REFCLK5N	GXBR4D_TX_CH5N	AR4	FMCA_DP_C2M_N11
10.0K R335	AG8	REFCLK_GXBR4D_CHTP			
	AG7	REFCLK_GXBR4D_CHTN			
FMCA_GBTCLK_M2C_P1	AJ8	REFCLK_GXBR4D_CHBP			
FMCA_GBTCLK_M2C_N1	AJ7	REFCLK_GXBR4D_CHBN			

10AX115F1932C

U28P — ARRIA 10 - RIGHT TRANSCEIVER BANK-4G

FMCB_DP_M2C_P6	R3	GXBR4G_RX_CH0P, GXBR4G_REFCLK0P	GXBR4G_TX_CH0P	K1	FMCB_DP_C2M_P6
FMCB_DP_M2C_N6	R4	GXBR4G_RX_CH0N, GXBR4G_REFCLK0N	GXBR4G_TX_CH0N	K2	FMCB_DP_C2M_N6
FMCB_DP_M2C_P7	P5	GXBR4G_RX_CH1P, GXBR4G_REFCLK1P	GXBR4G_TX_CH1P	J3	FMCB_DP_C2M_P7
FMCB_DP_M2C_N7	P6	GXBR4G_RX_CH1N, GXBR4G_REFCLK1N	GXBR4G_TX_CH1N	J4	FMCB_DP_C2M_N7
FMCB_DP_M2C_P8	N3	GXBR4G_RX_CH2P, GXBR4G_REFCLK2P	GXBR4G_TX_CH2P	H1	FMCB_DP_C2M_P8
FMCB_DP_M2C_N8	N4	GXBR4G_RX_CH2N, GXBR4G_REFCLK2N	GXBR4G_TX_CH2N	H2	FMCB_DP_C2M_N8
FMCB_DP_M2C_P9	M5	GXBR4G_RX_CH3P, GXBR4G_REFCLK3P	GXBR4G_TX_CH3P	G3	FMCB_DP_C2M_P9
FMCB_DP_M2C_N9	M6	GXBR4G_RX_CH3N, GXBR4G_REFCLK3N	GXBR4G_TX_CH3N	G4	FMCB_DP_C2M_N9
FMCB_DP_M2C_P10	L3	GXBR4G_RX_CH4P, GXBR4G_REFCLK4P	GXBR4G_TX_CH4P	F1	FMCB_DP_C2M_P10
FMCB_DP_M2C_N10	L4	GXBR4G_RX_CH4N, GXBR4G_REFCLK4N	GXBR4G_TX_CH4N	F2	FMCB_DP_C2M_N10
FMCB_DP_M2C_P11	K5	GXBR4G_RX_CH5P, GXBR4G_REFCLK5P	GXBR4G_TX_CH5P	E3	FMCB_DP_C2M_P11
FMCB_DP_M2C_N11	K6	GXBR4G_RX_CH5N, GXBR4G_REFCLK5N	GXBR4G_TX_CH5N	E4	FMCB_DP_C2M_N11
10.0K R350	R8	REFCLK_GXBR4G_CHTP			
	R7	REFCLK_GXBR4G_CHTN			
FMCB_GBTCLK_M2C_P1	U8	REFCLK_GXBR4G_CHBP			
FMCB_GBTCLK_M2C_N1	U7	REFCLK_GXBR4G_CHBN			

10AX115F1932C

10 REFCLK_FMCA_P
10 REFCLK_FMCA_N
10 REFCLK_FMCB_P
10 REFCLK_FMCB_N

U28N — ARRIA 10 - RIGHT TRANSCEIVER BANK-4E

FMCA_DP_M2C_P12	AG3	GXBR4E_RX_CH0P, GXBR4E_REFCLK0P	GXBR4E_TX_CH0P	AP1	FMCA_DP_C2M_P12
FMCA_DP_M2C_N12	AG4	GXBR4E_RX_CH0N, GXBR4E_REFCLK0N	GXBR4E_TX_CH0N	AP2	FMCA_DP_C2M_N12
FMCA_DP_M2C_P13	AF5	GXBR4E_RX_CH1P, GXBR4E_REFCLK1P	GXBR4E_TX_CH1P	AM1	FMCA_DP_C2M_P13
FMCA_DP_M2C_N13	AF6	GXBR4E_RX_CH1N, GXBR4E_REFCLK1N	GXBR4E_TX_CH1N	AM2	FMCA_DP_C2M_N13
FMCA_DP_M2C_P14	AE3	GXBR4E_RX_CH2P, GXBR4E_REFCLK2P	GXBR4E_TX_CH2P	AK1	FMCA_DP_C2M_P14
FMCA_DP_M2C_N14	AE4	GXBR4E_RX_CH2N, GXBR4E_REFCLK2N	GXBR4E_TX_CH2N	AK2	FMCA_DP_C2M_N14
FMCA_DP_M2C_P15	AD5	GXBR4E_RX_CH3P, GXBR4E_REFCLK3P	GXBR4E_TX_CH3P	AH1	FMCA_DP_C2M_P15
FMCA_DP_M2C_N15	AD6	GXBR4E_RX_CH3N, GXBR4E_REFCLK3N	GXBR4E_TX_CH3N	AH2	FMCA_DP_C2M_N15
	AC3	GXBR4E_RX_CH4P, GXBR4E_REFCLK4P	GXBR4E_TX_CH4P	AF1	
	AC4	GXBR4E_RX_CH4N, GXBR4E_REFCLK4N	GXBR4E_TX_CH4N	AF2	
	AB5	GXBR4E_RX_CH5P, GXBR4E_REFCLK5P	GXBR4E_TX_CH5P	AD1	
	AB6	GXBR4E_RX_CH5N, GXBR4E_REFCLK5N	GXBR4E_TX_CH5N	AD2	
REFCLK4_P	AC8	REFCLK_GXBR4E_CHTP			
REFCLK4_N	AC7	REFCLK_GXBR4E_CHTN			
10.0K R351	AE8	REFCLK_GXBR4E_CHBP			
	AE7	REFCLK_GXBR4E_CHBN			

10AX115F1932C

U28Q — ARRIA 10 - RIGHT TRANSCEIVER BANK-4H

FMCB_DP_M2C_P12	H5	GXBR4H_RX_CH0P, GXBR4H_REFCLK0P	GXBR4H_TX_CH0P	D1	FMCB_DP_C2M_P12
FMCB_DP_M2C_N12	H6	GXBR4H_RX_CH0N, GXBR4H_REFCLK0N	GXBR4H_TX_CH0N	D2	FMCB_DP_C2M_N12
FMCB_DP_M2C_P13	G7	GXBR4H_RX_CH1P, GXBR4H_REFCLK1P	GXBR4H_TX_CH1P	C3	FMCB_DP_C2M_P13
FMCB_DP_M2C_N13	G8	GXBR4H_RX_CH1N, GXBR4H_REFCLK1N	GXBR4H_TX_CH1N	C4	FMCB_DP_C2M_N13
FMCB_DP_M2C_P14	F5	GXBR4H_RX_CH2P, GXBR4H_REFCLK2P	GXBR4H_TX_CH2P	B1	FMCB_DP_C2M_P14
FMCB_DP_M2C_N14	F6	GXBR4H_RX_CH2N, GXBR4H_REFCLK2N	GXBR4H_TX_CH2N	B2	FMCB_DP_C2M_N14
FMCB_DP_M2C_P15	E7	GXBR4H_RX_CH3P, GXBR4H_REFCLK3P	GXBR4H_TX_CH3P	A3	FMCB_DP_C2M_P15
FMCB_DP_M2C_N15	E8	GXBR4H_RX_CH3N, GXBR4H_REFCLK3N	GXBR4H_TX_CH3N	A4	FMCB_DP_C2M_N15
	D5	GXBR4H_RX_CH4P, GXBR4H_REFCLK4P	GXBR4H_TX_CH4P	B5	
	D6	GXBR4H_RX_CH4N, GXBR4H_REFCLK4N	GXBR4H_TX_CH4N	B6	
	C7	GXBR4H_RX_CH5P, GXBR4H_REFCLK5P	GXBR4H_TX_CH5P	A7	
	C8	GXBR4H_RX_CH5N, GXBR4H_REFCLK5N	GXBR4H_TX_CH5N	A8	
10.0K R334	L8	REFCLK_GXBR4H_CHTP			
	L7	REFCLK_GXBR4H_CHTN			
	N8	REFCLK_GXBR4H_CHBP			
	N7	REFCLK_GXBR4H_CHBN			

10AX115F1932C

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 12 of 49

5M2210 System Controller

U16A

MAX V BANK1

FM_D23	G2	DIFFIO_L8P	DIFFIO_L13P	J4	FPGA_nSTATUS
FM_D28	E1	DIFFIO_L5N	DIFFIO_L13N	K1	FPGA_CONF_DONE
FM_D29	G3	DIFFIO_L8N	DIFFIO_B13N/DEV_CLRn	M9	FPGA_DCLK
FM_D30	F3	DIFFIO_L5P	DIFFIO_L14N	K2	USB_CFG2
FM_D31	F2	DIFFIO_L6N	DIFFIO_L15P	K5	USB_CFG3
FM_D24	E5	DIFFIO_L4N	DIFFIO_L15N	L1	USB_CFG4
FM_D25	C3	DIFFIO_L2P	DIFFIO_L16P	L2	USB_CFG5
FM_D26	D3	DIFFIO_L1P	DIFFIO_L16N	K3	USB_CFG6
FM_D27	D2	DIFFIO_L3P	DIFFIO_L17P	M1	USB_CFG12
FM_D20	D1	DIFFIO_L4P	DIFFIO_L17N	M2	USB_CFG7
FM_D21	F1	DIFFIO_L7P	DIFFIO_L18P	L4	USB_CFG8
FM_D22	E3	DIFFIO_L2N	DIFFIO_L18N	L3	USB_CFG9
FM_D16	E4	DIFFIO_L3N	DIFFIO_L19P	N1	USB_CFG10
FM_D17	F6	DIFFIO_L7N	DIFFIO_L19N	M4	USB_CFG0
FM_D18	F4	DIFFIO_L6P	DIFFIO_L20P	N2	USB_CFG11
FM_D19	C2	DIFFIO_L1N	DIFFIO_L20N	M3	USB_CFG1
FMCA_PRSNTn	G1	DIFFIO_L9P	DIFFIO_L21P	N3	USB_CFG13
FMCB_PRSNTn	E2	IOB1_1	DIFFIO_L21N	P2	USB_CFG14
FM_A25	H13	DIFFIO_R11P			
FM_A24	G5	DIFFIO_L10N	DIFFIO_L9N	G4	
FM_A23	J13	DIFFIO_R12P	IOB1_2	F5	
FLASH_WEn	J1	DIFFIO_L11N	IOB1_3	H1	
FM_A26	H4	DIFFIO_L12P	DIFFIO_B22P	R16	FMCA_C2M_PG
	J2	DIFFIO_L12N	IOB1_5	L5	FMCB_C2M_PG
USB_M5_CLK	H5	IOB1/CLK0	TCK	P3	26 M5_JTAG_TCK
CLK_CONFIG	J5	IOB1/CLK1	TDI	L6	26 M5_JTAG_TDI
			TDO	M5	26 M5_JTAG_TDO
			TMS	N4	26 M5_JTAG_TMS

5M2210ZF256

U16B

MAX V BANK2

SI516_FS	C5	DIFFIO_T2P	DIFFIO_T13P	E10	
	B1	DIFFIO_T1N	DIFFIO_T13N	A11	
	C13	DIFFIO_T18P	DIFFIO_T14P	B11	
	C4	DIFFIO_T2N	DIFFIO_T14N	A12	
	B4	DIFFIO_T3P	DIFFIO_T5N	D7	MAX_CONF_DONE
	A13	IOB2_6	DIFFIO_T15N	B12	
	E6	DIFFIO_T4P	DIFFIO_T16P	C11	
TSENSE_ALERTn	B14	DIFFIO_T17N	DIFFIO_T8N	A7	PGM_SEL
	A5	DIFFIO_T5P	IOB2_10	A6	PGM_CONFIG
	A4	IOB2_9	DIFFIO_T3N	D6	PGM_LED0
	B10	IOB2_11	IOB2_15	C6	PGM_LED1
	E7	DIFFIO_T6N	DIFFIO_T7N	B7	PGM_LED2
OVERTEMPn	B16	DIFFIO_T18N			
OVERTEMP	E11	DIFFIO_T15P			
SENSE_SMB_CLK	A15	IOB2_7	IOB2_8	A2	CLK_SEL
SENSE_SMB_DATA	B13	DIFFIO_T16N	DIFFIO_T1P	D4	CLK_ENABLE
ED8101_ALERT	B8	DIFFIO_T9P	DIFFIO_T4N	B5	FACTORY_LOAD
ED8101_SCL	A8	DIFFIO_T9N	IOB2_16	C7	MAX_ERROR
ED8101_SDA	A9	DIFFIO_T10P	DIFFIO_T6P	B6	MAX_LOAD
	D12	DIFFIO_T17P	DIFFIO_T12N	C9	SENSE_SDO
CLK125_EN	E9	DIFFIO_T10N	IOB2_12	B3	SENSE_SDI
CLOCK_I2C_SDA	C10	IOB2_13	DIFFIO_T11P	B9	SENSE_SCK
Si570_EN	A10	DIFFIO_T12P	DIFFIO_T11N	D9	SENSE_CS0n
CLOCK_I2C_SCL	C12	IOB2_14	DIFFIO_T8P	D8	
				C8	
			DIFFIO_T7P	D10	
			IOB2_17	D11	
			IOB2_18	D5	
			IOB2_19	E8	
			IOB2_20		

5M2210ZF256

U16C

MAX V BANK3

FPGA_PR_REQUEST	T4	IOB4_33	DIFFIO_R13N	J15	FM_D0
FM_A1	F15	DIFFIO_R6N	DIFFIO_R16P	L16	FM_D1
FM_A2	G16	DIFFIO_R9N	DIFFIO_R19N	L14	FM_D2
FM_A3	G15	DIFFIO_R8N	DIFFIO_R15N	K14	FM_D3
FM_A4	H16	DIFFIO_R11N	DIFFIO_R18N	L13	FM_D4
FM_A5	H15	DIFFIO_R10N	DIFFIO_R17P	L15	FM_D5
FM_A6	F16	DIFFIO_R7N	DIFFIO_R19P	M15	FM_D6
FM_A7	G14	DIFFIO_R7P	DIFFIO_R18P	M16	FM_D7
FM_A8	D16	DIFFIO_R4N	DIFFIO_R14P	K16	FM_D8
FM_A9	E15	DIFFIO_R5N	DIFFIO_R15P	K15	FM_D9
FM_A10	E16	DIFFIO_R6P	DIFFIO_R13P	J14	FM_D10
FM_A11	H14	DIFFIO_R10P	DIFFIO_R14N	K13	FM_D11
FM_A12	D15	DIFFIO_R3N	DIFFIO_R17N	L12	FM_D12
FM_A13	F14	DIFFIO_R4P	DIFFIO_R20P	N16	FM_D13
FM_A14	C14	DIFFIO_R1N	DIFFIO_R20N	M13	FM_D14
FM_A15	C15	DIFFIO_R2P	DIFFIO_R16N	L11	FM_D15
FM_A16	H3	DIFFIO_L11P	IOB3_22	D14	FLASH_CEn0
FM_A17	H2	DIFFIO_L10P	DIFFIO_R22N	P14	FLASH_OEn
FM_A18	E13	DIFFIO_R2N	IOB3_24	F12	FLASH_RDYBSYn0
FM_A19	F13	DIFFIO_R5P	IOB3_21	D13	FLASH_RESETn
FM_A20	G13	DIFFIO_R8P			
FM_A21	G12	DIFFIO_R9P	DIFFIO_R21P	N15	FLASH_CLK
FM_A22	E12	DIFFIO_R3P	DIFFIO_R21N	N14	FLASH_ADVn
CLK50_EN	J16	DIFFIO_R12N	IOB3_23	F11	FLASH_CEn1
			DIFFIO_R22P	P15	FLASH_RDYBSYn1
			IOB3_25	K12	FPGA_PR_ERROR
MV_CLK_50	J12	IOB3/CLK2	IOB3_26	M14	FPGA_CvP_CONFDONE
FPGA_PR_DONE	H12	IOB3/CLK3	DIFFIO_B21P	P12	FPGA_PR_READY

5M2210ZF256

U16D

MAX V BANK4

FPGA_CONFIG_D0	R1	DIFFIO_B1P	DIFFIO_B15P	N10	MAX5_OEn
FPGA_CONFIG_D1	T2	DIFFIO_B2P	DIFFIO_B15N	T11	MAX5_CSn
FPGA_CONFIG_D2	N6	DIFFIO_B4N	DIFFIO_B16N	R11	MAX5_WEn
FPGA_CONFIG_D3	N5	DIFFIO_B3N	DIFFIO_B17N	N11	MAX5_CLK
FPGA_CONFIG_D4	N7	DIFFIO_B7N	DIFFIO_B14N	R10	MAX5_BEn0
FPGA_CONFIG_D5	N8	DIFFIO_B10P	DIFFIO_B14P	M10	MAX5_BEn1
FPGA_CONFIG_D6	M12	IOB4_29	DIFFIO_B17P	T12	MAX5_BEn2
FPGA_CONFIG_D7	T13	DIFFIO_B19P	DIFFIO_B16P	P10	MAX5_BEn3
FPGA_CONFIG_D8	T15	DIFFIO_B21N	DIFFIO_B11N	T9	FPGA_CONFIG_D27
FPGA_CONFIG_D9	R13	DIFFIO_B19N	DIFFIO_B12P	R9	FPGA_CONFIG_D26
FPGA_CONFIG_D10	P4	DIFFIO_B1N	IOB1_4	K4	CPU_RESETn
FPGA_CONFIG_D11	R3	DIFFIO_B3P	DIFFIO_B20P	N12	SDI_MF2_MUTE
FPGA_CONFIG_D12	T10	IOB4_32	DIFFIO_B22N	P13	SDI_MF0_BYPASS
FPGA_CONFIG_D13	P5	DIFFIO_B2N	DIFFIO_B20N	R14	SDI_MF1_AUTO_SLEEP
FPGA_CONFIG_D14	R4	IOB4_31	IOB3_27	N13	SDI_TX_SD_HDn
FPGA_CONFIG_D15	R5	DIFFIO_B5P	DIFFIO_B9N	T7	FPGA_CONFIG_D28
FPGA_CONFIG_D16	M8	DIFFIO_B13P/DEV_OE	DIFFIO_B18P	R12	MSEL0
FPGA_CONFIG_D17	M7	DIFFIO_B8P	DIFFIO_B18N	P11	MSEL1
FPGA_CONFIG_D18	T5	DIFFIO_B6P	IOB4_28	M11	MSEL2
FPGA_CONFIG_D19	P9	DIFFIO_B12N	DIFFIO_B8N	R7	FPGA_CONFIG_D25
FPGA_CONFIG_D20	M6	DIFFIO_B5N	DIFFIO_B9P	P8	FPGA_CONFIG_D29
FPGA_CONFIG_D21	N9	IOB4_30	DIFFIO_B7P	R6	FPGA_CONFIG_D30
FPGA_CONFIG_D23	T8	DIFFIO_B11P	DIFFIO_B4P	P6	FPGA_CONFIG_D31
FPGA_CONFIG_D22	R8	DIFFIO_B10N	DIFFIO_R1P	E14	FPGA_nCONFIG
MAX_RESETn	J3	DIFFIO_L14P			
FPGA_CONFIG_D24	P7	DIFFIO_B6N			

5M2210ZF256

U16E

MAX V Power

F7	GNDINT	VCCINT	F10	
G6	GNDINT	VCCINT	G11	
H7	GNDINT	VCCINT	H10	
H9	GNDINT	VCCINT	H8	
J10	GNDINT	VCCINT	J7	
J8	GNDINT	VCCINT	J9	
K11	GNDINT	VCCINT	K6	
L10	GNDINT	VCCINT	L7	
A1	GNDIO	VCCIO1	C1	1.8V
A16	GNDIO	VCCIO1	H6	
B15	GNDIO	VCCIO1	J6	
B2	GNDIO	VCCIO1	P1	
G10	GNDIO			
G7	GNDIO	VCCIO2	A14	2.5V
G8	GNDIO	VCCIO2	A3	
G9	GNDIO	VCCIO2	F8	
K10	GNDIO	VCCIO2	F9	
K7	GNDIO			
K8	GNDIO	VCCIO3	C16	1.8V
K9	GNDIO	VCCIO3	H11	
R15	GNDIO	VCCIO3	J11	
R2	GNDIO	VCCIO3	P16	
T1	GNDIO			
T16	GNDIO	VCCIO4	L8	
T6	GNDIO	VCCIO4	L9	
		VCCIO4	T14	
		VCCIO4	T3	

5M2210ZF256

1.8V

7 FPGA_CONFIG_D[31:0]

7 FPGA_nSTATUS
7,35 FPGA_CONF_DONE
7,14 FPGA_DCLK
7 FPGA_nCONFIG

7 FPGA_PR_DONE
7 FPGA_PR_REQUEST
7 FPGA_PR_READY
7 FPGA_PR_ERROR
7 FPGA_CvP_CONFDONE

29 TSENSE_ALERTn
29 OVERTEMPn
29 OVERTEMP
29,30 SENSE_SMB_CLK
29,30 SENSE_SMB_DATA

4,23 SDI_MF2_MUTE
4,23 SDI_MF0_BYPASS
4,23 SDI_MF1_AUTO_SLEEP
4,23 SDI_TX_SD_HDn

29 SENSE_SDO
29 SENSE_SDI
29 SENSE_SCK
29 SENSE_CS0n

32,39 ED8101_SDA
32,39 ED8101_SCL
32,39 ED8101_ALERT

5,14 FM_D[31:0]
5,14 FM_A[26:1]

5,14 FLASH_WEn
5,14 FLASH_CEn0
5,14 FLASH_CEn1
5,14 FLASH_OEn
5,14 FLASH_RDYBSYn0
8,14 FLASH_RDYBSYn1
5,14 FLASH_RESETn
5,14 FLASH_CLK
5,14 FLASH_ADVn

9 CLK125_EN
9 CLK50_EN
9 Si570_EN
9,13,24 SI516_FS
9,10 CLOCK_I2C_SDA
9,10 CLOCK_I2C_SCL

7 MSEL0
7 MSEL1
7 MSEL2

6 MAX5_BEn[3:0]
6 MAX5_OEn
6 MAX5_CSn
6 MAX5_WEn
8 MAX5_CLK

6,19,24,26 FMCA_PRSNTn
6,20,24,26 FMCB_PRSNTn

19 FMCA_C2M_PG
20 FMCB_C2M_PG

7,24 CPU_RESETn
9 MV_CLK_50

ON-BOARD USB BLASTER II

26 USB_CFG[14:0]
25 USB_M5_CLK

MAXV DIPSWITCH

9,24 CLK_SEL
24 CLK_ENABLE
24 FACTORY_LOAD
9,13,24 SI516_FS

PUSH BUTTON INTERFACE

24 PGM_SEL
24 PGM_CONFIG
24 MAX_RESETn

LED INTERFACE

24 PGM_LED[2:0]

24 MAX_ERROR
24 MAX_LOAD
24 MAX_CONF_DONE

1.8V

X5

1 EN VCC 4

2 GND OUT 3

125MHz

CLK_CONFIG

C128 2.2uF

C141 0.1uF

VCCINT

1.8V

C397 C426 C427 C400 C398 C402 C383 C401

0.1uF

1.8V VCCIO

1.8V

C455 C458 C343 C330 C384 C399

0.1uF

1.8V VCCIO

1.8V

C425 C353 C456 C457 C483 C385

0.1uF

Title: **Arria 10 GX FPGA Development Kit**

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

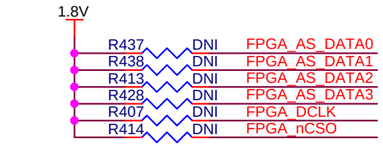
Date: Thursday, May 28, 2015 Sheet 13 of 49

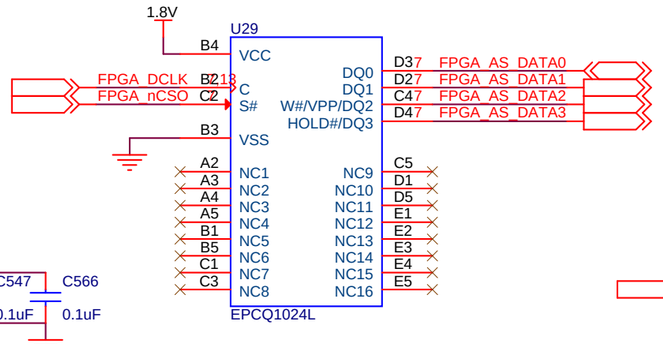
FLASH

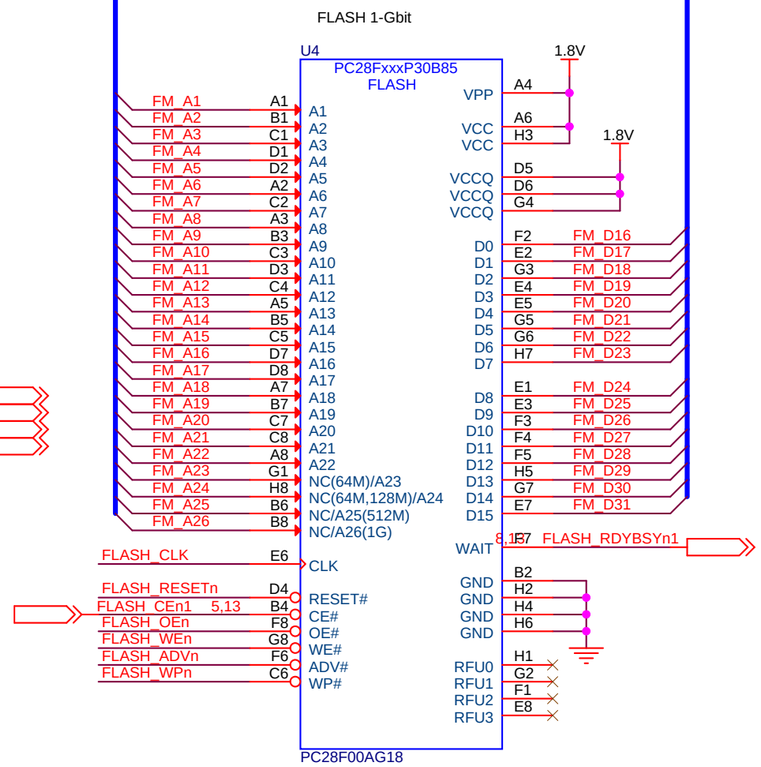
FM BUS

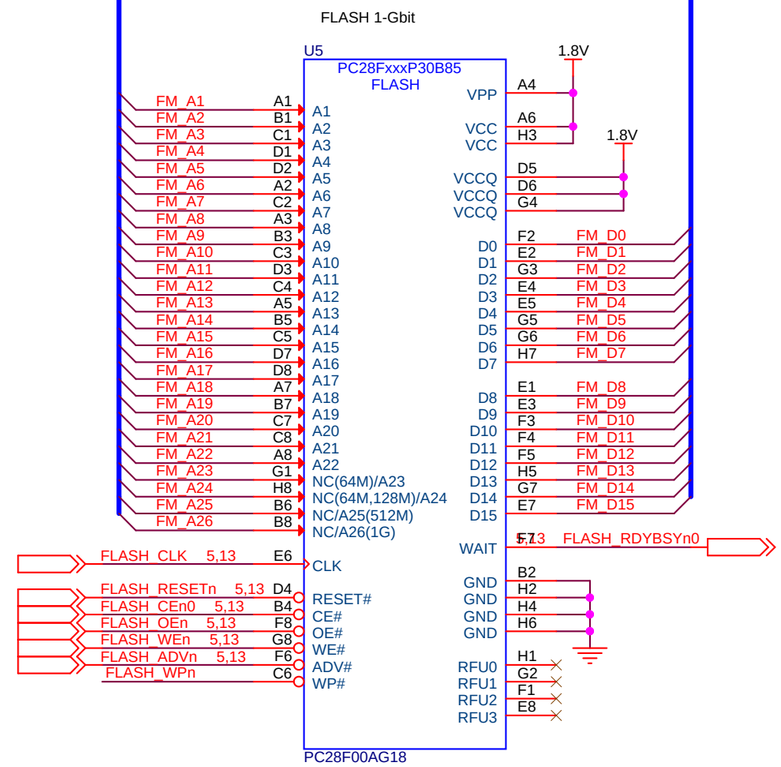
FM_D[31:0] 5,13

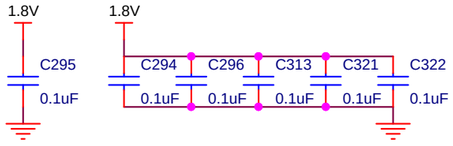
FM_A[26:1] 5,13

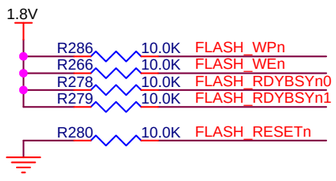


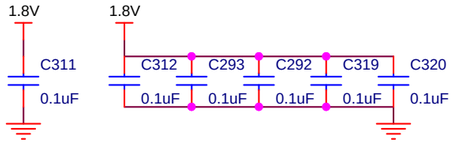












- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.
- When using dual x16 flash devices for an equivalent x32 (x16||x16) flash device a word consists of 32 data bits so addressing starts with FM_A1 mapped to address bit 2 in software.

Title: Arria 10 GX FPGA Development Kit

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 14 of 49

10/100/1000 Ethernet

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

SGMII Mode (default)

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

DVDD = 1.0V
DVDD = 1.2V

Place near 88E1111 PHY

ENET_DVDD = 1.0V/0.207A

Title: Arria 10 GX FPGA Development Kit
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Size: B | Document Number: 150-0321301-E1 (6XX-44362R) | Rev: E1.2

Date: Thursday, May 28, 2015 | Sheet 15 of 49

External Memory Interface Connector Map

DDR3 x72 (DQS x8	DDR4 x72 (DQS x8 Groups)	RLDRAM3 x36 (DQS x8/x9 Groups)	QDR IV x36 (DQS x18 Groups)	HiLo Pin Name	HiLo Pin Number
				CONFIG0	L6
				CONFIG1	M6
A0	A0	A0	A1	MEM_ADDR_CMD[0]	F1
A1	A1	A1	A2	MEM_ADDR_CMD[1]	H1
A10	A10	A10	A11	MEM_ADDR_CMD[10]	E4
A11	A11	A11	A12	MEM_ADDR_CMD[11]	F4
A12	A12	A12	A13	MEM_ADDR_CMD[12]	G4
A13	A13	A13	A14	MEM_ADDR_CMD[13]	H4
A14	A14	A14	A15	MEM_ADDR_CMD[14]	J4
A15	A15	A15	A16	MEM_ADDR_CMD[15]	K4
BA0	BA0	BA0	A19	MEM_ADDR_CMD[16]	M1
BA1	BA1	BA1	A20	MEM_ADDR_CMD[17]	M2
BA2	BG0	BA2	A21	MEM_ADDR_CMD[18]	N2
CASn	A17	A17	A18	MEM_ADDR_CMD[19]	L4
A2	A2	A2	A3	MEM_ADDR_CMD[2]	F2
CKE0	CKE0	A20	RWAn	MEM_ADDR_CMD[20]	P5
CKE1	CKE1	WEn	RWBn	MEM_ADDR_CMD[21]	M5
CSn0	CSn0	CSn0	LBK0n	MEM_ADDR_CMD[22]	P1
CSn1	ACTn	CSn1	LBK1n	MEM_ADDR_CMD[23]	R4
ODT0	ODT0	A18	LDAn	MEM_ADDR_CMD[24]	M4
ODT1	ODT1	A19	LDBn	MEM_ADDR_CMD[25]	R3
RASn	A16	A16	A17	MEM_ADDR_CMD[26]	L2
RESETn	RESETn	RESETn	RESETn	MEM_ADDR_CMD[27]	K1
WEn	BG1	BA3	CFGn	MEM_ADDR_CMD[28]	P2
	ALERTn	CSn3	A22	MEM_ADDR_CMD[29]	N4
A3	A3	A3	A4	MEM_ADDR_CMD[3]	G2
	CSn1	CSn2	AINV	MEM_ADDR_CMD[30]	P4
	PAR	REFn	A0	MEM_ADDR_CMD[31]	N3
A4	A4	A4	A5	MEM_ADDR_CMD[4]	H2
A5	A5	A5	A6	MEM_ADDR_CMD[5]	J2
A6	A6	A6	A7	MEM_ADDR_CMD[6]	K2
A7	A7	A7	A8	MEM_ADDR_CMD[7]	G3
A8	A8	A8	A9	MEM_ADDR_CMD[8]	J3
A9	A9	A9	A10	MEM_ADDR_CMD[9]	L3
CK_N0	CK_N0	CK_N	CK_N	MEM_CLK_N	V2
CK_P0	CK_P0	CK_P	CK_P	MEM_CLK_P	V1
DM0	LDM_n0		DINVA0	MEM_DMA[0]	B10
DM1	UDM_n0	DM1	QVLDA0	MEM_DMA[1]	C4
DM2	LDM_n1		DINVA1	MEM_DMA[2]	B17
DM3	UDM_n1		QVLDA1	MEM_DMA[3]	F17
DM4	LDM_n2	DQ18	DINVB0	MEM_DMB[0]	M16
DM5	UDM_n2		QVLDB0	MEM_DMB[1]	U16
DM6	LDM_n3	DQ0	DINVB1	MEM_DMB[2]	U11
DM7	UDM_n3		QVLDB1	MEM_DMB[3]	U6
DM8	LDM_n4			MEM_DQ_ADDR_CMD[0]	R6
DQ64	DQ64			MEM_DQ_ADDR_CMD[1]	T1
DQ65	DQ65			MEM_DQ_ADDR_CMD[2]	R2
DQ66	DQ66			MEM_DQ_ADDR_CMD[3]	T2

DDR3 x72 (DQS x8	DDR4 x72 (DQS x8 Groups)	RLDRAM3 x36 (DQS x8/x9 Groups)	QDR IV x36 (DQS x18 Groups)	HiLo Pin Name	HiLo Pin Number
DQ67	DQ67			MEM_DQ_ADDR_CMD[4]	U2
DQ68	DQ68			MEM_DQ_ADDR_CMD[5]	U3
DQ69	DQ69		AP	MEM_DQ_ADDR_CMD[6]	T4
DQ70	DQ70		A24	MEM_DQ_ADDR_CMD[7]	U4
DQ71	DQ71		A23	MEM_DQ_ADDR_CMD[8]	T5
DQ0	DQ0		DQA0	MEM_DQA[0]	A4
DQ1	DQ1		DQA1	MEM_DQA[1]	B4
DQ10	DQ10	DQ11	DQA9	MEM_DQA[10]	C2
DQ11	DQ11	DQ12	DQA10	MEM_DQA[11]	C3
DQ12	DQ12	DQ13	DQA11	MEM_DQA[12]	E3
DQ13	DQ13	DQ14	DQA12	MEM_DQA[13]	D4
DQ14	DQ14	DQ15	DQA13	MEM_DQA[14]	D1
DQ15	DQ15	DQ16	DQA14	MEM_DQA[15]	D2
DQ16	DQ16	QVLD1	DQA18	MEM_DQA[16]	A12
DQ17	DQ17		DQA19	MEM_DQA[17]	B12
DQ18	DQ18		DQA20	MEM_DQA[18]	B13
DQ19	DQ19		DQA21	MEM_DQA[19]	B14
DQ2	DQ2		DQA2	MEM_DQA[2]	B5
DQ20	DQ20		DQA22	MEM_DQA[20]	C15
DQ21	DQ21		DQA23	MEM_DQA[21]	A16
DQ22	DQ22		DQA24	MEM_DQA[22]	B16
DQ23	DQ23		QKA_N1	MEM_DQA[23]	A18
DQ24	DQ24	DQ27	DQA25	MEM_DQA[24]	C16
DQ25	DQ25	DQ28	DQA26	MEM_DQA[25]	D16
DQ26	DQ26	DQ29	DQA27	MEM_DQA[26]	E16
DQ27	DQ27	DQ30	DQA28	MEM_DQA[27]	F16
DQ28	DQ28	DQ31	DQA29	MEM_DQA[28]	D17
DQ29	DQ29	DQ32	DQA30	MEM_DQA[29]	C18
DQ3	DQ3		DQA3	MEM_DQA[3]	B6
DQ30	DQ30	DQ33	DQA31	MEM_DQA[30]	D18
DQ31	DQ31	DQ34	DQA32	MEM_DQA[31]	E18
		DQ17	DQA15	MEM_DQA[32]	E2
		DQ35	DQA33	MEM_DQA[33]	G16
DQ4	DQ4		DQA4	MEM_DQA[4]	A8
DQ5	DQ5		DQA5	MEM_DQA[5]	B8
DQ6	DQ6		DQA6	MEM_DQA[6]	B9
DQ7	DQ7		QKA_N0	MEM_DQA[7]	A10
DQ8	DQ8	DQ9	DQA7	MEM_DQA[8]	B1
DQ9	DQ9	DQ10	DQA8	MEM_DQA[9]	B2
DQ32	DQ32	DQ19	DQB0	MEM_DQB[0]	H16
DQ33	DQ33	DQ20	DQB1	MEM_DQB[1]	J16
DQ42	DQ42		DQB9	MEM_DQB[10]	P17
DQ43	DQ43		DQB10	MEM_DQB[11]	P18
DQ44	DQ44		DQB11	MEM_DQB[12]	R18
DQ45	DQ45		DQB12	MEM_DQB[13]	T16
DQ46	DQ46		DQB13	MEM_DQB[14]	T17
DQ47	DQ47		DQB14	MEM_DQB[15]	T18
DQ48	DQ48	DQ1	DQB18	MEM_DQB[16]	U15

DDR3 x72 (DQS x8	DDR4 x72 (DQS x8 Groups)	RLDRAM3 x36 (DQS x8/x9 Groups)	QDR IV x36 (DQS x18 Groups)	HiLo Pin Name	HiLo Pin Number
DQ49	DQ49	DQ2	DQB19	MEM_DQB[17]	T14
DQ50	DQ50	DQ3	DQB20	MEM_DQB[18]	U14
DQ51	DQ51	DQ4	DQB21	MEM_DQB[19]	V14
DQ34	DQ34	DQ21	DQB2	MEM_DQB[2]	K16
DQ52	DQ52	DQ5	DQB22	MEM_DQB[20]	T13
DQ53	DQ53	DQ6	DQB23	MEM_DQB[21]	T12
DQ54	DQ54	DQ7	DQB24	MEM_DQB[22]	U12
DQ55	DQ55	DQ8	QKB_N1	MEM_DQB[23]	V12
DQ56	DQ56		DQB25	MEM_DQB[24]	T10
DQ57	DQ57		DQB26	MEM_DQB[25]	U10
DQ58	DQ58		DQB27	MEM_DQB[26]	V10
DQ59	DQ59		DQB28	MEM_DQB[27]	T9
DQ60	DQ60		DQB29	MEM_DQB[28]	T8
DQ61	DQ61		DQB30	MEM_DQB[29]	U8
DQ35	DQ35	DQ22	DQB3	MEM_DQB[3]	L16
DQ62	DQ62		DQB31	MEM_DQB[30]	U7
DQ63	DQ63		DQB32	MEM_DQB[31]	V6
			DQB15	MEM_DQB[32]	R16
			DQB33	MEM_DQB[33]	T6
DQ36	DQ36	DQ23	DQB4	MEM_DQB[4]	H17
DQ37	DQ37	DQ24	DQB5	MEM_DQB[5]	K17
DQ38	DQ38	DQ25	DQB6	MEM_DQB[6]	K18
DQ39	DQ39	DQ26	QKB_N0	MEM_DQB[7]	L18
DQ40	DQ40	QVLD0	DQB7	MEM_DQB[8]	M17
DQ41	DQ41		DQB8	MEM_DQB[9]	N18
DQS_N8	DQSL_N4			MEM_DQS_ADDR_CMD_N	V5
DQS_P8	DQSL_P4		PEn	MEM_DQS_ADDR_CMD_P	V4
DQS_N0	DQSL_N0		DQA17	MEM_DQSA_N[0]	A7
DQS_N1	DQSU_N0	QK1#	DKA_N0	MEM_DQSA_N[1]	A3
DQS_N2	DQSL_N1	DK1#	DQA35	MEM_DQSA_N[2]	A15
DQS_N3	DQSU_N1	QK3#	DKA_N1	MEM_DQSA_N[3]	G18
DQS_P0	DQSL_P0		DQA16	MEM_DQSA_P[0]	A6
DQS_P1	DQSU_P0	QK1	DKA_P0	MEM_DQSA_P[1]	A2
DQS_P2	DQSL_P1	DK1	DQA34	MEM_DQSA_P[2]	A14
DQS_P3	DQSU_P1	QK3	DKA_P1	MEM_DQSA_P[3]	F18
DQS_N4	DQSL_N2	QK2#	DQB17	MEM_DQSB_N[0]	J18
DQS_N5	DQSU_N2	DK0#	DKB_N0	MEM_DQSB_N[1]	V18
DQS_N6	DQSL_N3	QK0#	DQB35	MEM_DQSB_N[2]	V17
DQS_N7	DQSU_N3		DKB_N1	MEM_DQSB_N[3]	V9
DQS_P4	DQSL_P2	QK2	DQB16	MEM_DQSB_P[0]	H18
DQS_P5	DQSU_P2	DK0	DKB_P0	MEM_DQSB_P[1]	U18
DQS_P6	DQSL_P3	QK0	DQB34	MEM_DQSB_P[2]	V16
DQS_P7	DQSU_P3		DKB_P1	MEM_DQSB_P[3]	V8
			QKA_P0	MEM_QKA_P[0]	A11
			QKA_P1	MEM_QKA_P[1]	B18
			QKB_P0	MEM_QKB_P[0]	M18
		DM0	QKB_P1	MEM_QKB_P[1]	V13

Title: Arria 10 GX FPGA Development Kit

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 16 of 49

External Memory Interface - HiLo connector

J14A — HiLo EMI - EMI SIGNALS

MEM_ADDR_CMD0	F1	MEM_ADDR_CMD0	MEM_DQ_ADDR_CMD0	R6	MEM_DQ_ADDR_CMD0
MEM_ADDR_CMD1	H1	MEM_ADDR_CMD1	MEM_DQ_ADDR_CMD1	T1	MEM_DQ_ADDR_CMD1
MEM_ADDR_CMD2	F2	MEM_ADDR_CMD2	MEM_DQ_ADDR_CMD2	R2	MEM_DQ_ADDR_CMD2
MEM_ADDR_CMD3	G2	MEM_ADDR_CMD3	MEM_DQ_ADDR_CMD3	T2	MEM_DQ_ADDR_CMD3
MEM_ADDR_CMD4	H2	MEM_ADDR_CMD4	MEM_DQ_ADDR_CMD4	U2	MEM_DQ_ADDR_CMD4
MEM_ADDR_CMD5	J2	MEM_ADDR_CMD5	MEM_DQ_ADDR_CMD5	U3	MEM_DQ_ADDR_CMD5
MEM_ADDR_CMD6	K2	MEM_ADDR_CMD6	MEM_DQ_ADDR_CMD6	T4	MEM_DQ_ADDR_CMD6
MEM_ADDR_CMD7	G3	MEM_ADDR_CMD7	MEM_DQ_ADDR_CMD7	U4	MEM_DQ_ADDR_CMD7
MEM_ADDR_CMD8	J3	MEM_ADDR_CMD8	MEM_DQ_ADDR_CMD8	T5	MEM_DQ_ADDR_CMD8
MEM_ADDR_CMD9	L3	MEM_ADDR_CMD9			
MEM_ADDR_CMD10	E4	MEM_ADDR_CMD10	MEM_DQS_ADDR_CMD_P	V4	MEM_DQS_ADDR_CMD_P
MEM_ADDR_CMD11	F4	MEM_ADDR_CMD11	MEM_DQS_ADDR_CMD_N	V5	MEM_DQS_ADDR_CMD_N
MEM_ADDR_CMD12	G4	MEM_ADDR_CMD12			
MEM_ADDR_CMD13	H4	MEM_ADDR_CMD13			
MEM_ADDR_CMD14	J4	MEM_ADDR_CMD14	MEM_CLK_P	V1	MEM_CLK_P
MEM_ADDR_CMD15	K4	MEM_ADDR_CMD15	MEM_CLK_N	V2	MEM_CLK_N
MEM_ADDR_CMD16	M1	MEM_ADDR_CMD16			
MEM_ADDR_CMD17	M2	MEM_ADDR_CMD17			
MEM_ADDR_CMD18	N2	MEM_ADDR_CMD18	CONFIG0	L6	
MEM_ADDR_CMD19	L4	MEM_ADDR_CMD19	CONFIG1	M6	
MEM_ADDR_CMD20	P5	MEM_ADDR_CMD20			
MEM_ADDR_CMD21	M5	MEM_ADDR_CMD21			
MEM_ADDR_CMD22	P1	MEM_ADDR_CMD22	RFU0	D5	
MEM_ADDR_CMD23	R4	MEM_ADDR_CMD23	RFU1	F5	
MEM_ADDR_CMD24	M4	MEM_ADDR_CMD24	RFU2	H5	
MEM_ADDR_CMD25	R3	MEM_ADDR_CMD25	RFU3	K5	
MEM_ADDR_CMD26	L2	MEM_ADDR_CMD26	RFU4	N6	
MEM_ADDR_CMD27	K1	MEM_ADDR_CMD27	RFU5	R7	
MEM_ADDR_CMD28	P2	MEM_ADDR_CMD28	RFU6	R8	
MEM_ADDR_CMD29	N4	MEM_ADDR_CMD29			
MEM_ADDR_CMD30	P4	MEM_ADDR_CMD30			
MEM_ADDR_CMD31	N3	MEM_ADDR_CMD31			
MEM_DMA0	B10	MEM_DMA0	MEM_DMB0	M16	MEM_DMB0
MEM_DMA1	C4	MEM_DMA1	MEM_DMB1	U16	MEM_DMB1
MEM_DMA2	B17	MEM_DMA2	MEM_DMB2	U11	MEM_DMB2
MEM_DMA3	F17	MEM_DMA3	MEM_DMB3	U6	MEM_DMB3
MEM_DQA0	A4	MEM_DQA0	MEM_DQB0	H16	MEM_DQB0
MEM_DQA1	B4	MEM_DQA1	MEM_DQB1	J16	MEM_DQB1
MEM_DQA2	B5	MEM_DQA2	MEM_DQB2	K16	MEM_DQB2
MEM_DQA3	B6	MEM_DQA3	MEM_DQB3	L16	MEM_DQB3
MEM_DQA4	A8	MEM_DQA4	MEM_DQB4	H17	MEM_DQB4
MEM_DQA5	B8	MEM_DQA5	MEM_DQB5	K17	MEM_DQB5
MEM_DQA6	B9	MEM_DQA6	MEM_DQB6	K18	MEM_DQB6
MEM_DQA7	A10	MEM_DQA7	MEM_DQB7	L18	MEM_DQB7
MEM_DQA8	B1	MEM_DQA8	MEM_DQB8	M17	MEM_DQB8
MEM_DQA9	B2	MEM_DQA9	MEM_DQB9	N18	MEM_DQB9
MEM_DQA10	C2	MEM_DQA10	MEM_DQB10	P17	MEM_DQB10
MEM_DQA11	C3	MEM_DQA11	MEM_DQB11	P18	MEM_DQB11
MEM_DQA12	E3	MEM_DQA12	MEM_DQB12	R18	MEM_DQB12
MEM_DQA13	D4	MEM_DQA13	MEM_DQB13	T16	MEM_DQB13
MEM_DQA14	D1	MEM_DQA14	MEM_DQB14	T17	MEM_DQB14
MEM_DQA15	D2	MEM_DQA15	MEM_DQB15	T18	MEM_DQB15
MEM_DQA16	A12	MEM_DQA16	MEM_DQB16	U15	MEM_DQB16
MEM_DQA17	B12	MEM_DQA17	MEM_DQB17	T14	MEM_DQB17
MEM_DQA18	B13	MEM_DQA18	MEM_DQB18	U14	MEM_DQB18
MEM_DQA19	B14	MEM_DQA19	MEM_DQB19	V14	MEM_DQB19
MEM_DQA20	C15	MEM_DQA20	MEM_DQB20	T13	MEM_DQB20
MEM_DQA21	A16	MEM_DQA21	MEM_DQB21	T12	MEM_DQB21
MEM_DQA22	B16	MEM_DQA22	MEM_DQB22	U12	MEM_DQB22
MEM_DQA23	A18	MEM_DQA23	MEM_DQB23	V12	MEM_DQB23
MEM_DQA24	C16	MEM_DQA24	MEM_DQB24	T10	MEM_DQB24
MEM_DQA25	D16	MEM_DQA25	MEM_DQB25	U10	MEM_DQB25
MEM_DQA26	E16	MEM_DQA26	MEM_DQB26	V10	MEM_DQB26
MEM_DQA27	F16	MEM_DQA27	MEM_DQB27	T9	MEM_DQB27
MEM_DQA28	D17	MEM_DQA28	MEM_DQB28	T8	MEM_DQB28
MEM_DQA29	C18	MEM_DQA29	MEM_DQB29	U8	MEM_DQB29
MEM_DQA30	D18	MEM_DQA30	MEM_DQB30	U7	MEM_DQB30
MEM_DQA31	E18	MEM_DQA31	MEM_DQB31	V6	MEM_DQB31
MEM_DQA32	E2	MEM_DQA32	MEM_DQB32	R16	MEM_DQB32
MEM_DQA33	G16	MEM_DQA33	MEM_DQB33	T6	MEM_DQB33
MEM_DQSA_P0	A6	MEM_DQSA_P0	MEM_DQSB_P0	H18	MEM_DQSB_P0
MEM_DQSA_N0	A7	MEM_DQSA_N0	MEM_DQSB_N0	J18	MEM_DQSB_N0
MEM_DQSA_P1	A2	MEM_DQSA_P1	MEM_DQSB_P1	U18	MEM_DQSB_P1
MEM_DQSA_N1	A3	MEM_DQSA_N1	MEM_DQSB_N1	V18	MEM_DQSB_N1
MEM_DQSA_P2	A14	MEM_DQSA_P2	MEM_DQSB_P2	V16	MEM_DQSB_P2
MEM_DQSA_N2	A15	MEM_DQSA_N2	MEM_DQSB_N2	V17	MEM_DQSB_N2
MEM_DQSA_P3	F18	MEM_DQSA_P3	MEM_DQSB_P3	V8	MEM_DQSB_P3
MEM_DQSA_N3	G18	MEM_DQSA_N3	MEM_DQSB_N3	V9	MEM_DQSB_N3
MEM_QKA_P0	A11	MEM_QKA_N0	MEM_QKB_N0	M18	MEM_QKB_P0
MEM_QKA_P1	B18	MEM_QKA_N1	MEM_QKB_N1	V13	MEM_QKB_P1

HLS-180324-B-12

J14B — HiLo EMI - POWER

MEM_VDD

C7	VDD	VEXT = 2.5V	VEXT	L11
C9	VDD		VEXT	L13
C11	VDD		VEXT	M8
C13	VDD		VEXT	M10
D6	VDD		VEXT	M12
D8	VDD		VEXT	M14
D10	VDD	VDD = 1.2(DEFAULT)	VEXT	N7
D12	VDD	(1.2V, 1.25V, 1.35V, 1.8V)	VEXT	N9
D14	VDD		VEXT	N11
E7	VDD		VEXT	N13
E9	VDD		VEXT	P8
E11	VDD		VEXT	P10
E13	VDD		VEXT	P12
F6	VDD		VEXT	P14
F8	VDD			
F10	VDD			

2.5V

VDD DEFAULT IS 1.2V
VDD_1.2V_SET NOT USED.

VDD_1.8V_SET NOT USED
NO SUPPORTED 1.8V EMIF.

VDD_1.25V_SET	G15	VDD_1.2V_SET
VDD_1.35V_SET	E15	VDD_1.25V_SET
VDD_1.5V_SET	J15	VDD_1.35V_SET
	L15	VDD_1.5V_SET
	N16	VDD_1.8V_SET

MEM_VDDQ

F12	VDDQ	2.5V/3.3V (VTT)	J7	
F14	VDDQ	2.5V/3.3V (VTT)	J9	
G7	VDDQ	2.5V/3.3V (VTT)	K6	
G9	VDDQ	VDDQ = 1.2(DEFAULT) 2.5V/3.3V (VTT)	K8	
G11	VDDQ	(1.1V,1.2V, 1.25V, 2.5V/3.3V (VTT)	K10	
G13	VDDQ	1.35V, 1.8V) 2.5V/3.3V (VTT)	K12	
H6	VDDQ	2.5V/3.3V (VTT)	J11	
H8	VDDQ	2.5V/3.3V (VTT)	L7	
H10	VDDQ	2.5V/3.3V (VTT)	L9	
H12	VDDQ	2.5V/3.3V (VTT)		

3.3V

MEM_VREF

N15	VDDQ_1.1V_SET	VREF H14
P16	VDDQ_1.2V_SET	VREF J13
R15	VDDQ_1.25V_SET	VREF K14
N18	VDDQ_1.35V_SET	
P17	VDDQ_1.5V_SET	
P18	VDDQ_1.8V_SET	
R18		

VDDQ_1.25V_SET
VDDQ_1.35V_SET
VDDQ_1.5V_SET

VDDQ DEFAULT IS 1.2V
VDDQ_1.2V_SET NOT USED.

VDDQ_1.1V_SET and VDDQ_1.8V_SET NOT USED
NO SUPPORTED 1.1V or 1.8V EMIF PLANNED.

HLS-180324-B-12

MEM_VDD

C728 10uF, C730 1uF, C729 0.1uF

Place near HILO connector J14 VDD pins

MEM_VDDQ

C731 10uF, C733 1uF, C732 0.1uF

Place near HILO connector J14 VDDQ pins

J14C — HiLo EMI - GND

A1	GND	GND	J10	GND	GND
A5	GND	GND	J12	GND	GND
A9	GND	GND	J14	GND	GND
A13	GND	GND	J17	GND	GND
A17	GND	GND	K3	GND	GND
B3	GND	GND	K7	GND	GND
B7	GND	GND	K9	GND	GND
B11	GND	GND	K11	GND	GND
B15	GND	GND	K13	GND	GND
C1	GND	GND	K15	GND	GND
C5	GND	GND	L1	GND	GND
C6	GND	GND	L5	GND	GND
C8	GND	GND	L8	GND	GND
C10	GND	GND	L10	GND	GND
C12	GND	GND	L12	GND	GND
C14	GND	GND	L14	GND	GND
C17	GND	GND	L17	GND	GND
D3	GND	GND	M3	GND	GND
D7	GND	GND	M7	GND	GND
D9	GND	GND	M9	GND	GND
D11	GND	GND	M11	GND	GND
D13	GND	GND	M13	GND	GND
D15	GND	GND	M15	GND	GND
E1	GND	GND	N1	GND	GND
E5	GND	GND	N5	GND	GND
E6	GND	GND	N8	GND	GND
E8	GND	GND	N10	GND	GND
E10	GND	GND	N12	GND	GND
E12	GND	GND	N14	GND	GND
E14	GND	GND	N17	GND	GND
E17	GND	GND	P3	GND	GND
F3	GND	GND	P6	GND	GND
F7	GND	GND	P7	GND	GND
F9	GND	GND	P9	GND	GND
F11	GND	GND	P11	GND	GND
F13	GND	GND	P13	GND	GND
F15	GND	GND	P15	GND	GND
G1	GND	GND	R1	GND	GND
G5	GND	GND	R5	GND	GND
G6	GND	GND	R9	GND	GND
G8	GND	GND	R10	GND	GND
G10	GND	GND	R13	GND	GND
G12	GND	GND	R17	GND	GND
G14	GND	GND	T3	GND	GND
G17	GND	GND	T7	GND	GND
H3	GND	GND	T11	GND	GND
H7	GND	GND	T15	GND	GND
H9	GND	GND	U1	GND	GND
H11	GND	GND	U5	GND	GND
H13	GND	GND	U9	GND	GND
H15	GND	GND	U13	GND	GND
J1	GND	GND	U17	GND	GND
J5	GND	GND	V3	GND	GND
J6	GND	GND	V7	GND	GND
J8	GND	GND	V11	GND	GND
			V15	GND	GND

HLS-180324-B-12

POWER CONTROL

34	VDD_1.25V_SET
3,34	VDD_1.35V_SET
34	VDD_1.5V_SET
45	VDDQ_1.25V_SET
45	VDDQ_1.35V_SET
45	VDDQ_1.5V_SET

MEMORY INTERFACE

4,8	MEM_ADDR_CMD[31:0]
4	MEM_CLK_P
4	MEM_CLK_N
4	MEM_DQ_ADDR_CMD[8:0]
4	MEM_DQS_ADDR_CMD_P
4	MEM_DQS_ADDR_CMD_N
4,8	MEM_DMA[3:0]
4,8	MEM_DQA[33:0]
4,8	MEM_DQSA_P[3:0]
4,8	MEM_DQSA_N[3:0]
4	MEM_QKA_P[1:0]
4,8	MEM_DMB[3:0]
4,8	MEM_DQB[33:0]
4,8	MEM_DQSB_P[3:0]
4,8	MEM_DQSB_N[3:0]
4	MEM_QKB_P[1:0]

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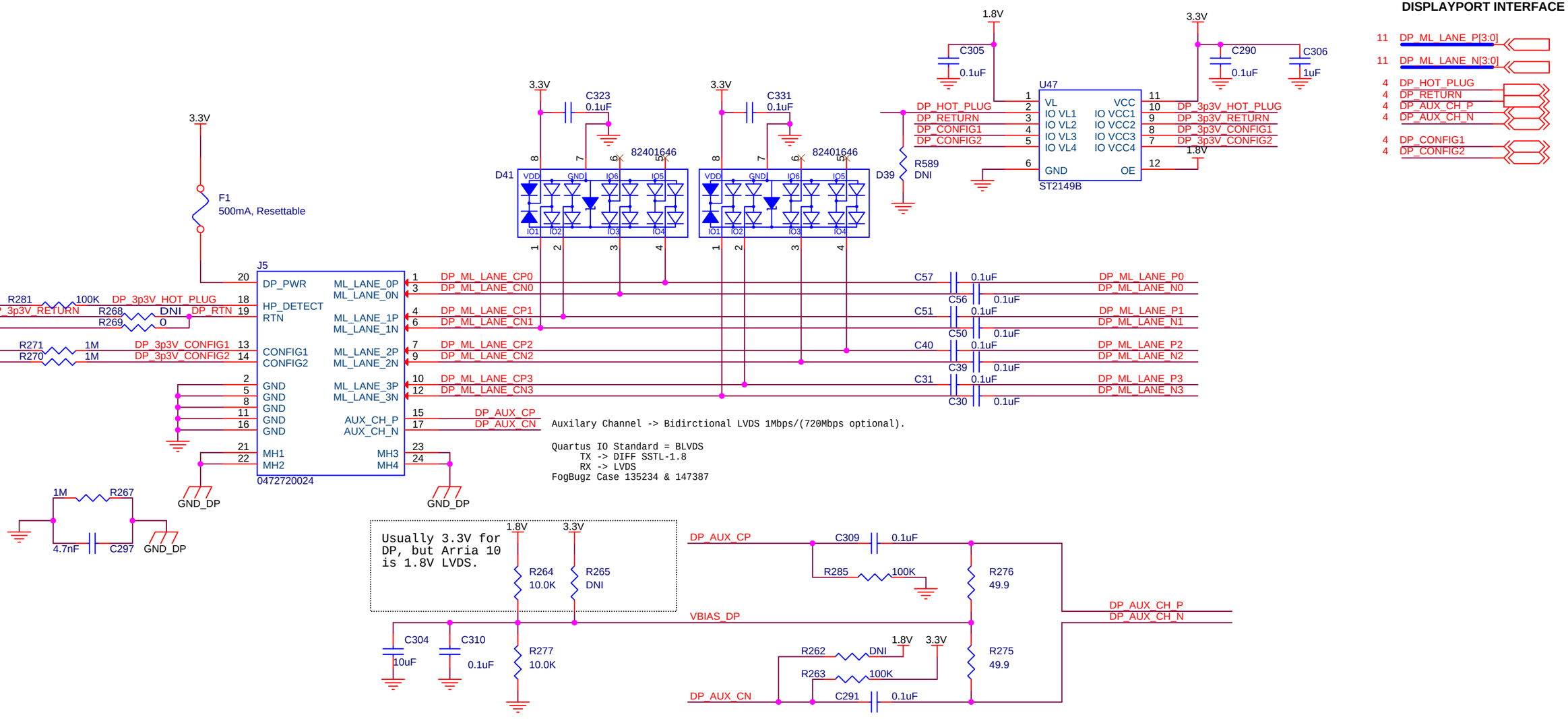
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 17 of 49

Display Port (x4)



1) TX uses diff sstl18 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
2) RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9v.
   a. If the channel is AC couple, then user need to choose the correct Vbias_RX so that Vpin < 1.9v. The spec is 0 – 2v, which is quite wide. Selecting Vbias_Rx at 2v region will cause NF device to have reliability issue.
   b. If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.

Altera Corporation, 101 Innovation Dr., San Jose CA 95134

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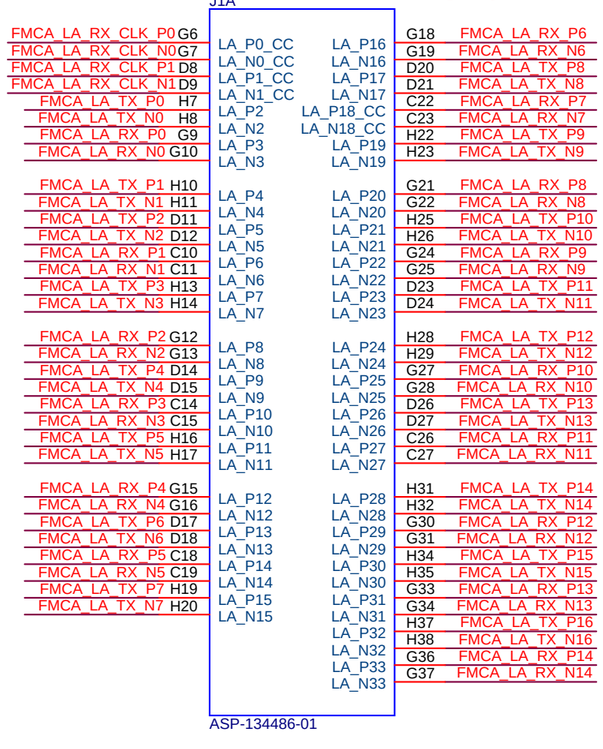
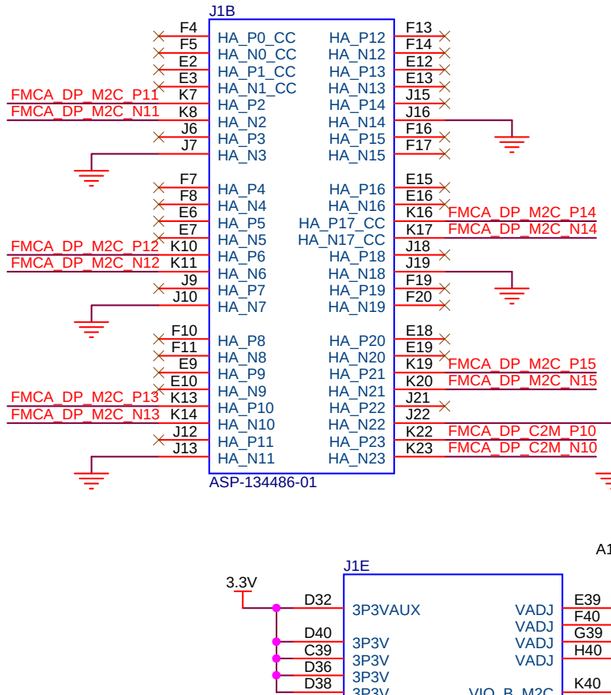
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

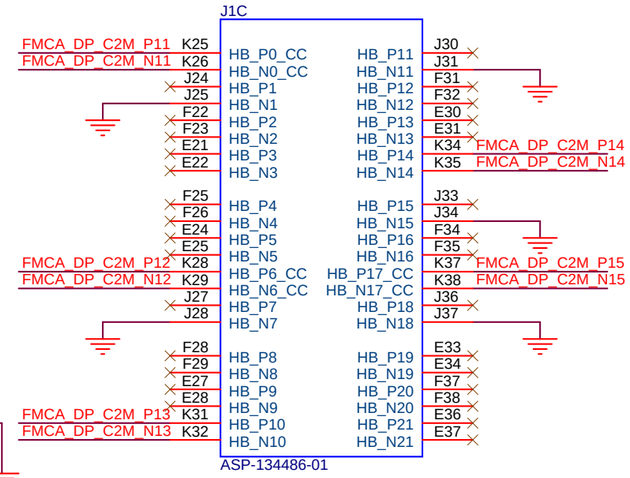
Date: Thursday, May 28, 2015 Sheet 18 of 49

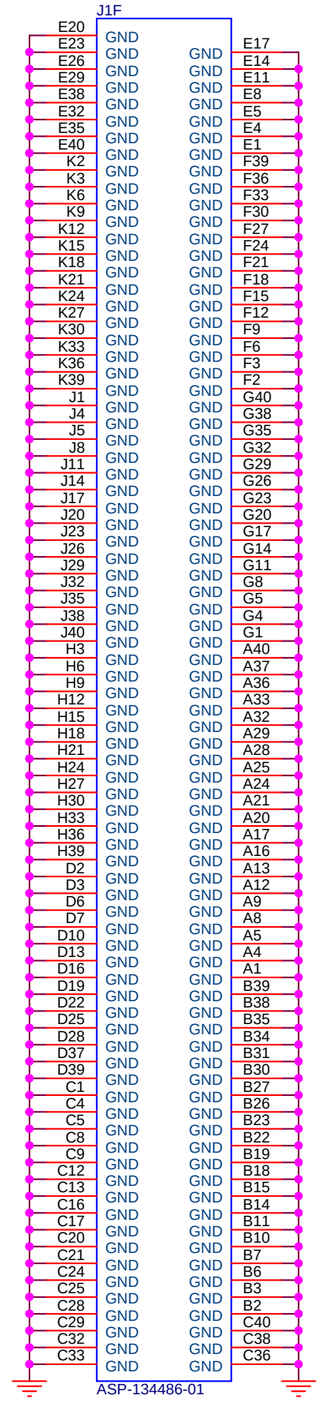
FMC Port A

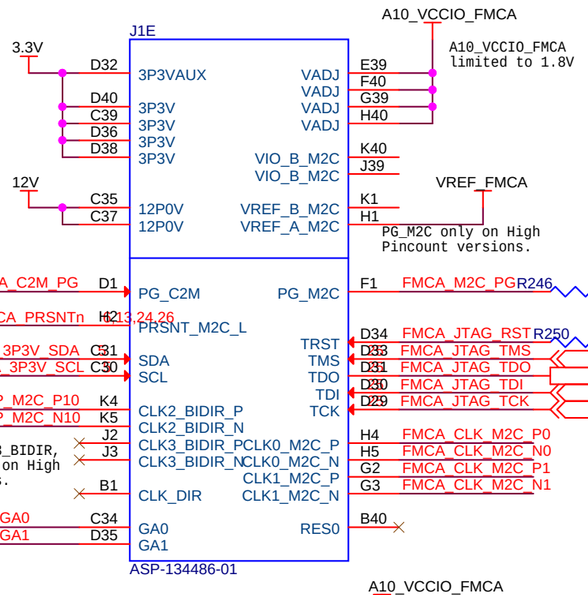
LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.

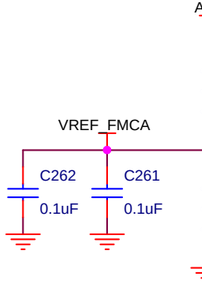


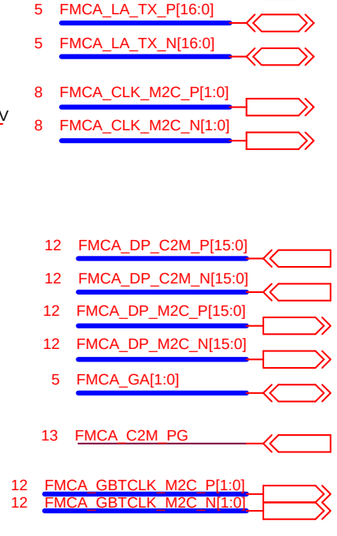












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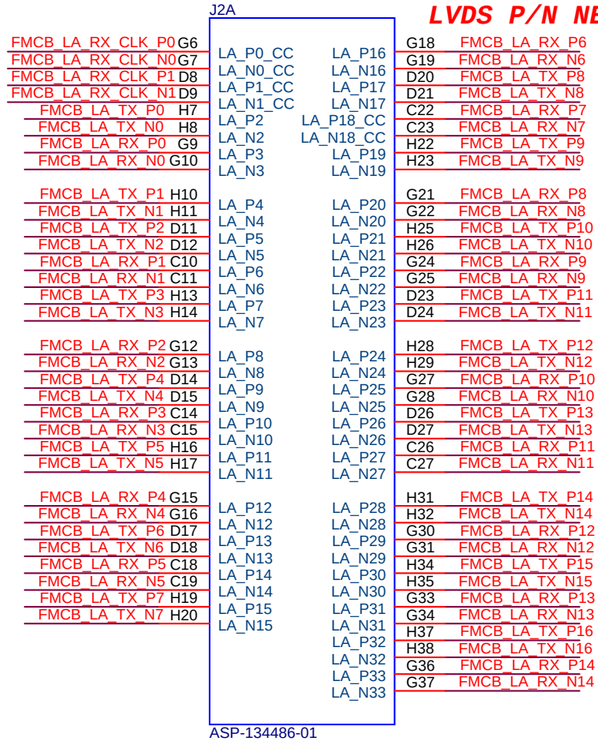
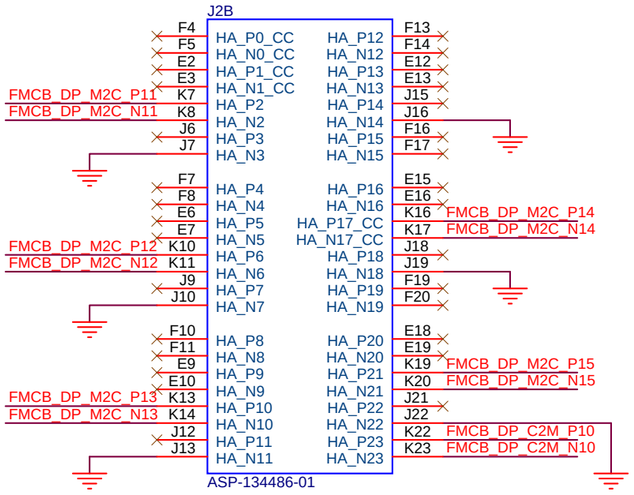
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

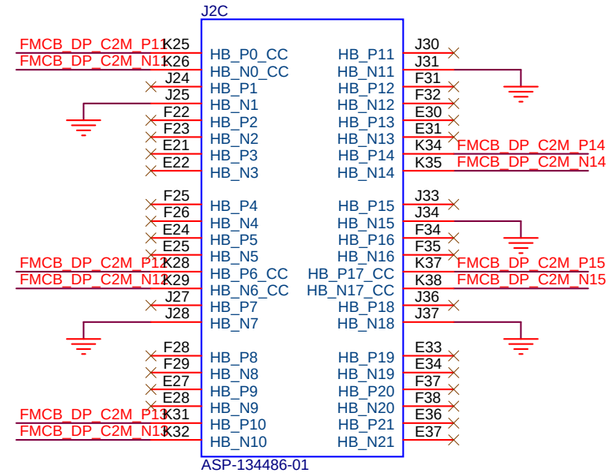
Date: Thursday, May 28, 2015 Sheet 19 of 49

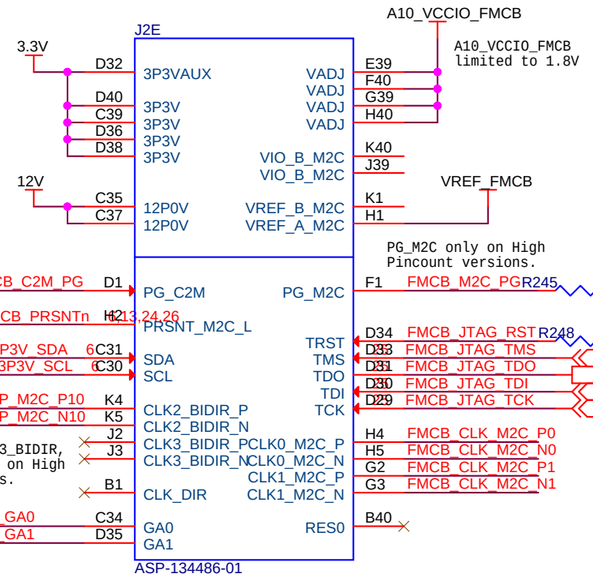
FMC Port B

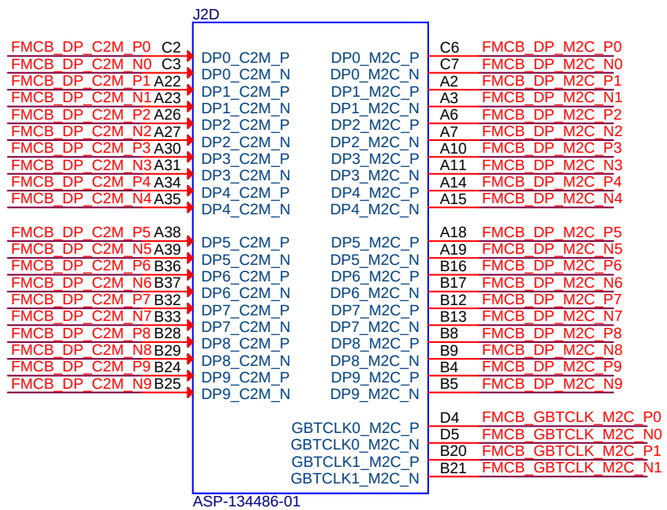
LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.

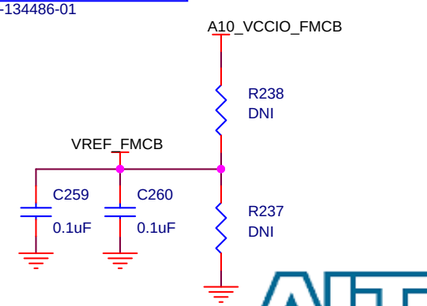


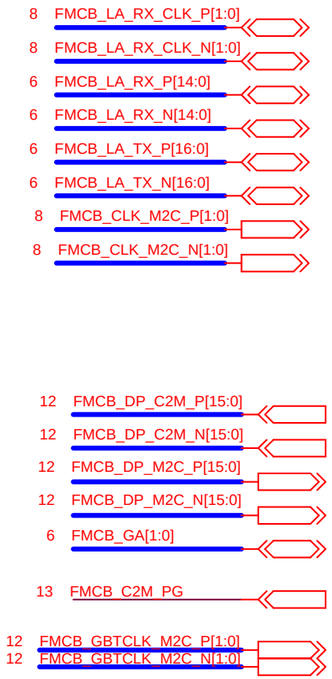


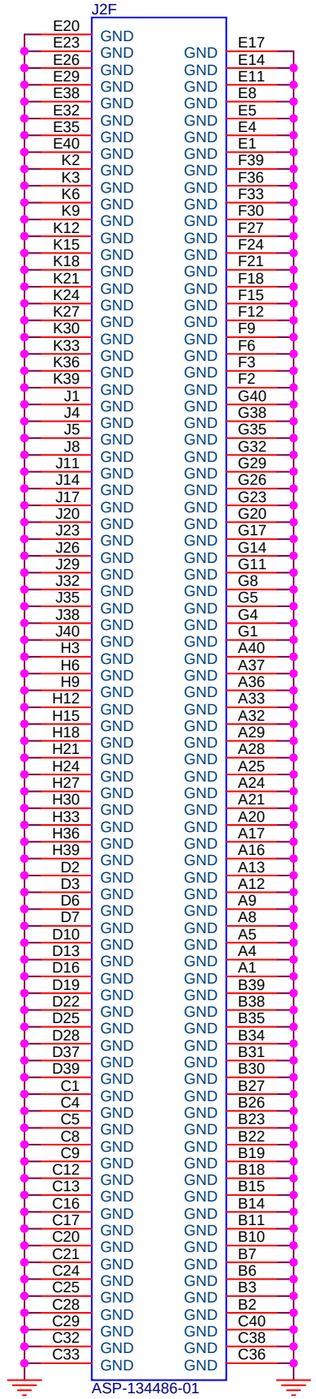












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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 20 of 49

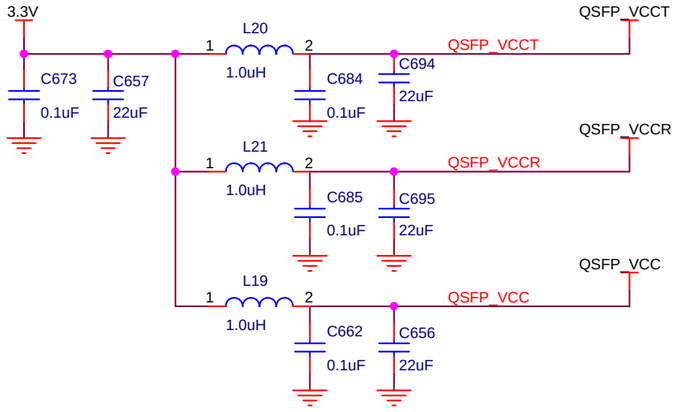
Quad Small Form-factor Pluggable (QSFP) Interface

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

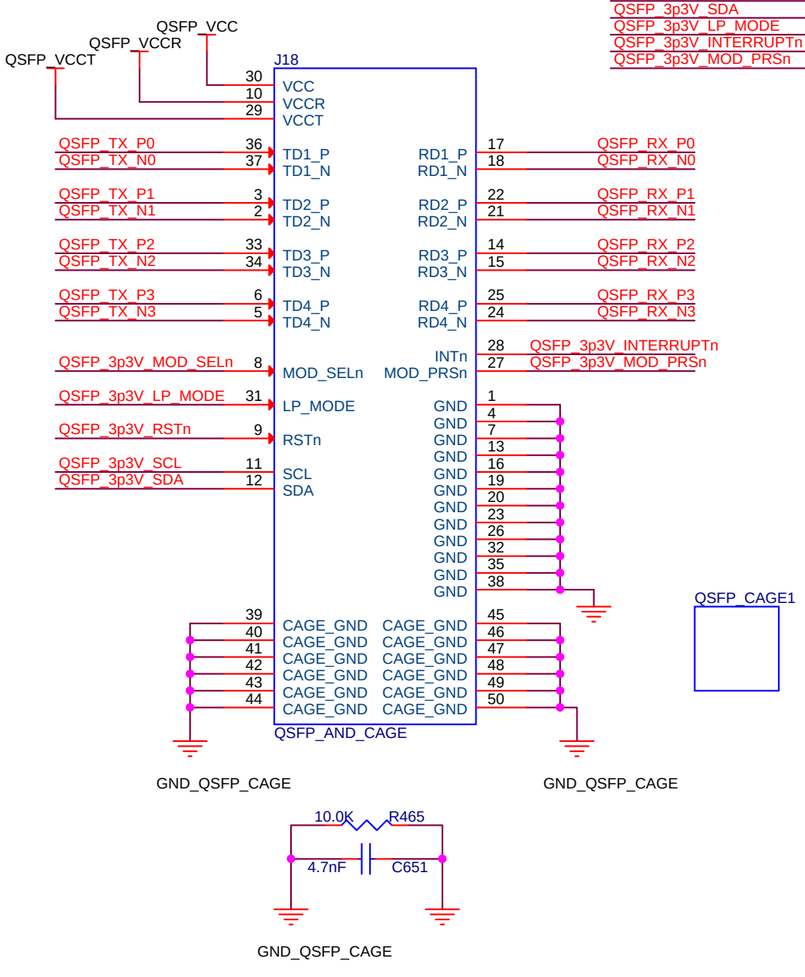
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

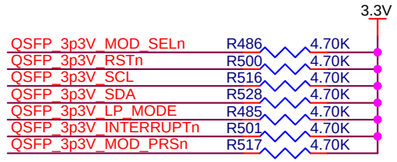
NOTE 3: DC blocking capacitors are in the module for RX and TX.

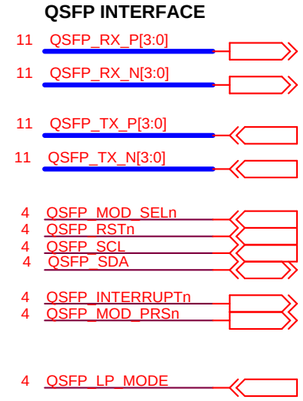
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

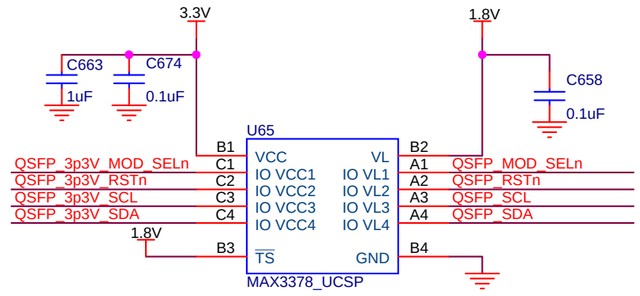


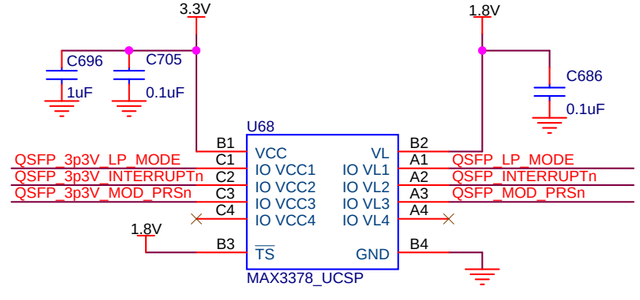
Maximum power is <= 3.5W (1.06 A)
Maximum inrush current = 1.3A











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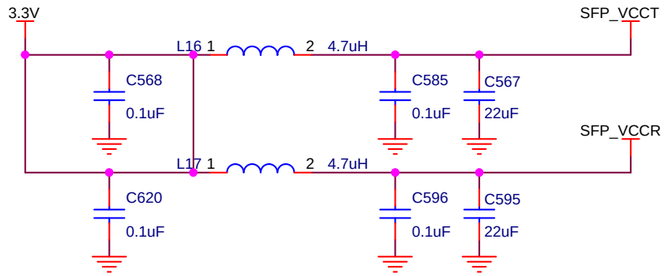
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2
Date: Thursday, May 28, 2015	Sheet 21 of 49	

Small Form Factor Pluggable Plus (SFP+) Connector

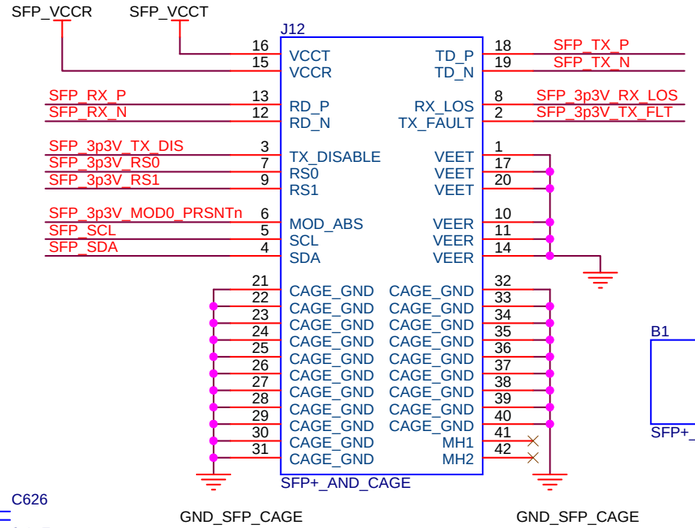
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

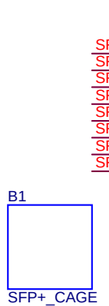
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

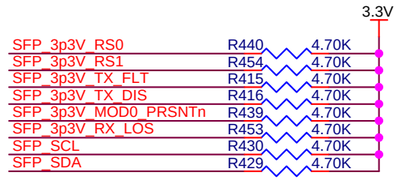
NOTE 3: DC blocking capacitors are in the module for RX and TX.



Level I power is < 1W (0.3 A)
Level II power is < 1.5W (0.45 A)
Level II Instantaneous peak current per rail 600mA



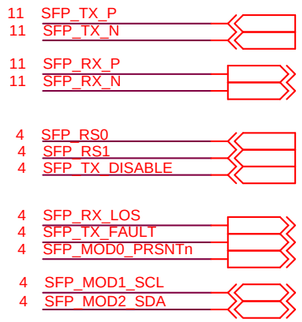




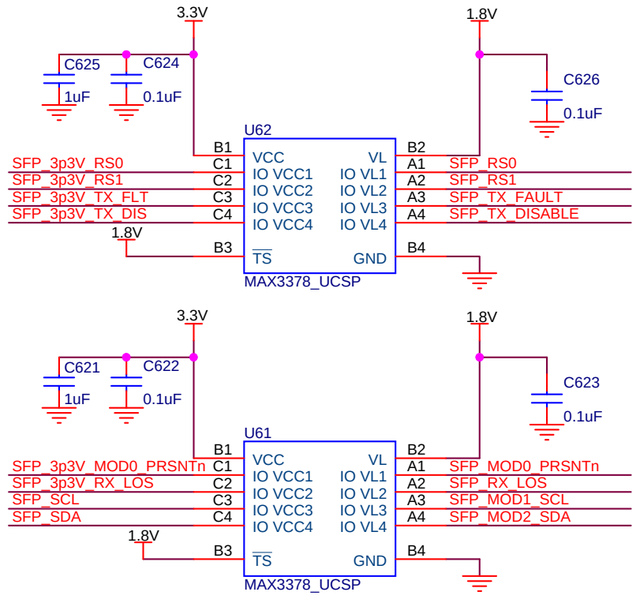
SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

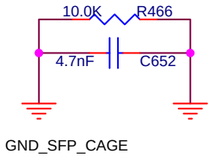
RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s

SFP+ INTERFACE



Optical (SFP+) Transceiver Cage & Connector





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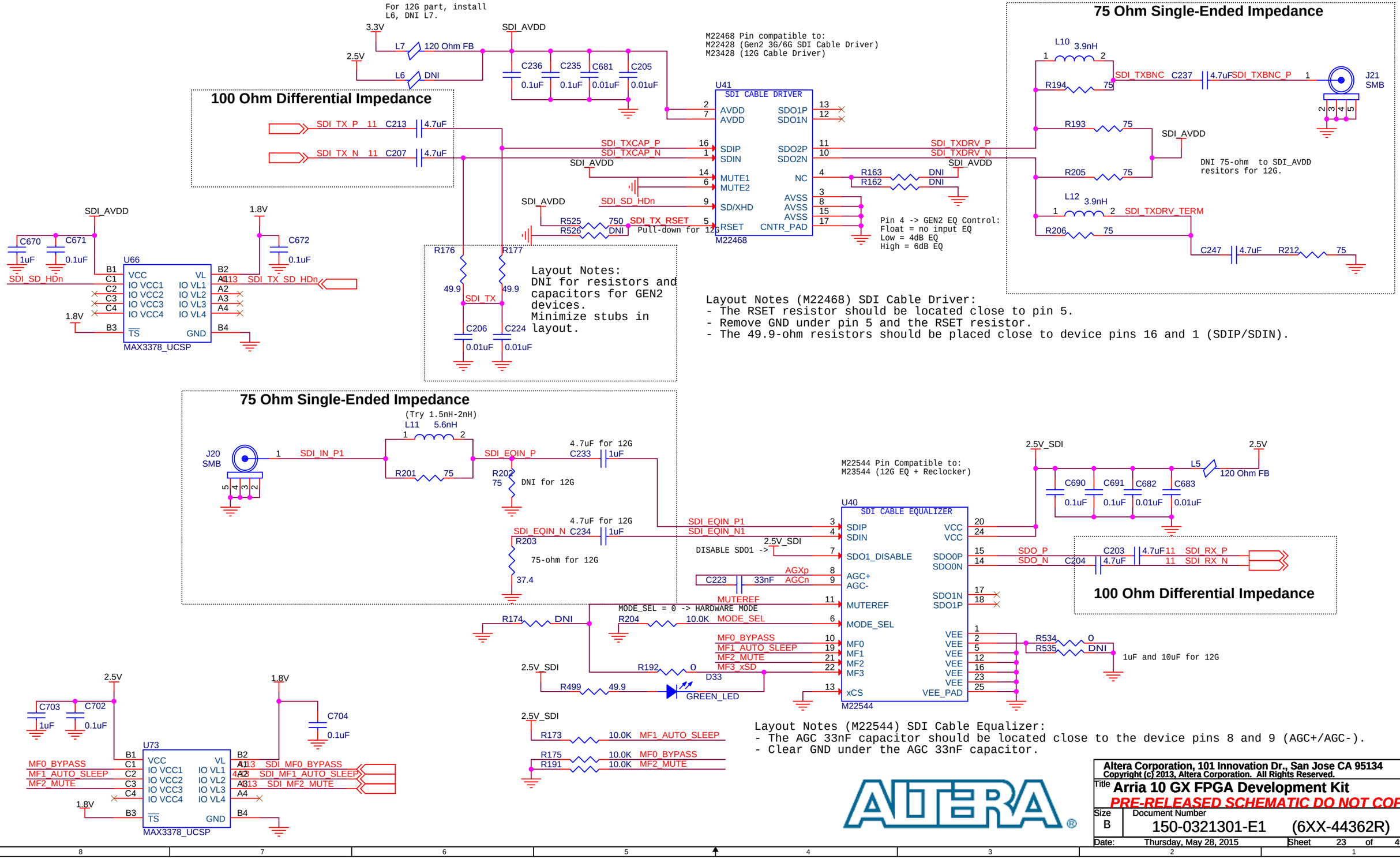
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 22 of 49

SDI Cable Driver, Equalizer, and SMB



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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 23 of 49

User I/O

MAX_ERROR — D16 RED_LED — RES_MAX_ERROR — R243 22.0 — 2.5V
MAX_LOAD — D15 GREEN_LED — RES_MAX_LOAD — R244 22.0 — 2.5V
MAX_CONF_DONE — D17 GREEN_LED — RES_CONF_DONEn — R242 22.0 — 2.5V

FMCA_RX_LED — D2 GREEN_LED — RESn_FMAC_RX_LED — R233 22.0 — 2.5V
FMCA_TX_LED — D1 GREEN_LED — RESn_FMCA_TX_LED — R216 22.0 — 2.5V
FMCA_PRSNTn — R241 22.0 — D11 GREEN_LED — 2.5V

FMCB_RX_LED — D20 GREEN_LED — RESn_FMCB_RX_LED — R254 22.0 — 2.5V
FMCB_TX_LED — D18 GREEN_LED — RESn_FMCB_TX_LED — R253 22.0 — 2.5V
FMCB_PRSNTn — R255 22.0 — D21 GREEN_LED — 2.5V

PCIE_LED_X1 — D34 YELLOW_LED — R551 22.0 — 2.5V
PCIE_LED_X4 — D35 YELLOW_LED — R550 22.0 — 2.5V
PCIE_LED_X8 — D36 YELLOW_LED — R549 22.0 — 2.5V
PCIE_LED_G2 — D37 YELLOW_LED — R548 22.0 — 2.5V
PCIE_LED_G3 — D38 YELLOW_LED — R547 22.0 — 2.5V

2.5V

R217 75	D10 LED_GR	USER_LED_G0	R218 75	USER_LED_R0	
R219 75	D9 LED_GR	USER_LED_G1	R220 75	USER_LED_R1	
R221 75	D8 LED_GR	USER_LED_G2	R222 75	USER_LED_R2	
R223 75	D7 LED_GR	USER_LED_G3	R224 75	USER_LED_R3	
R225 75	D6 LED_GR	USER_LED_G4	R226 75	USER_LED_R4	
R227 75	D5 LED_GR	USER_LED_G5	R228 75	USER_LED_R5	
R229 75	D4 LED_GR	USER_LED_G6	R230 75	USER_LED_R6	
R231 75	D3 LED_GR	USER_LED_G7	R232 75	USER_LED_R7	

PGM_LED0 — D14 GREEN_LED — RESn_PGM_LED0 — R234 22.0 — 2.5V
PGM_LED1 — D13 GREEN_LED — RESn_PGM_LED1 — R235 22.0 — 2.5V
PGM_LED2 — D12 GREEN_LED — RESn_PGM_LED2 — R236 22.0 — 2.5V

S6 PGM_CONFIG — R12 10.0K — 2.5V
S5 PGM_SEL — R11 10.0K — 2.5V
S7 MAX_RESETn — R13 10.0K — 2.5V
S4 CPU_RESETn — R10 10.0K — 1.8V
S3 USER_PB0 — R9 10.0K — 1.8V
S2 USER_PB1 — R8 10.0K — 1.8V
S1 USER_PB2 — R7 10.0K — 1.8V
PB Switch

4,9 CLOCK_SDA
7,13 CPU_RESETn
6 USER_PB[2:0]

PUSH BUTTON INTERFACE
13 PGM_SEL
13 PGM_CONFIG
13 MAX_RESETn

LED INTERFACE
13 PGM_LED[2:0]
13 MAX_ERROR
13 MAX_LOAD
13 MAX_CONF_DONE
13,29 OVERTEMPn
6 USER_LED_G[7:0]
6 USER_LED_R[7:0]

6 FMCA_RX_LED
6 FMCA_TX_LED
6,13,19,26 FMCA_PRSNTn
6 FMCB_RX_LED
6 FMCB_TX_LED
6,13,20,26 FMCB_PRSNTn

7 PCIE_LED_X1
7 PCIE_LED_X4
7 PCIE_LED_X8
7 PCIE_LED_G2
7 PCIE_LED_G3

DIPSWITCH INTERFACE
6 USER_DIPSW[7:0]
9,13 CLK_SEL
13 CLK_ENABLE
13 FACTORY_LOAD
9,13 SI516_FS
4 RZQ_B2K

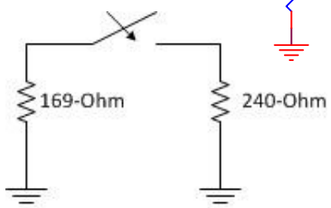
SW2 DIPSWITCH8 — 1.8V

16	1	USER_DIPSW0	RN1A 1	16 10K
15	2	USER_DIPSW1	RN1B 2	15 10K
14	3	USER_DIPSW2	RN1C 3	14 10K
13	4	USER_DIPSW3	RN1D 4	13 10K
12	5	USER_DIPSW4	RN1E 5	12 10K
11	6	USER_DIPSW5	RN1F 6	11 10K
10	7	USER_DIPSW6	RN1G 7	10 10K
9	8	USER_DIPSW7	RN1H 8	9 10K

SW6 DIPSWITCH5 — 2.5V

10	1	CLK_SEL	R518	10.0K
9	2	CLK_ENABLE	R529	10.0K
8	3	SI516_FS	R530	10.0K
7	4	FACTORY_LOAD	R537	10.0K
6	5	RZQ_B2K		

R545 169, 0.1% — R536 240, 0.1%



169 || 240 = 99.17-Ohm

5.0V — J10 — LCD_HEADER
SPI_SS_DISP
I2C_SCL_DISP
I2C_SDA_DISP
B2 2x16 LCD I2C

SPACER1
SPACER2
SPACER3

5.0V — 1.8V
DNI R484, DNI R483, DNI R482
C654 0.1uF, C194 1uF, C193 0.1uF

U64 MAX3378_UCSP

I2C_SCL_DISP	B1 VCC	VL B2	DISP_I2C_SCL
I2C_SDA_DISP	C1 IO VCC1	IO VL1 A1	DISP_I2C_SDA
SPI_SS_DISP	C2 IO VCC2	IO VL2 A2	DISP_SPISS
	C3 IO VCC3	IO VL3 A3	
	C4 IO VCC4	IO VL4 A4	
	B3 TS	GND B4	

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 24 of 49

On-Board USB Blaster II - Part 1

J3
MICRO_USB_CONN
VBUS_5V
FX2_D_N
FX2_D_P
R260 DNI
1M R258
4.7nF C275

U45
TPD2EUSB30

FX2_SDA R16 0 MAX_SDA
3.3V
C282 0.1uF
U2
GND VCC
RESET MR
MAX811
100K R259 FX2_RESETn

U1
CY7C68013A_QFN
AVCC AVCC
VCC VCC VCC VCC VCC VCC VCC
DMINUS DPLUS
IFCLK XTALIN XTALOUT
RESERVED
AGND AGND
GND GND GND GND GND GND
GND EXPOSED_PAD
RESET SCL SDA
WAKEUP
CTL0 CTL1 CTL2
RDY0 RDY1
CLKOUT
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7
FX2_RESETn FX2_SCL FX2_SDA
R14 2.00K R15 2.00K
FX2_WAKEUP
FX2_FLAGA FX2_FLAGB FX2_FLAGC
FX2_SLRDn FX2_SLWRn
IFCLK = 48MHz
FX2_CLK 24M_XTALIN 24M_XTALOUT
FX2_PA0 FX2_PA1 FX2_PA2 FX2_PA3 FX2_PA4 FX2_PA5 FX2_PA6 FX2_PA7
FX2_PB0 FX2_PB1 FX2_PB2 FX2_PB3 FX2_PB4 FX2_PB5 FX2_PB6 FX2_PB7
FX2_PD0 FX2_PD1 FX2_PD2 FX2_PD3 FX2_PD4 FX2_PD5 FX2_PD6 FX2_PD7

Y1 24.00MHz
C265 12pF
C264 12pF

VBUS_5V R257 10.0K FX2_WAKEUP
R256 20.0K C273 0.1uF

PLACE NEAR CY7C68013A
3.3V
C267 C268 C271 C274 C284 C266 C270 C283
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

U49A
MAX II BANK1
EPM1270_M256FBGA
IOB1_1 IOB1_2 IOB1_3 IOB1_4 IOB1_5 IOB1_6 IOB1_7 IOB1_8
IOB1_9 IOB1_10 IOB1_11 IOB1_12 IOB1_13 IOB1_14 IOB1_15 IOB1_16
IOB1_17 IOB1_18 IOB1_19 IOB1_20 IOB1_21 IOB1_22 IOB1_23 IOB1_24
IOB1/GCLK0 IOB1/GCLK1
IOB1_25 IOB1_26 IOB1_27 IOB1_28 IOB1_29 IOB1_30 IOB1_31 IOB1_32
IOB1_33 IOB1_34 IOB1_35 IOB1_36 IOB1_37 IOB1_38 IOB1_39 IOB1_40
IOB1_41 IOB1_42 IOB1_43 IOB1_44 IOB1_45 IOB1_46 IOB1_47 IOB1_48 IOB1_49
TCK TDI TDO TMS
FX2_SCL FX2_PB0 FX2_PB1 FX2_PB7 FX2_PB5 FX2_PB6 FX2_FLAGC FX2_FLAGA FX2_CLK FX2_PA0
FX2_FLAGB FX2_PA1 FX2_PA4 FX2_PA2 FX2_PA3 FX2_PA6 FX2_PA5
C_USB_MAX_TCK C_USB_MAX_TDI C_USB_MAX_TDO C_USB_MAX_TMS
R23 R25 R26 R24 0
FX2_PD0 FX2_PD2 FX2_PD3 FX2_PD1

ARRIA 10 USB INTERFACE
8 USB_FPGA_CLK
MAX V USB INTERFACE
13 USB_M5_CLK
JTAG INTERFACE
19 FMCA_JTAG_TCK
19 FMCA_JTAG_TMS
19 FMCA_JTAG_TDO
19 FMCA_JTAG_TDI
20 FMCB_JTAG_TCK
20 FMCB_JTAG_TMS
20 FMCB_JTAG_TDO
20 FMCB_JTAG_TDI

CAN WE USE MAX II TO LEVEL TRANSLATE USB_CLK?
1.8V
0.1uF C506
U58
VL VCC
IO_VL1 IO_VL2 IO_VL3 IO_VL4
IO_VCC1 IO_VCC2 IO_VCC3 IO_VCC4
EN GND
MAX13042
3.3V
0.1uF C505
1uF C504
USB_FPGA_CLK USB_M5_CLK
FX2_CLK

U49D
MAX II BANK4
EPM1270_M256FBGA
IOB4_1 IOB4_2 IOB4_3 IOB4_4 IOB4_5 IOB4_6 IOB4_7 IOB4_8
IOB4_9 IOB4_10 IOB4_11 IOB4_12 IOB4_13 IOB4_14 IOB4_15 IOB4_16
IOB4_17 IOB4_18 IOB4_19 IOB4_20 IOB4_21 IOB4_22 IOB4_23 IOB4_24
IOB4/DEV_CLRn IOB4/DEV_OE
IOB4_25 IOB4_26 IOB4_27 IOB4_28 IOB4_29 IOB4_30 IOB4_31 IOB4_32
IOB4_33 IOB4_34 IOB4_35 IOB4_36 IOB4_37 IOB4_38 IOB4_39 IOB4_40
IOB4_41 IOB4_42 IOB4_43 IOB4_44 IOB4_45 IOB4_46 IOB4_47 IOB4_48
IOB4_49 IOB4_50 IOB4_51
FX2_RESETn FMCA_JTAG_TDO
FX2_PA7 FX2_SLWRn FX2_SLRDn FMCA_JTAG_TMS FMCA_JTAG_TDI FMCA_JTAG_TCK FMCB_JTAG_TDO FMCB_JTAG_TMS FMCB_JTAG_TDI FMCB_JTAG_TCK FX2_PB4 FX2_PB3 FX2_PB2 FX2_PD5 FX2_PD4 FX2_PD7 FX2_PD6 MAX_SDA

3.3V
R502 1.00K C_USB_MAX_TCK
R531 1.00K C_USB_MAX_TDO
C_USB_MAX_TMS
C_USB_MAX_TDI
J23
DNI

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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 25 of 49

On-Board USB Blaster II - Part 2

SW4
DIPSWITCH4
OPEN
8 7 6 5 — 1 2 3 4
A10_JTAG_BYPASSn R473 10.0K
M5_JTAG_BYPASSn R474 10.0K
FMCA_JTAG_BYPASSn R487 10.0K
FMCB_JTAG_BYPASSn R488 10.0K
1.8V

Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

U49B
MAX II
BANK2
EPM1270_M256FBGA

JTAG_RX	A1	IOB2_1	IOB2_25	B14	USB_CFG7
USB_CFG14	A10	IOB2_2	IOB2_26	B15	USB_CFG1
USB_CFG11	A11	IOB2_3	IOB2_27	B16	USB_CFG4
USB_CFG10	A12	IOB2_4	IOB2_28	B17	USB_CFG8
USB_CFG13	A13	IOB2_5	IOB2_29	B18	USB_CFG0
USB_CFG12	A14	IOB2_6	IOB2_30	B19	FMCB_PRSNTn
USB_CFG5	A15	IOB2_7	IOB2_31	B2	JTAG_TX
USB_CFG9	A16	IOB2_8	IOB2_32	B3	FMCB_JTAG_BYPASSn
USB_CFG2	A17	IOB2_9	IOB2_33	B4	
USB_CFG6	A18	IOB2_10	IOB2_34	B5	
USB_CFG3	A19	IOB2_11	IOB2_35	B6	
SC_RX	A2	IOB2_12	IOB2_36	B7	
USB_DATA3	A20	IOB2_13	IOB2_37	B8	
C_JTAG_TDO	A3	IOB2_14	IOB2_38	B9	
SC_TX	A4	IOB2_15	IOB2_39	C14	
FMCA_PRSNTn	A5	IOB2_16	IOB2_40	C15	
M5_JTAG_TDI	A6	IOB2_17	IOB2_41	C16	
M5_JTAG_TDO	A7	IOB2_18	IOB2_42	C17	A10_JTAG_BYPASSn
M5_JTAG_TMS	A8	IOB2_19	IOB2_43	C5	
M5_JTAG_TCK	A9	IOB2_20	IOB2_44	C6	
B10		IOB2_21	IOB2_45	C7	
B11		IOB2_22	IOB2_46	D13	
B12		IOB2_23	IOB2_47	D14	
B13		IOB2_24	IOB2_48	D15	FMCB_JTAG_MASTERn
			IOB2_49	D16	
			IOB2_50	D5	FMCA_JTAG_MASTERn
			IOB2_51	D6	
			IOB2_52	D7	
			IOB2_53	D8	FMCA_JTAG_BYPASSn

1.8V
R43 10.0K
R44 10.0K
R45 1.00k

1.8V
R33 1.00k USB_SCL
R27 1.00k USB_SDA
R39 1.00k USB_FULL
R40 1.00k USB_EMPTY

R42 DNI FMCA_JTAG_MASTERn
R46 DNI FMCB_JTAG_MASTERn

U49C
MAX II
BANK3
EPM1270_M256FBGA

USB_DATA2	B20	IOB3_1	IOB3_25	J20	USB_DATA0
M5_JTAG_BYPASSn	C18	IOB3_2	IOB3_26	K19	
	C19	IOB3_3	IOB3_27	K20	USB_RDn
USB_EMPTY	C20	IOB3_4	IOB3_28	L19	C_JTAG_TCK
	D17	IOB3_5	IOB3_29	M19	USB_DATA5
	D18	IOB3_6	IOB3_30	N17	
	D19	IOB3_7	IOB3_31	N19	
USB_ADDR0	D20	IOB3_8	IOB3_32	N20	USB_DATA7
	E17	IOB3_9	IOB3_33	P17	
	E18	IOB3_10	IOB3_34	P18	
C_JTAG_TMS	E19	IOB3_11	IOB3_35	P19	
USB_FULL	E20	IOB3_12	IOB3_36	P20	A10_JTAG_TDI
	F17	IOB3_13	IOB3_37	R17	
	F18	IOB3_14	IOB3_38	R18	
	F19	IOB3_15	IOB3_39	R19	
USB_ADDR1	F20	IOB3_16	IOB3_40	R20	A10_JTAG_TCK
	G17	IOB3_17	IOB3_41	T17	
	G18	IOB3_18	IOB3_42	T18	
C_JTAG_TDI	G19	IOB3_19	IOB3_43	T19	USB_WRn
USB_OEn	G20	IOB3_20	IOB3_44	T20	USB_SCL
	H17	IOB3_21	IOB3_45	U17	
	H19	IOB3_22	IOB3_46	U18	
USB_DATA1	H20	IOB3_23	IOB3_47	U19	
USB_DISABLEn	J19	IOB3_24	IOB3_48	U20	USB_RESETn
			IOB3_49	V19	
			IOB3_50	V20	USB_SDA
			IOB3_51	W19	
USB_DATA6	M20	IOB3/GCLK2	IOB3_52	W20	A10_JTAG_TMS
USB_DATA4	L20	IOB3/GCLK3	IOB3_53	Y20	A10_JTAG_TDO

1.8V
R30 10.0K A10_JTAG_TDI
R32 1.00k A10_JTAG_TCK
1.8V
R31 10.0K A10_JTAG_TMS

ARRIA 10 USB INTERFACE

5	USB_DATA[7:0]
5	USB_ADDR[1:0]
8	USB_FULL
8	USB_EMPTY
8	USB_SCL
8	USB_SDA
5	USB_RESETn
5	USB_OEn
5	USB_RDn
5	USB_WRn

MAX V USB INTERFACE

13	USB_CFG[14:0]

JTAG INTERFACE

7	A10_JTAG_TCK
7	A10_JTAG_TMS
7	A10_JTAG_TDO
7	A10_JTAG_TDI
13	M5_JTAG_TCK
13	M5_JTAG_TMS
13	M5_JTAG_TDO
13	M5_JTAG_TDI

6,13,19,24	FMCA_PRSNTn
6,13,20,24	FMCB_PRSNTn

USB Blaster Programming Header
(uses JTAG mode only)

2.5V
R504 1.00k USB_DISABLEn
J17
2X5_100mil

2	1	1	J17_JTAG_TCK
4	2	3	J17_JTAG_TDO
6	3	5	J17_JTAG_TMS
8	4	7	
10	5	9	J17_JTAG_TDI
	6		
	7		
	8		
	9		
	10		

R477 1.00k 2.5V
R467 1.00k

J17_JTAG_TCK R491 DNI C664 DNI
R503 1.00k

U49E
MAX II
Power
EPM1270_M256FBGA

J4				K4	
U12	GNDINT	VCCINT		U11	
M17	GNDINT	VCCINT		L17	
D12	GNDINT	VCCINT		D11	
	GNDINT	VCCINT			
H3				K3	3.3V
J3	GNDIO	VCCIO1		L3	
M4	GNDIO	VCCIO1		L4	
N3	GNDIO	VCCIO1		M3	
U9	GNDIO	VCCIO1			
V8	GNDIO			C9	1.8V
V9	GNDIO	VCCIO2		C10	
V13	GNDIO	VCCIO2		D10	
H18	GNDIO	VCCIO2		C11	
J17	GNDIO	VCCIO2			
N18	GNDIO			J18	1.8V
C8	GNDIO	VCCIO3		K17	
D9	GNDIO	VCCIO3		K18	
C12	GNDIO	VCCIO3		L18	
C13	GNDIO	VCCIO3			
M18	GNDIO			U10	3.3V
	GNDIO	VCCIO4		V10	
		VCCIO4		V11	
		VCCIO4		V12	
		VCCIO4			

2.5V
0.1uF C741
0.1uF C742
1uF C740

U76
MAX13042

	B2	VL	VCC	B1	
C_JTAG_TCK	C4	IO_VL1	IO_VCC1	A4	J17_JTAG_TCK
C_JTAG_TDO	C3	IO_VL2	IO_VCC2	A3	J17_JTAG_TDO
C_JTAG_TMS	C2	IO_VL3	IO_VCC3	A2	J17_JTAG_TMS
C_JTAG_TDI	C1	IO_VL4	IO_VCC4	A1	J17_JTAG_TDI
1.8V					
	B3	EN	GND	B4	

1.8V

JTAG_RX	D22	RESn_JTAG_RX	R314 22.0
JTAG_TX	D23	RESn_JTAG_TX	R313 22.0
SC_RX	D24	RESn_SC_RX	R312 22.0
SC_TX	D25	RESn_SC_TX	R311 22.0

GREEN_LED

PLACE NEAR MAX II (U25)

2.5V	C18	C43	3.3V C19	C17	3.3V C32 C33
	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF 0.1uF
1.8V	C42	C41	1.8V C34	C35	
	0.1uF	0.1uF	0.1uF	0.1uF	

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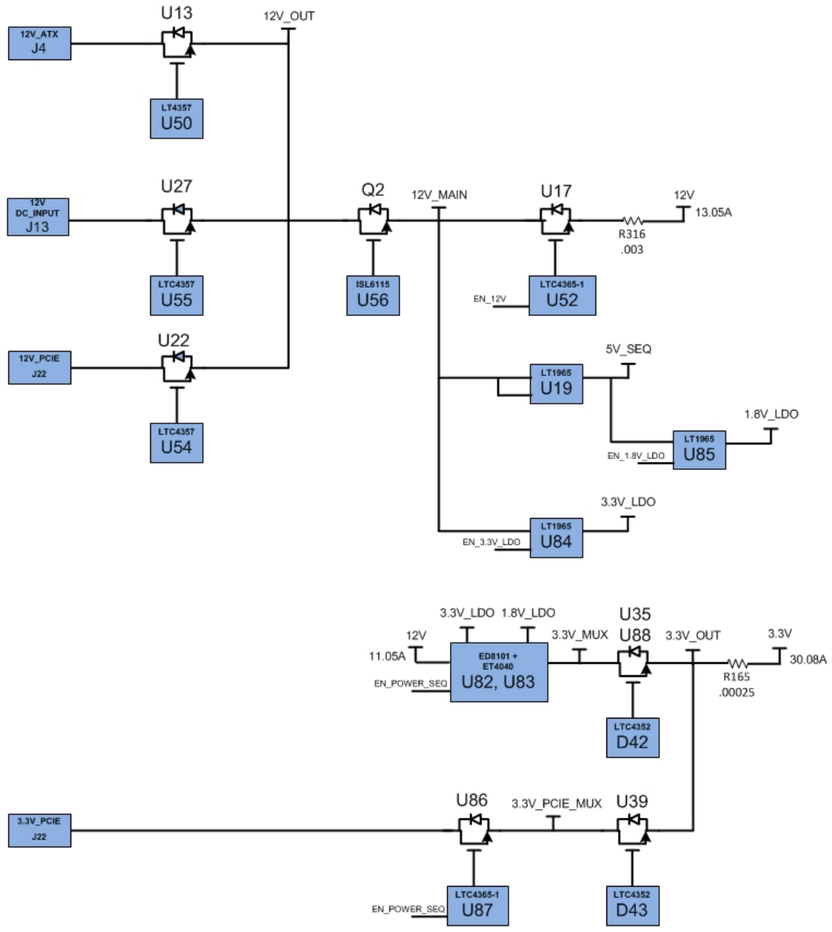
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 26 of 49

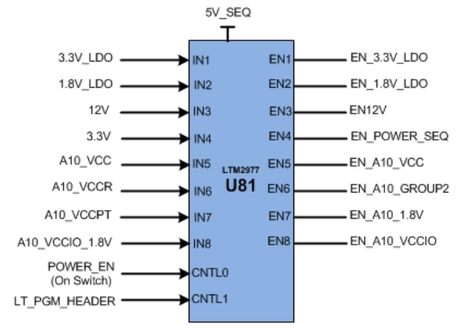
Power Tree

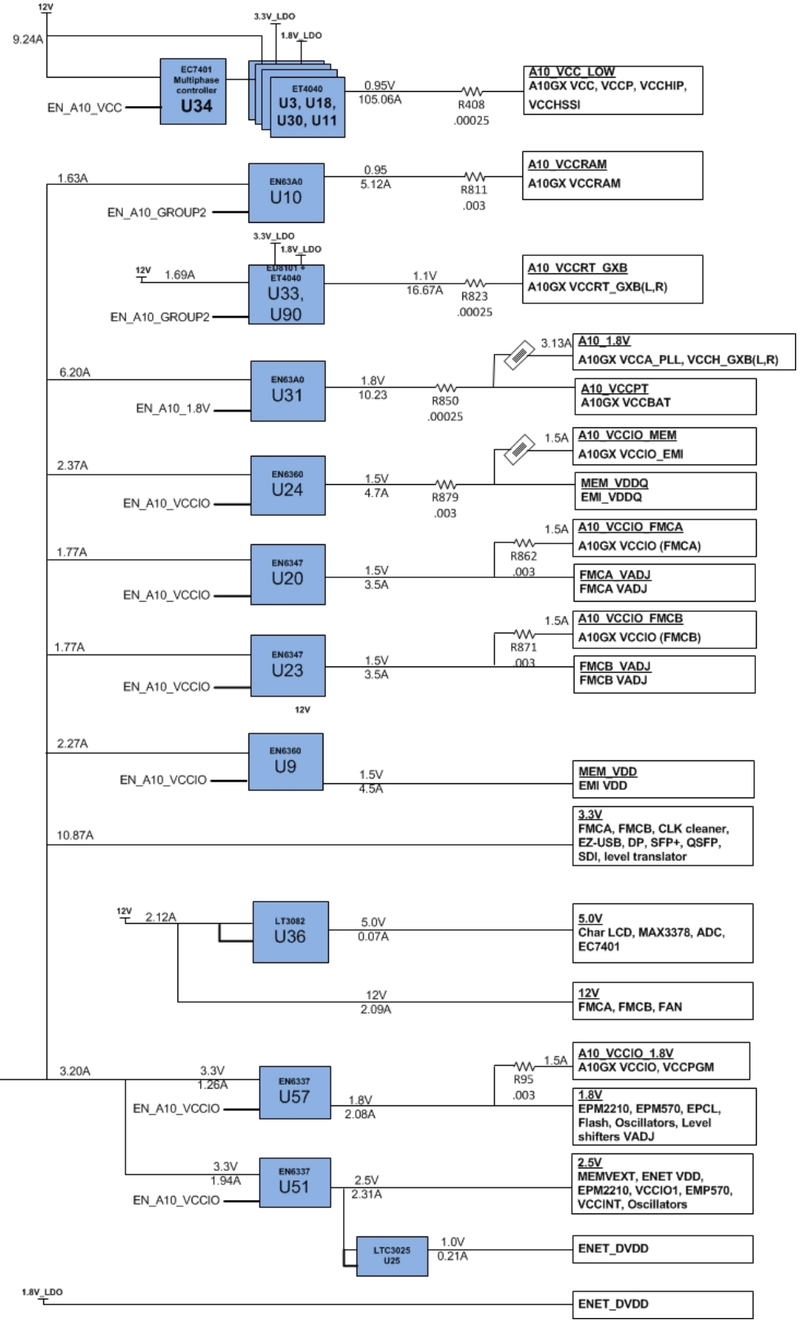


Power UP Sequencing:
1) EN_3.3V_LDO
2) EN_1.8V_LDO
3) EN_12V
4) EN_POWER_SEQ
5) EN_A10_VCC
6) EN_A10_GROUP2
7) EN_A10_1.8V
8) EN_A10_VCCIO

Power DOWN Sequencing:
1) DISABLE A10_VCCIO
2) DISABLE A10_1.8V
3) DISABLE A10_GROUP2
4) DISABLE A10_VCC
5) DISABLE POWER_SEQ
6) DISABLE 12V
7) DISABLE 1.8V_LDO
8) DISABLE 3.3V_LDO

PCIe Component Height Restrictions:
-Top Side (Max): 14.47mm
-Bottom Side (Max) 2.67mm





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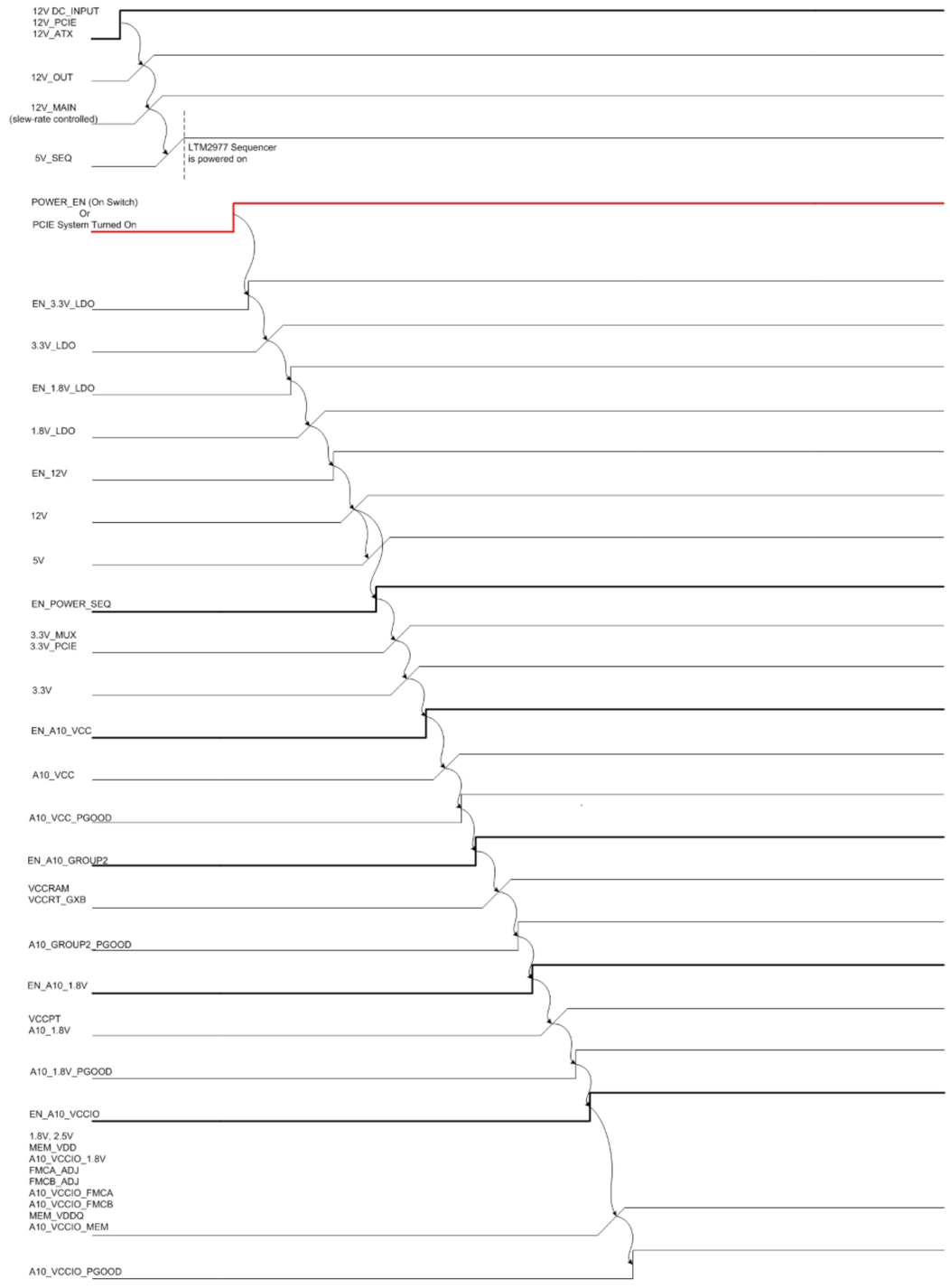
Size	Document Number	Rev
C	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 27 of 49

Power-On Sequencing
(Power-Off is reverse of Power-On)



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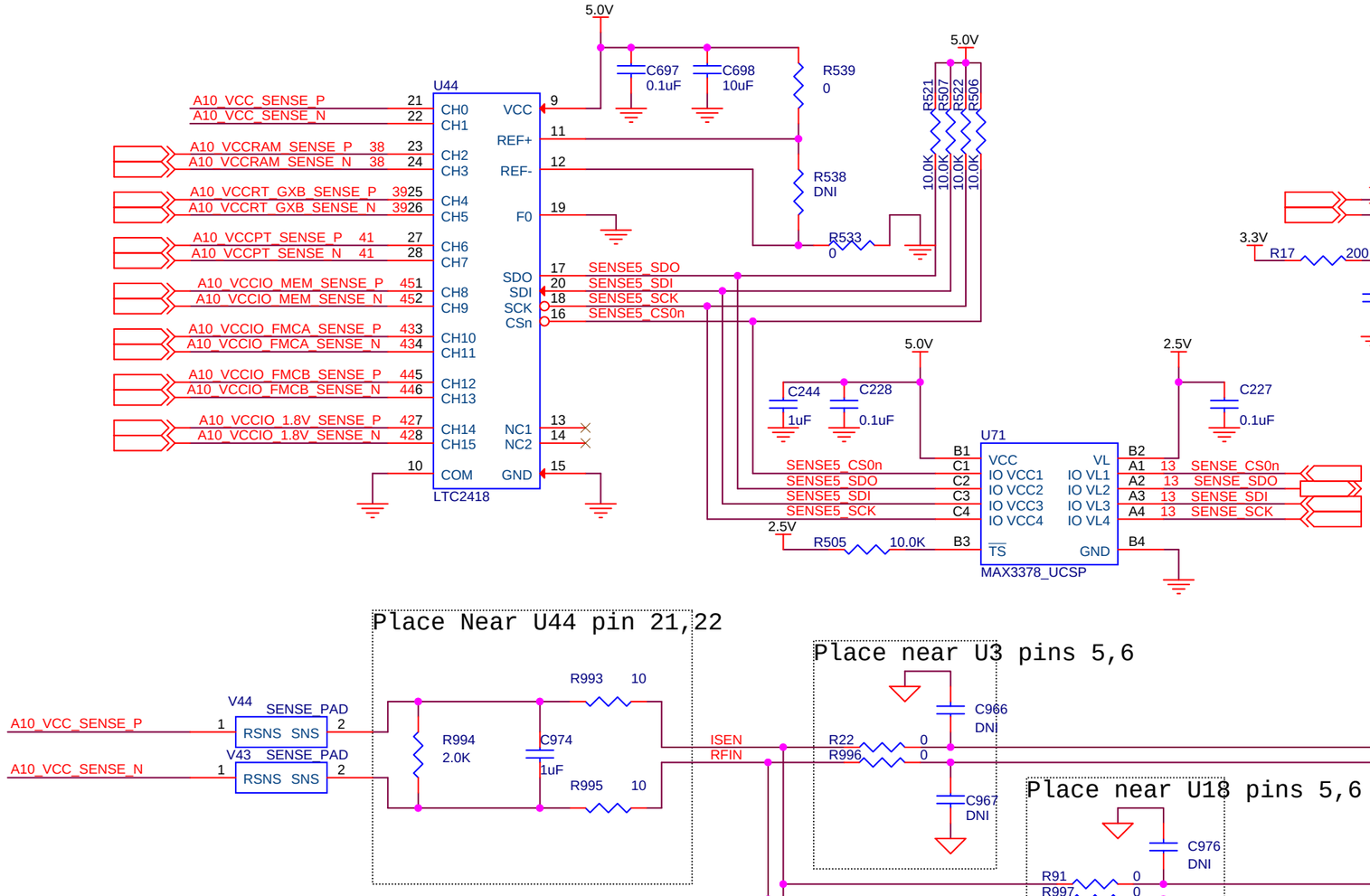
C	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 28 of 49

Voltage &Temp Sense



Title: **Arria 10 GX FPGA Development Kit**

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 29 of 49

Power Sequence Controller

12V_OUT
R735 100K
4V
R740 49.9K

3.3V_LDO
1.8V_LDO
3.3V
A10_VCC
A10_VCCRT_GXB
A10_VCCPT
A10_VCCIO_1.8V

R733 200
R734 200 C804 0.1uF C805 0.1uF
R736 200
R737 200 C806 0.1uF C807 0.1uF
R738 200
R739 200 C809 0.1uF C810 0.1uF
R741 200
R742 200 C811 0.1uF C812 0.1uF
R743 200
R744 200 C813 0.1uF C814 0.1uF
R745 200
R746 200 C815 0.1uF C816 0.1uF
R747 200
R748 200 C817 0.1uF C818 0.1uF
R749 200
R754 200 C819 0.1uF C820 0.1uF

these GND connections needs to be placed close to a GND pin of the BGA!

5V_SEQ

U81

14	VIN_SNS	VIN_EN	12
36	VSENSEP0	REFP	34
37	VSENSEM0	REFM	35
42	VSENSEP1	NC	13
43	VSENSEM1		
46	VSENSEP2	VDACP0	39
47	VSENSEM2	VDACM0	38
48	VSENSEP3	VDACP1	40
49	VSENSEM3	VDACM1	41
52	VSENSEP4	VDACP2	44
53	VSENSEM4	VDACM2	45
62	VSENSEP5	VDACP3	50
63	VSENSEM5	VDACM3	51
64	VSENSEP6	VDACP4	55
1	VSENSEM6	VDACM4	54
2	VSENSEP7	VDACP5	56
3	VSENSEM7	VDACM5	57
		VDACP6	59
		VDACM6	58
		VDACP7	60
		VDACM7	61
28	SCL	VOUT_EN0	4
27	SDA	VOUT_EN1	5
32	ASEL0	VOUT_EN2	6
33	ASEL1	VOUT_EN3	7
30	CONTROL0	VOUT_EN4	8
31	CONTROL1	VOUT_EN5	9
22	WDI/RESET	VOUT_EN6	10
		VOUT_EN7	11
23	FAULTB00		
24	FAULTB01		
25	FAULTB10		
26	FAULTB11		
21	SHARE_CLK	ALERTB	29
		PWRGD	20
19	WP	VPWR	15
65	E-PAD	VDD25	18
		VDD33_OUT	16
		VDD33_IN	17
	GND PAD		

LTC2977

POWER_EN
LT_SCL
LT_SDA
PM_ASEL0
PM_ASEL1
PM_CNTL1
PM_FAULTB00
PM_FAULTB01
PM_FAULTB10
PM_FAULTB11
PM_SHARE_CLK

C808 0.1uf

VDD33

C821 0.1uf
C822 0.1uf
C823 0.1uf

LTC2977
Address Select = 7'h5C

VDD33

R722 5.49K
R723 10K
R724 10K
R725 10K
R726 10K
R727 10K
R728 10K
R729 10K
R730 10K
R731 10K
R732 10K

PM_SHARE_CLK
PM_CNTL1
PM_RSTn
PM_ALERT
PM_PWRGD
PM_FAULTB00
PM_FAULTB01
PM_FAULTB10
PM_FAULTB11
LT_SDA
LT_SCL

VDD33

R750 10K
R755 10K
R751 10K
R756 10K
R757 10K
R752 10K
R758 10K
R753 10K

EN_3.3V_LDO
EN_1.8V_LDO
EN_12V
EN_POWER_SEQ
EN_A10_VCC
EN_A10_GROUP2
EN_A10_1.8V
EN_A10_VCCIO

EN_3.3V_LDO 32,49
EN_1.8V_LDO 32,49
EN_12V 31,49
EN_POWER_SEQ 31,32
EN_A10_VCC 35
EN_A10_GROUP2 38,39
EN_A10_1.8V 41
EN_A10_VCCIO 34,42,43,44,45,49

POWER_EN
POWER_EN 31

PM_ALERT
PM_PWRGD

SENSE_SMB_CLK 13,29
SENSE_SMB_DATA 13,29
R1000 0
R1001 0

I2C Interface

J24 2x6HDR

1	1	2	2
3	3	4	4 LT_SDA
5	5	6	6 LT_SCL
7	7	8	8 PM_ALERT
9	9	10	10
11	11	12	12

PM_CNTL1

12V_MAIN

C824 10uF

U19 LT1965EMS

8	IN1	OUT1	1
7	IN2	OUT2	2
		ADJ	3
6	SHDN	GND	5
		GND	4
		GNDPAD	9

R759 19.1K
R760 3.92K

C825 10uF
C826 10uF

5V_SEQ

Note: Changed value so Vout = 7V in RevE1.1 to reduce Vdropout and power dissipation

Title: Arria 10 GX FPGA Development Kit
PRE-RELEASED SCHEMATIC DO NOT COPY

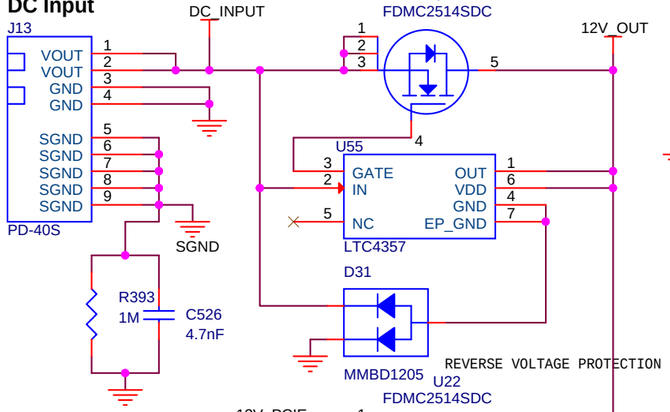
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 30 of 49

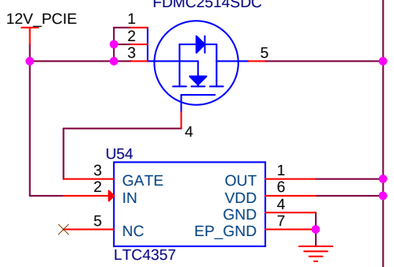
Power - Select Power Input

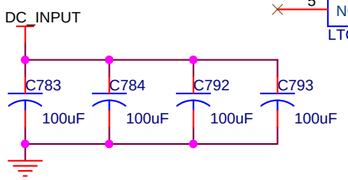
DC_IN = 12V from a laptop power supply.

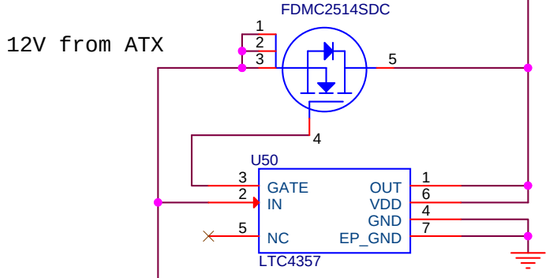
12V DC Input

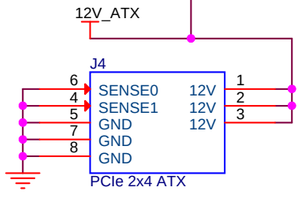


SHOULD SHIELD JUST BE TIED DIRECTLY TO GND?



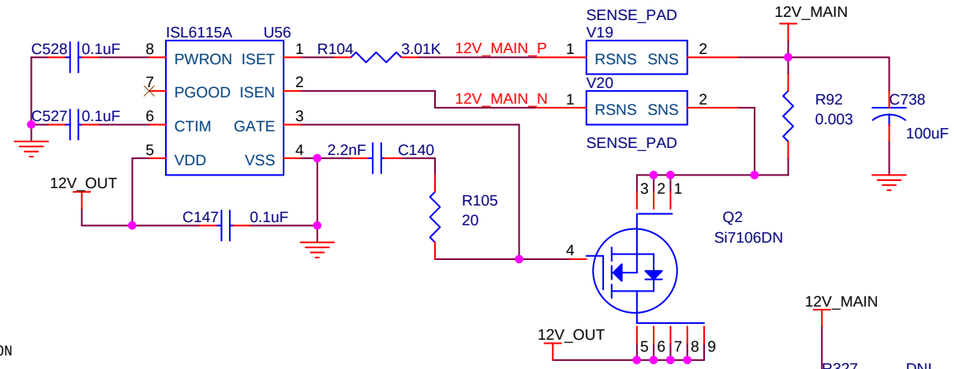


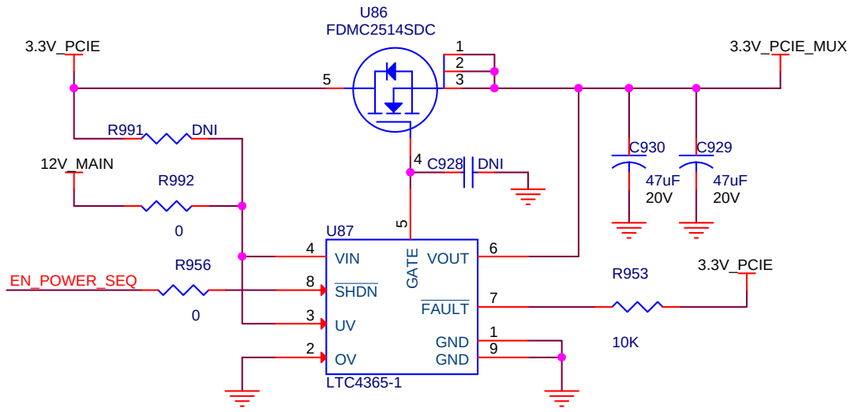


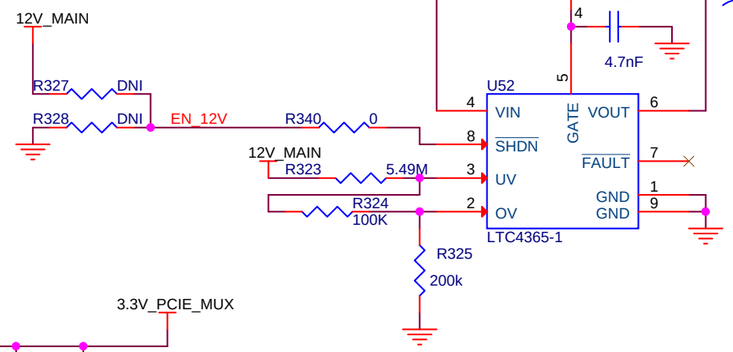


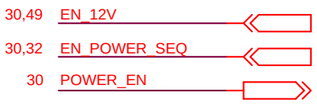
12V ATX INPUT (12.5A)

Sense0 = GND
Sense1 = GND
A 2 x 4 auxiliary power connector is plugged into the card. The card can draw up to150 W from the auxiliary power connector.

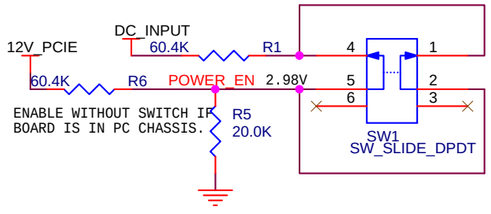








Power On Switch



DC_IN -> 12V (Laptop Supply)	*12V_PCIE ATX (2x4 ATX)*	*DC_IN_ATX (Voltage Selected by LTC4357)*
12V	12V	12V from 12V_ATX_IN
12V	0V	12V from DC_IN->12V
0V	12V	12V from 12V_ATX_IN

Title: **Arria 10 GX FPGA Development Kit**

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 31 of 49

Power - 12V to 3.3V

Place D48 between VIN and SW pins

Input Decoupling:
0402 caps directly next to part
0805 caps back side on sides of part

U82 ED8101 PWM Controller
ED8101P02
Addr = x040h

U83 ET4040

U84 LT1965EMS

U85 LT1965EMS

NOTE: Change Vin to 5V_SEQ instead of 12V_MAIN in RevE1.1 to reduce Vdropout and power dissipation

connect AGND to PGND through a single via

Keep path short

Keep path short

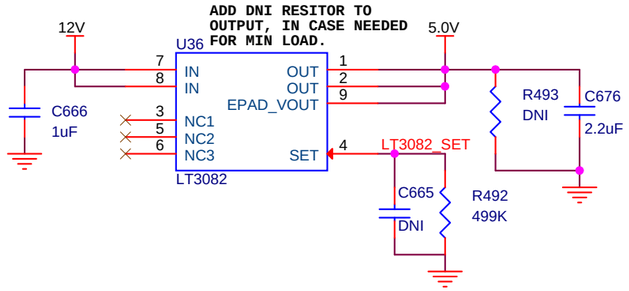
place bulk input caps on pads under ET4040 device

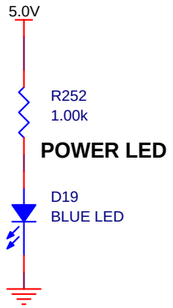
Title: Arria 10 GX FPGA Development Kit
PRE-RELEASED SCHEMATIC DO NOT COPY

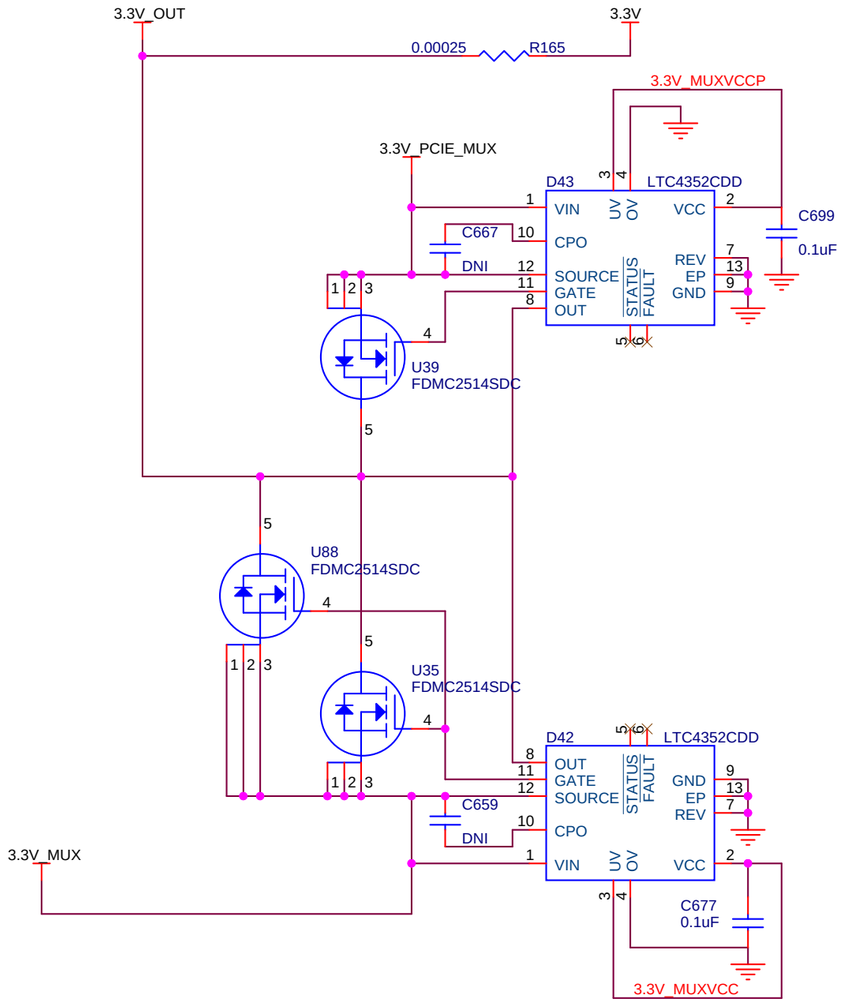
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 32 of 49

Power 1 - DC Input to 3.3V Output







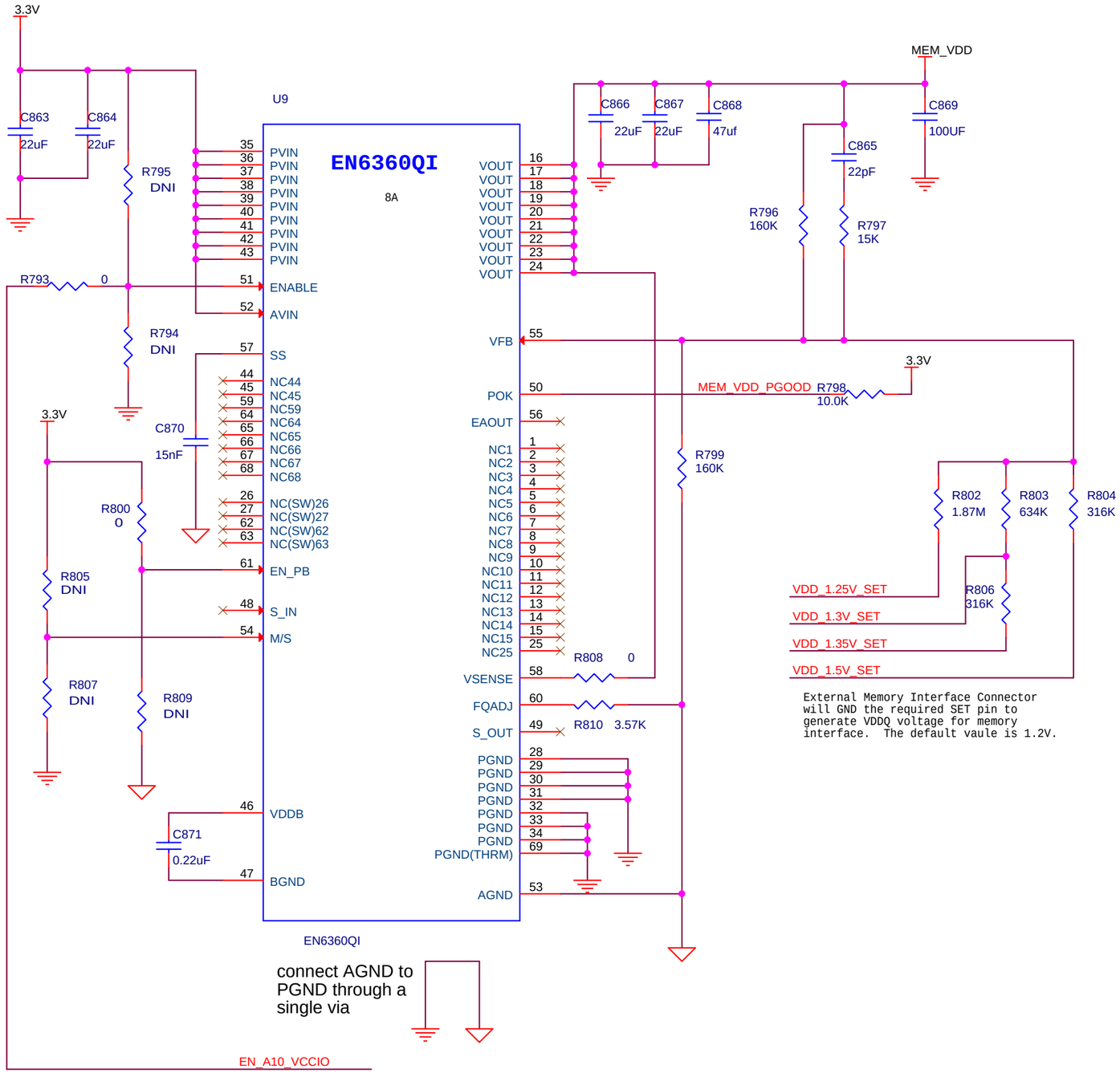
Title: **Arria 10 GX FPGA Development Kit**

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 33 of 49

Power - MEM_VDD, 2.5V

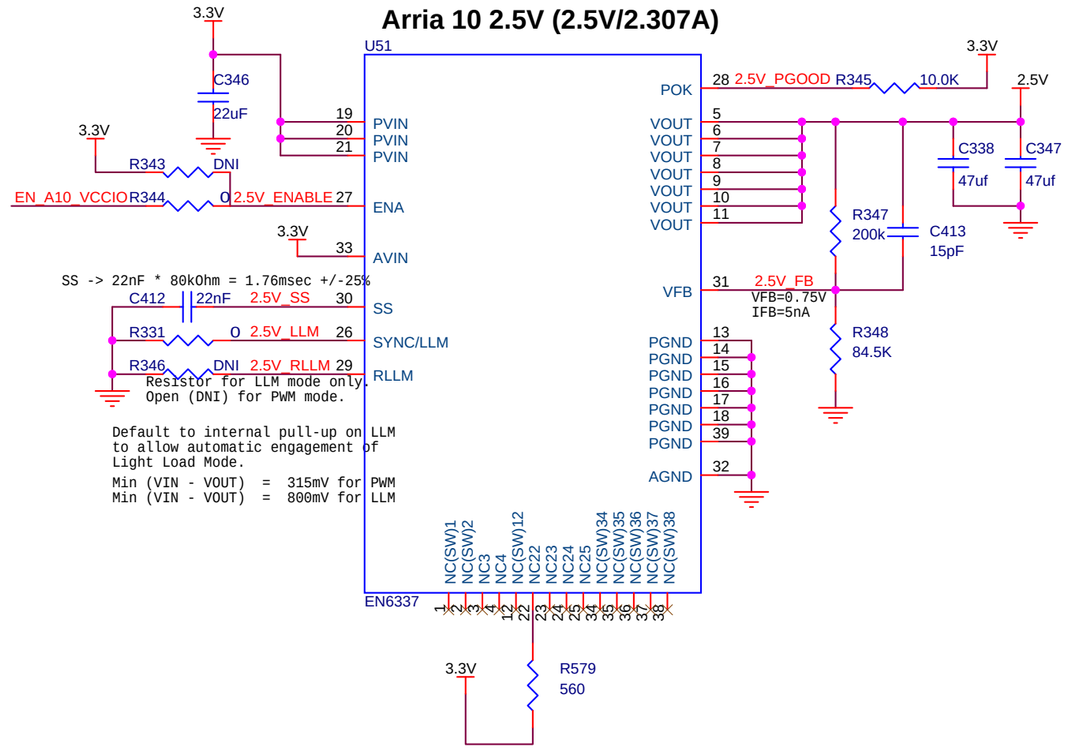


POWER CONTROL

17 VDD_1.25V_SET
3 VDD_1.3V_SET
3,17 VDD_1.35V_SET
17 VDD_1.5V_SET

30,42,43,44,45,49 EN_A10_VCCIO

Arria 10 2.5V (2.5V/2.307A)



Title: **Arria 10 GX FPGA Development Kit**

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 34 of 49

Power - A10 VCC

A10_VCCIO_1.8V_PGOOD 42 R397 0 A10_VCCIO_PGOOD
A10_VCCIO_FMCA_PGOOD 43 R64 0
A10_VCCIO_FMCB_PGOOD 44 R114 0
A10_VCCIO_MEM_PGOOD 45 R117 0

5.0V
R150
2.20
5.0V_VCC
0402 C201 1uF

30 EN_A10_VCC
36 PWM1
36 PWM2
37 PWM3
37 PWM4
6 VID[6:0]

5.0V
R143 DNI
EN_A10_VCC R144 0
C984 22pF
1.8V_LDO
R145 10.0K
R146 15.0K
A10_VCC_ENABLE 32
A10_VCC_EN_VTT 33

U34
19 VCC
EN_PWR
EN_VTT
VR_RDY 36 A10_VCC_PGOOD 100K R157
VR_FAN 37
VR_HOT 38
ISEN1+ 21 ISEN1_P
ISEN1- 22 ISEN1_N
ISEN2+ 27 ISEN2_P
ISEN2- 28 ISEN2_N
ISEN3+ 30 ISEN3_P
ISEN3- 29 ISEN3_N
ISEN4+ 24 ISEN4_P
ISEN4- 23 ISEN4_N
VSEN 17 A10_VCC_VSEN_P
RGND 16 A10_VCC_VSEN_N
PWM1 20 PWM1
PWM2 26 PWM2
PWM3 31 PWM3
PWM4 25 PWM4
GND 41

3.3V
R186 4.70K A10_VCC_VID0 7 VID0
R170 4.70K 6 VID1
R184 DNI A10_VCC_VID1 5 VID2
R185 4.70K A10_VCC_VID2 4 VID3
R210 4.70K A10_VCC_VID3 3 VID4
R169 DNI 2 VID5
R183 4.70K A10_VCC_VID4 1 VID6
R182 4.70K A10_VCC_VID5 40 VID7
R168 4.70K A10_VCC_VID6 8 VRSEL
R167 4.70K A10_VCC_VID7
R171 DNI VRSEL
R151 31.6K A10_VCC_FS 34 FS
R152 499K A10_VCC_SS 35 SS
5.0V_VCC R187 DNI A10_VCC_OFS 9 OFS
R189 DNI
C222 0.1uF R188 1.00k A10_VCC_DAC 10 DAC
R190 4.02K A10_VCC_REF 11 REF
C212 1nF R172 10.0K A10_VCC_COMP 12 COMP
C211 DNI
A10_VCC_FB 13 FB
POPULATE 0-OHM RESISTOR TO ENABLE DROOP -> R160 DNI A10_VCC_IDROOP 14 IDROOP
R161 2.74K C202 470pF R588 15 VDIFF
R159 2.74K 0
5.0V_VCC R153 10.0K A10_VCC_TCOMP 18 TCOMP
R154 806
R158 1.27K A10_VCC_TM 39 TM
R166 6.8K
NTC RESITOR:
EC7401

VID settings:
0.90V (Production Si) -> VID[7:0] = 0100 1110
0.95V (ES Silicon) -> VID[7:0] = 0100 0100
(VID table adjusted based on DAC resistor, to default boot voltage of 0.880V with 5mV increments)
*To increment in 10mV steps always leave VID0=0

VRSEL
- VR11 (DEFAULT) - FLOATING OR HIGH
- VR10 - GND

FS
FREQ = 2.5*10^10/RFS
FREQ = 2.5*10^10/33.2K = 753KHz

R140 143 C192 DNI C190 DNI C189 0.1uF 36 PH1_VCC_P
R138 4.42K 36 PH1_VCC_N
R135 143 C186 DNI C176 DNI C184 0.1uF 36 PH2_VCC_P
R133 4.42K 36 PH2_VCC_N
R134 143 C191 DNI C183 DNI C185 0.1uF 37 PH3_VCC_P
R136 4.42K 37 PH3_VCC_N
R137 143 C187 DNI C177 DNI C188 0.1uF 37 PH4_VCC_P
R139 4.42K 37 PH4_VCC_N

C983 220pF
A10_VCC PLACE RESISTOR PADS OVERLAPPING SO THAT A RESISTOR CAN BE POPULATED TO PULL-UP TO A10_VCC OR ROUTE A10_VCC_VCCLSENSE_P.
R1003 10 R512 0 R513 DNI 46 A10_VCC_VCCLSENSE_P
R1002 10 R514 DNI 46 A10_VCC_VCCLSENSE_N R515 0
PLACE RESISTOR PADS OVERLAPPING SO THAT A RESISTOR CAN BE POPULATED TO PULL-DOWN TO GND OR ROUTE A10_VCC_VCCLSENSE_N.

U72 74VCX08BQX
1.8V
VCC 14
A0 B0 A0&B0=00 1 2 O0 3 FPGA_USER_MODE
A1 B1 A1&B1=01 4 5 O1 6 VID_SELECTED
A2 B2 A2&B2=02 13 12 O2 11 VID_READY
A3 B3 A3&B3=03 10 9 O3 8
GND 7
EPAD_NC 15
FPGA_CONF_DONE 7,13
FPGA_VID_EN 7
VID_EN 6,7
A10_VCCIO_PGOOD
FPGA_USER_MODE
VID_SELECTED
R519 DNI
R520 10.0K
R532 DNI

U70 MAX3378_UCSP
3.3V
1.8V
C230 1uF C245 0.1uF C229 0.1uF
B1 VCC IO VCC1 IO VCC2 IO VCC3 IO VCC4 VL IO VL1 IO VL2 IO VL3 IO VL4 B2
A10_VCC_VID0 C1 A1 VID0
A10_VCC_VID1 C2 A2 VID1
A10_VCC_VID2 C3 A3 VID2
A10_VCC_VID3 C4 A4 VID3
VID_READY B3 TS GND B4

U69 MAX3378_UCSP
3.3V
1.8V
C232 1uF C246 0.1uF C231 0.1uF
B1 VCC IO VCC1 IO VCC2 IO VCC3 IO VCC4 VL IO VL1 IO VL2 IO VL3 IO VL4 B2
A10_VCC_VID4 C1 A1 VID4
A10_VCC_VID5 C2 A2 VID5
A10_VCC_VID6 R211 DNI VID6_RES C3 A3 VID6
C4 A4
VID_READY B3 TS GND B4

Title: Arria 10 GX FPGA Development Kit
PRE-RELEASED SCHEMATIC DO NOT COPY

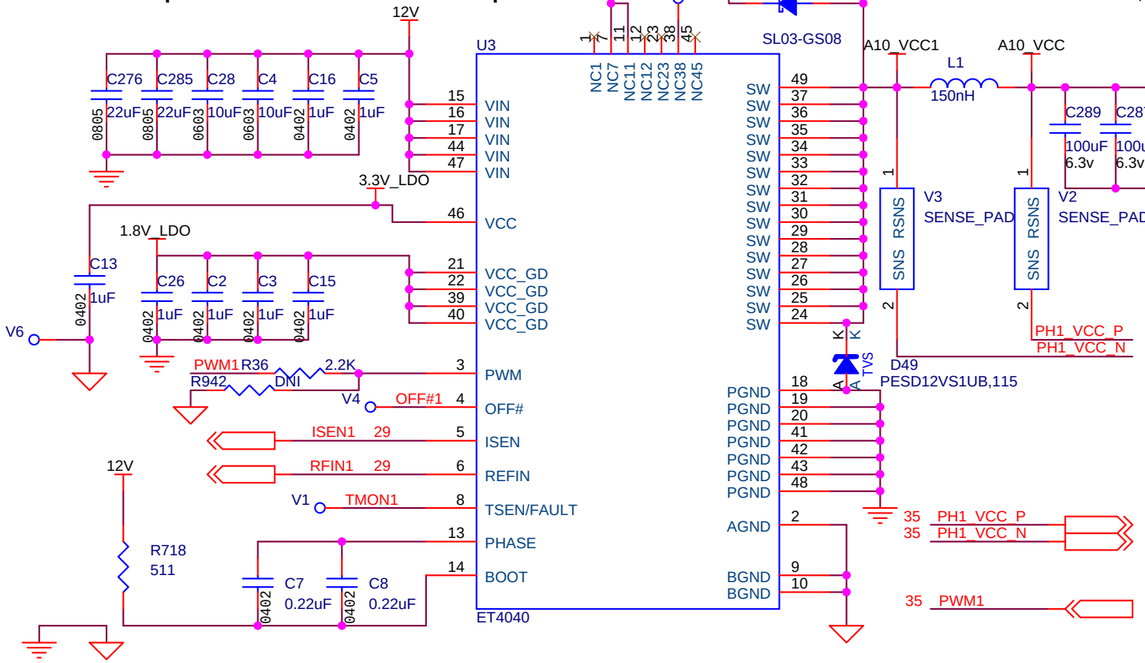
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 35 of 49

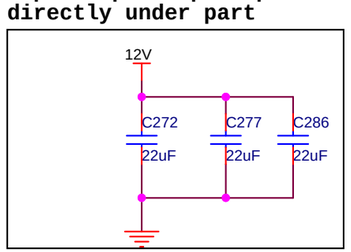
Power1 A10 VCC ET4040 (1)

PHASE 1

Input Decoupling:
0402 caps directly next to part
0805 caps back side on sides of part

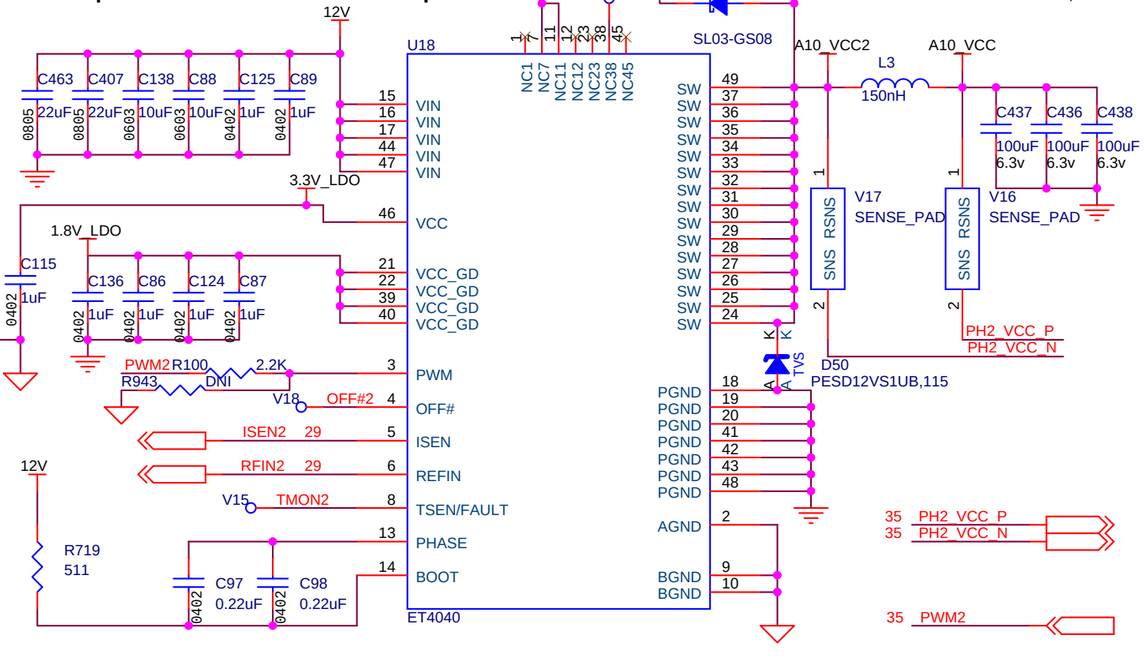


Input caps on part pads directly under part

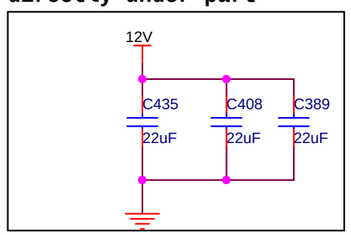


PHASE 2

Input Decoupling:
0402 caps directly next to part
0805 caps back side on sides of part



Input caps on part pads directly under part



Title: **Arria 10 GX FPGA Development Kit**

PRE-RELEASED SCHEMATIC DO NOT COPY

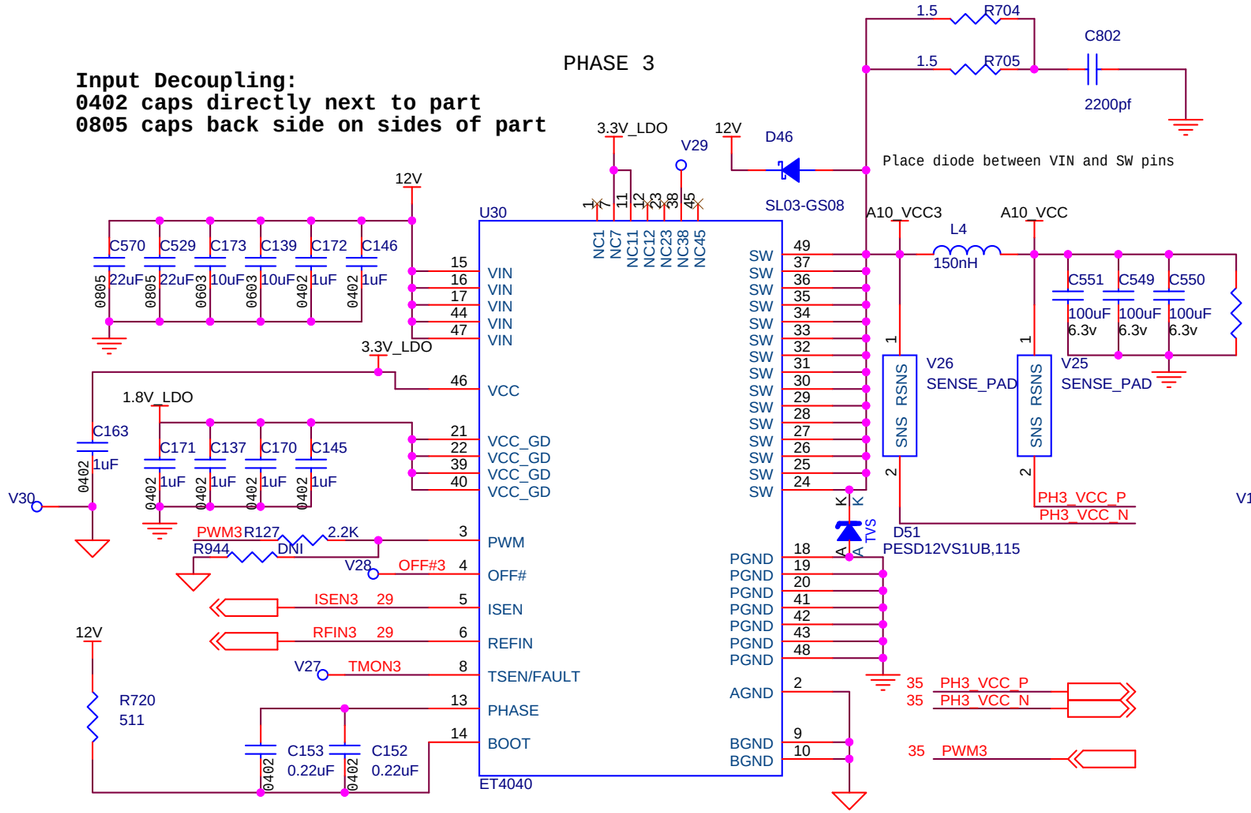
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 36 of 49

Power1 A10 VCC ET4040 (2)

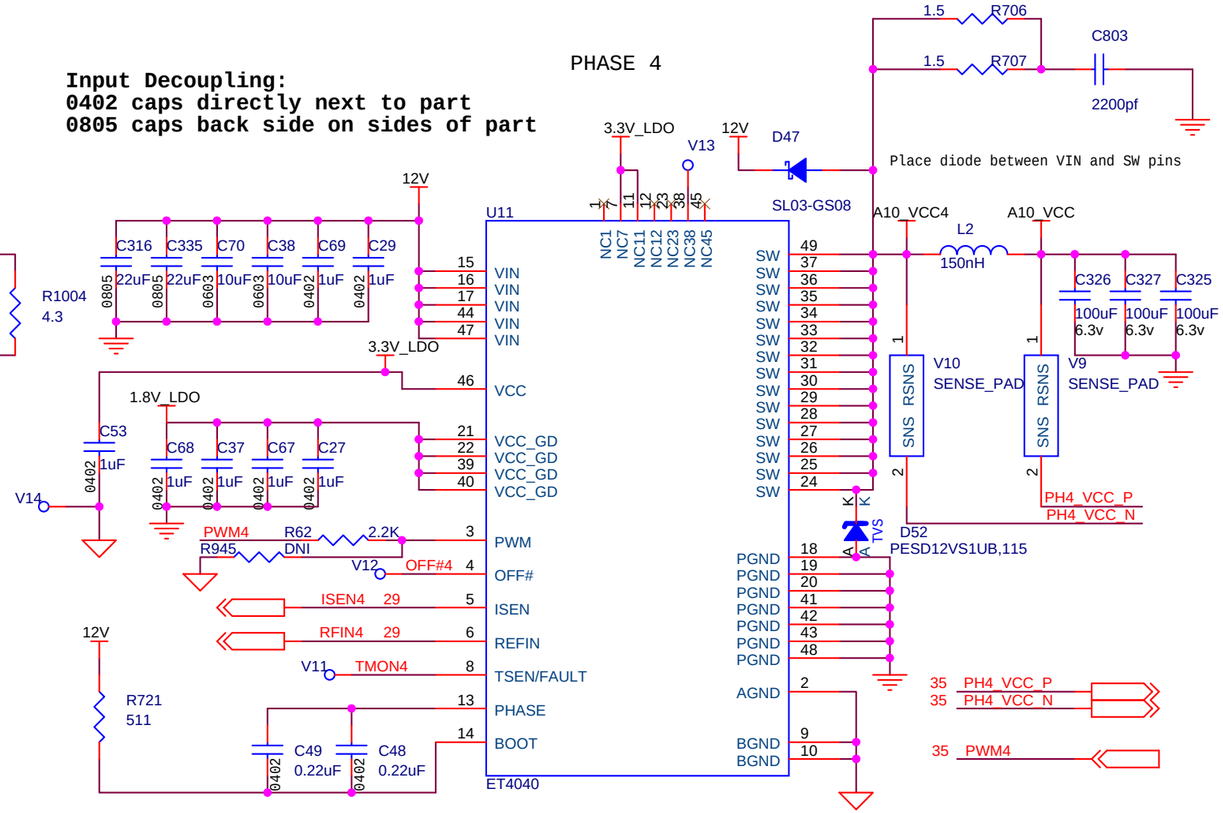
Input Decoupling:
0402 caps directly next to part
0805 caps back side on sides of part

PHASE 3

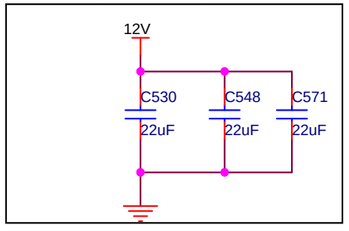


Input Decoupling:
0402 caps directly next to part
0805 caps back side on sides of part

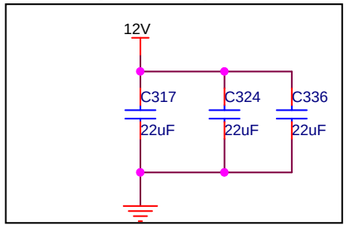
PHASE 4



Input caps on part pads directly under part



Input caps on part pads directly under part



Title: Arria 10 GX FPGA Development Kit

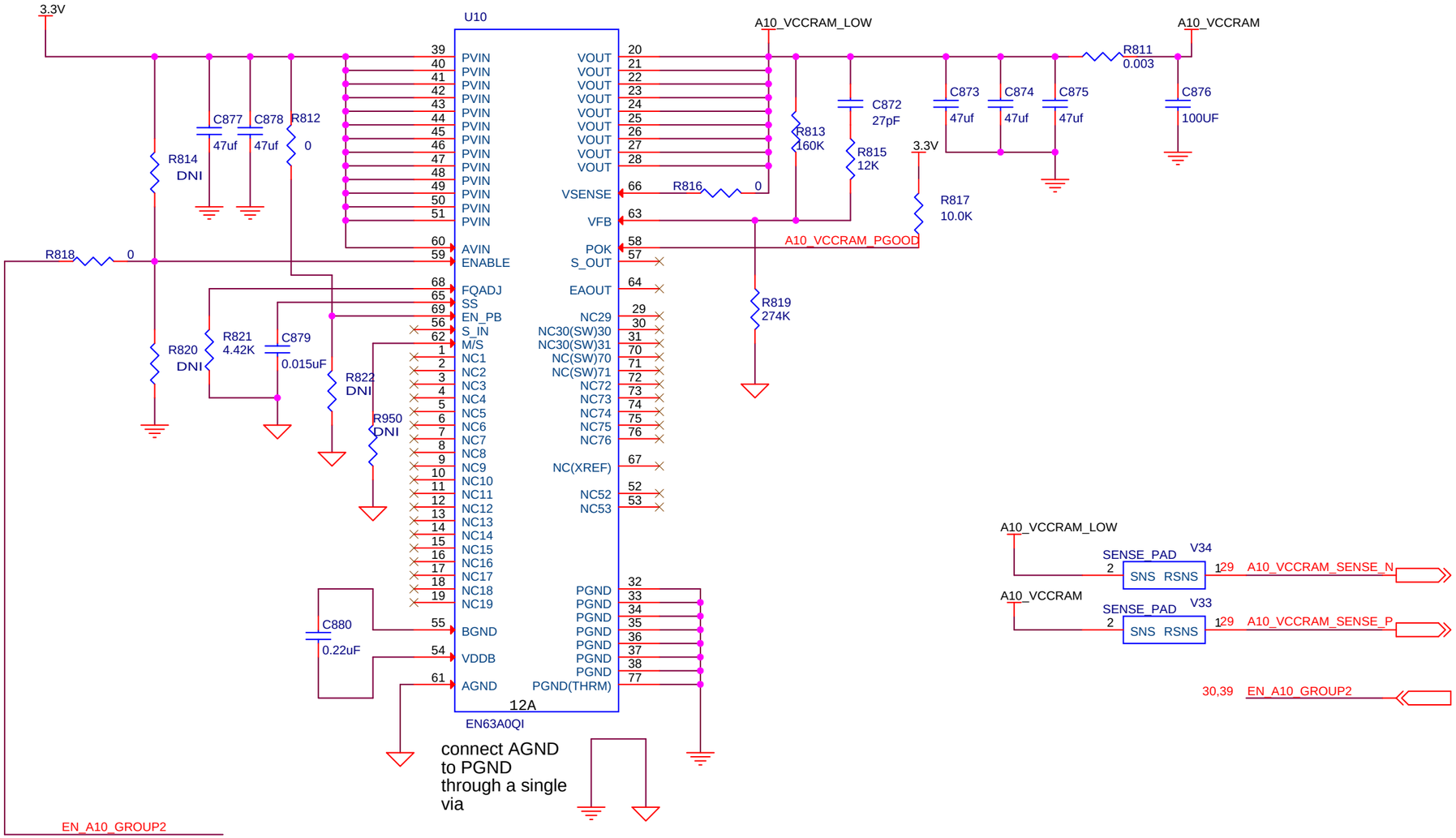
PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 37 of 49

Power - A10 VCCRAM

Arria 10 - VCCRAM (0.95V/5.117A)



Title: Arria 10 GX FPGA Development Kit

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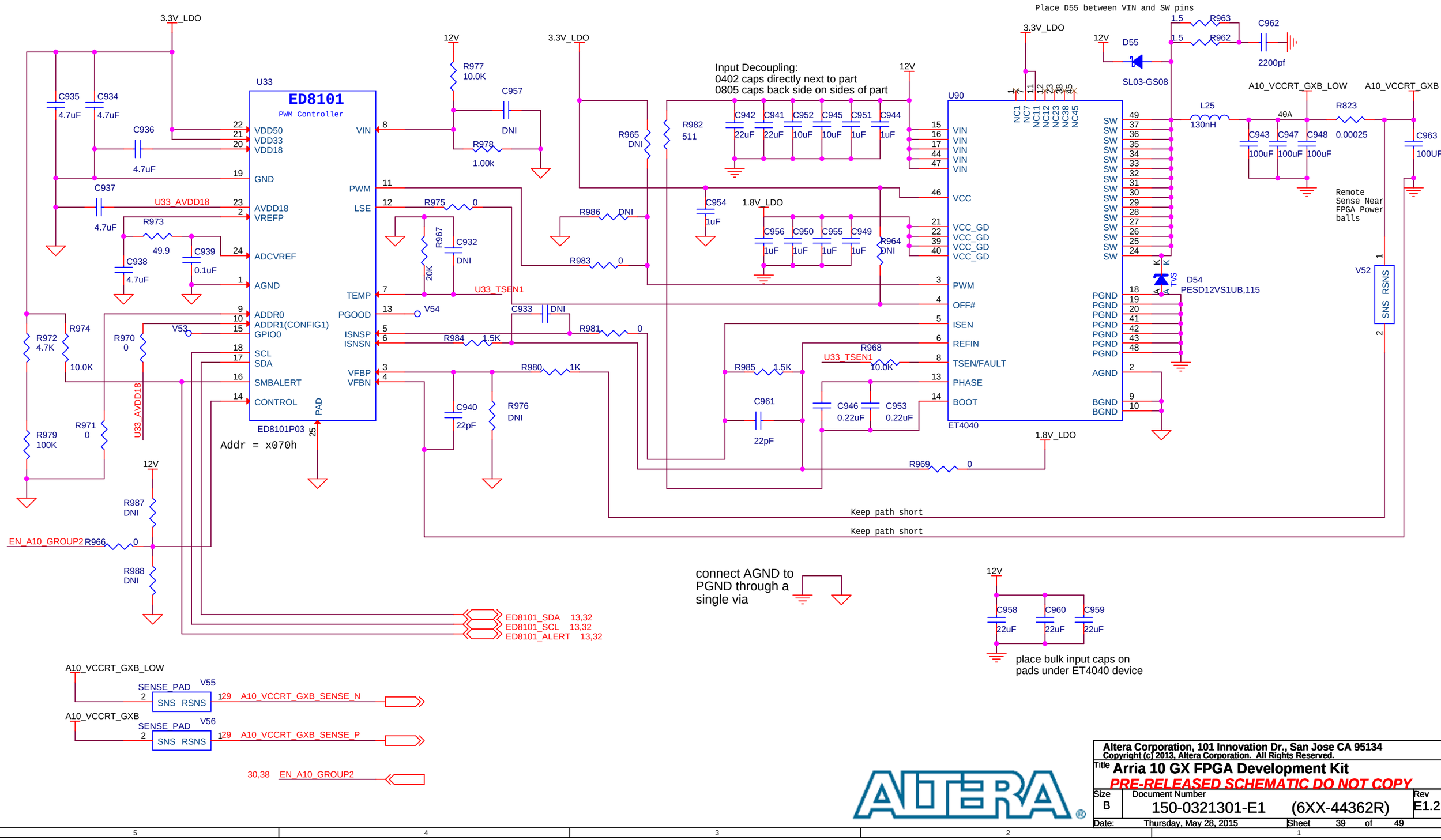
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 38 of 49

Power - A10 VCCRT GXB

Arria 10 - VCCRT_GXB (1.03V/17A)
Can be 0.9V, 1.03V, or 1.1V



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PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 39 of 49

Title **Arria 10 GX FPGA Development Kit**

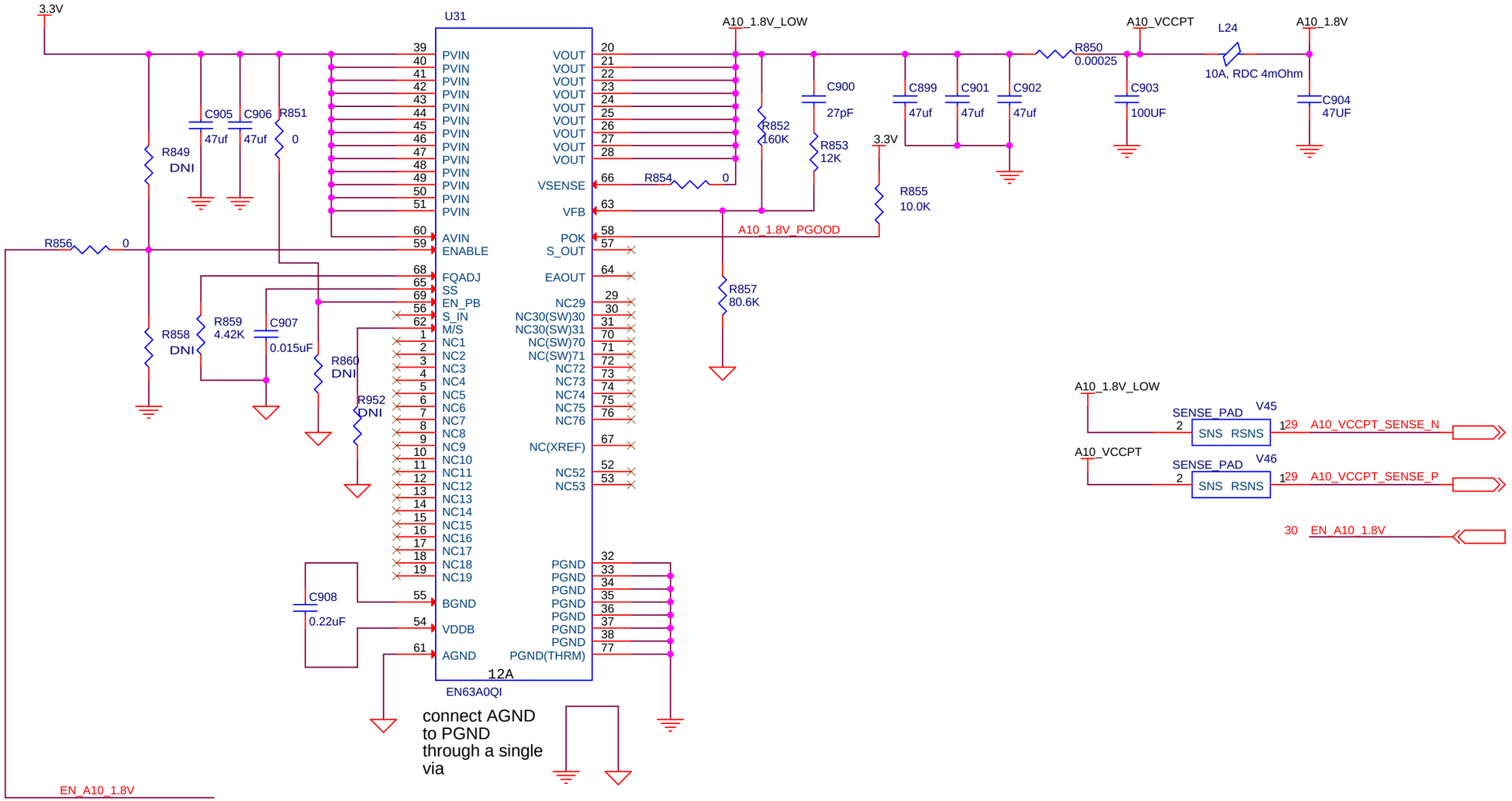
PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 40 of 49

Power - A10 VCCPT & 1.8V

Arria 10
VCCA_PLL, VCCH_GXB, VCCPT
(1.8V/10.229A)



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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 41 of 49

Power - A10 VCCIO 1.8V

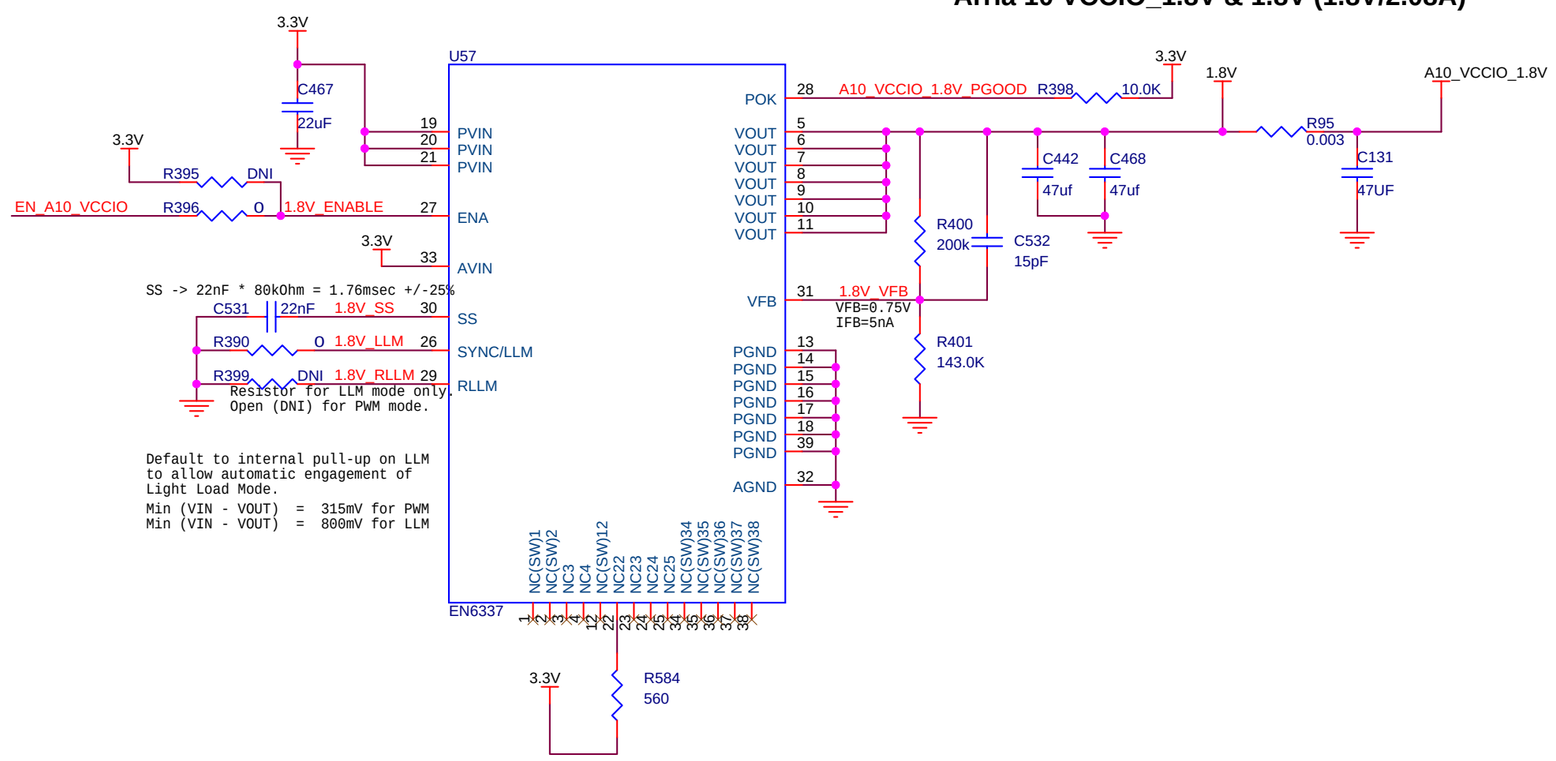
34,43,44,45,49 EN_A10_VCCIO

35 A10_VCCIO_1.8V_PGOOD

1.8V — SENSE_PAD V21 — 2 SNS RSNS 29 — A10_VCCIO_1.8V_SENSE_N

A10_VCCIO_1.8V — SENSE_PAD V24 — 2 SNS RSNS 29 — A10_VCCIO_1.8V_SENSE_P

Arria 10 VCCIO_1.8V & 1.8V (1.8V/2.08A)



Title: Arria 10 GX FPGA Development Kit

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 42 of 49

Power - A10 VCCIO FMCA

34,42,44,45,49 EN_A10_VCCIO

35 A10_VCCIO_FMCA_PGOOD

FMCA_ADJ

SENSE_PAD V37

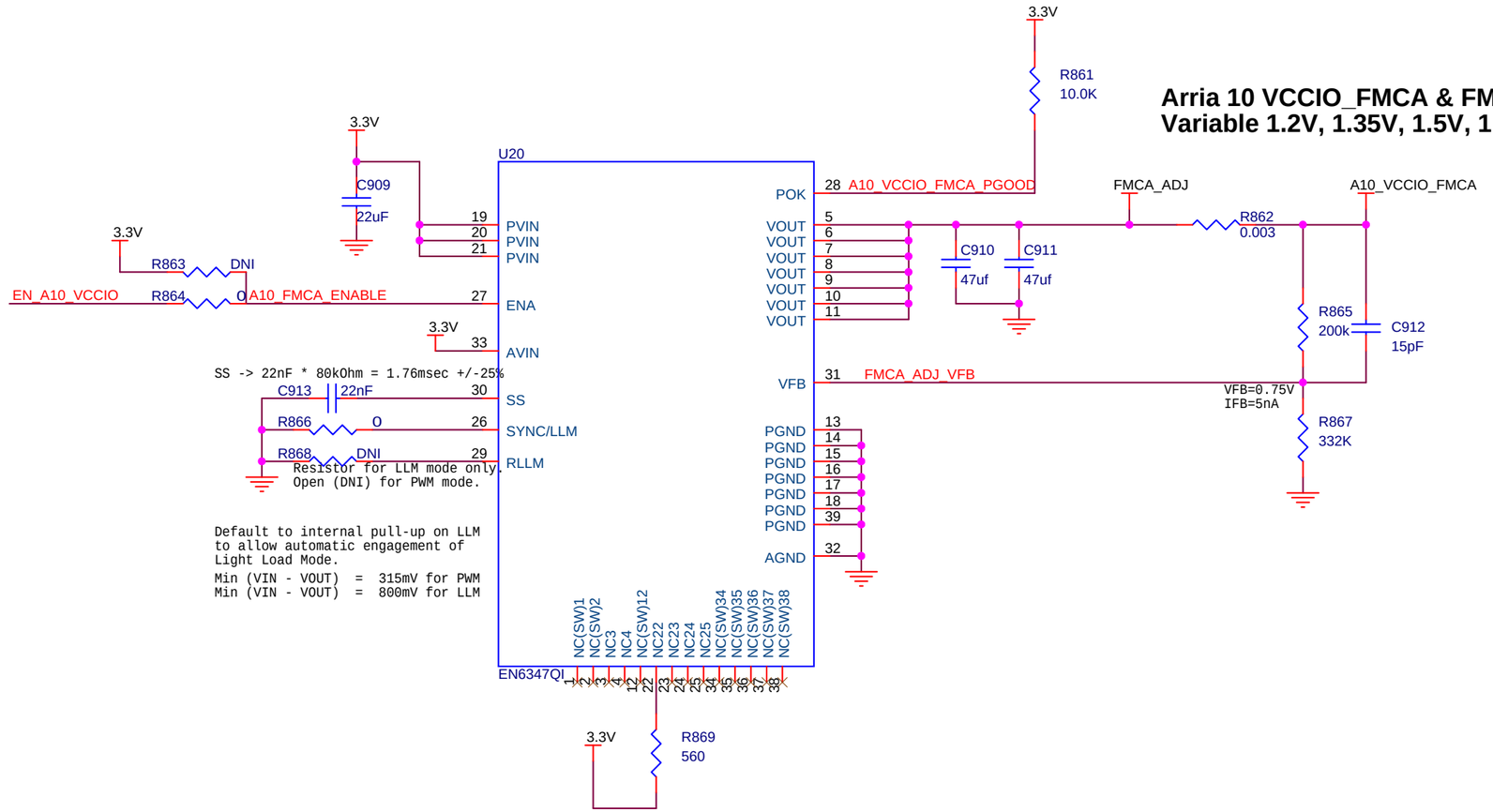
2 SNS RSNS 29 A10_VCCIO_FMCA_SENSE_N

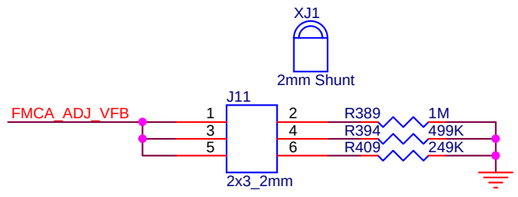
A10_VCCIO_FMCA

SENSE_PAD V38

2 SNS RSNS 29 A10_VCCIO_FMCA_SENSE_P

Arria 10 VCCIO_FMCA & FMCA_VADJ (1.2V/3.5A)
Variable 1.2V, 1.35V, 1.5V, 1.8V





FMCA Voltage

Setting	VCCIO FMCA SELECT
NO JUMPER	1.2V
JUMPER 1-2	1.35V
JUMPER 3-4	1.5V
JUMPER 5-6	1.8V

Title: Arria 10 GX FPGA Development Kit

PRE-RELEASED SCHEMATIC DO NOT COPY

Size: B | Document Number: 150-0321301-E1 (6XX-44362R) | Rev: E1.2

Date: Thursday, May 28, 2015 | Sheet 43 of 49

Power - A10 VCCIO FMCB

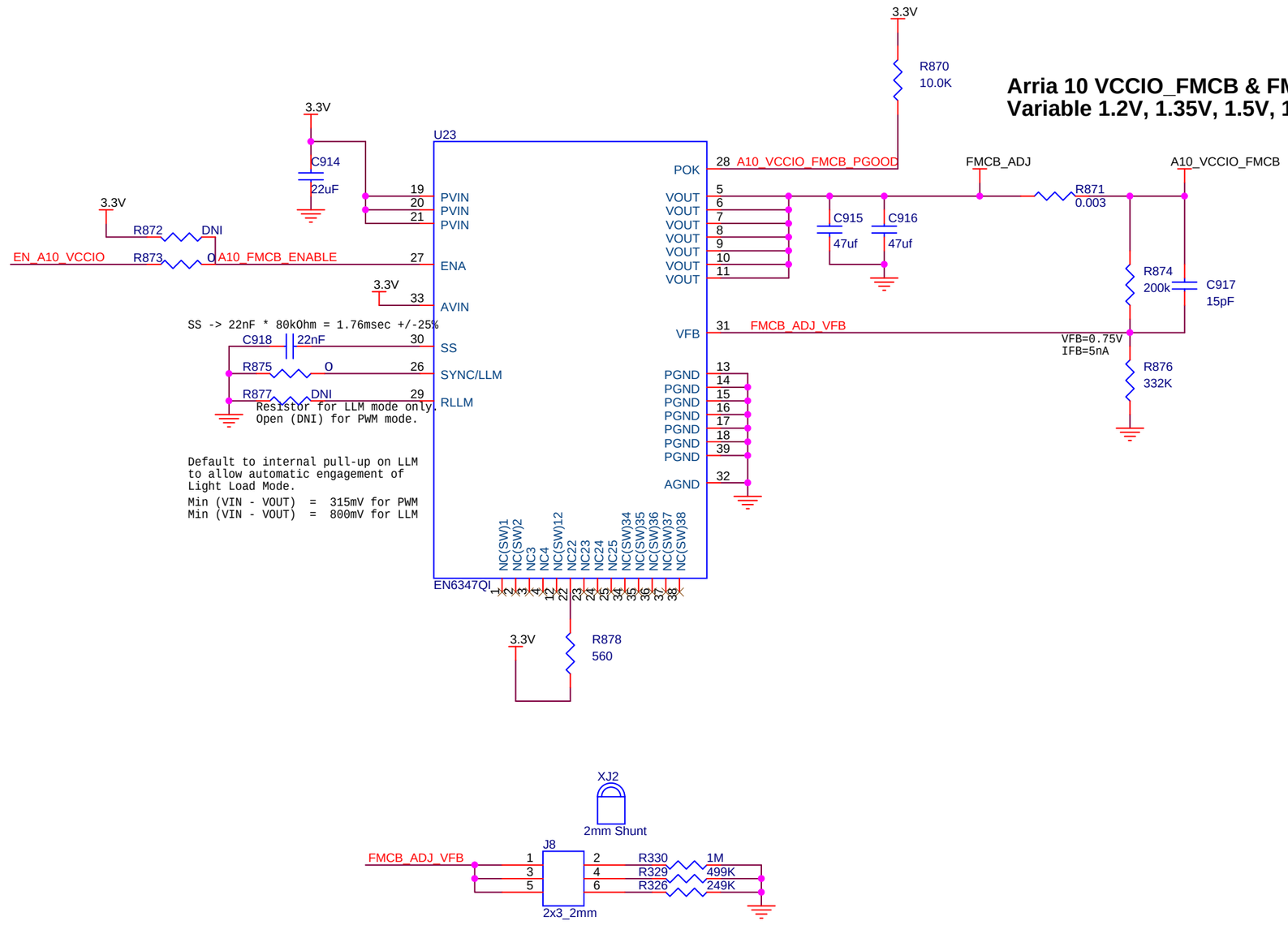
3,45,49 EN_A10_VCCIO

35 A10_VCCIO_FMCB_PGOOD

FMCB_ADJ — SENSE_PAD V42 — 2 SNS RSNS 29 — A10_VCCIO_FMCB_SENSE_N

A10_VCCIO_FMCB — SENSE_PAD V41 — 2 SNS RSNS 29 — A10_VCCIO_FMCB_SENSE_P

Arria 10 VCCIO_FMCB & FMCB_VADJ (1.2V/3.5A)
Variable 1.2V, 1.35V, 1.5V, 1.8V



FMCA Voltage

Setting	VCCIO FMCB SELECT
NO JUMPER	1.2V
JUMPER 1-2	1.35V
JUMPER 3-4	1.5V
JUMPER 5-6	1.8V

Title: Arria 10 GX FPGA Development Kit

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 44 of 49

Power - A10 VCCIO MEM

POWER CONTROL

17 VDDQ_1.25V_SET
17 VDDQ_1.35V_SET
17 VDDQ_1.5V_SET
49 EN_A10_VCCIO
35 A10_VCCIO_MEM_PGOOD

MEM_VDDQ
SENSE_PAD 2 — V40 — SNS RSNS — 129 A10_VCCIO_MEM_SENSE_N

A10_VCCIO_MEM
SENSE_PAD 2 — V39 — SNS RSNS — 129 A10_VCCIO_MEM_SENSE_P

Arria 10 VCCIO_MEM & MEM_VDDQ (1.2V/4.7A)
Variable 1.2V, 1.25V, 1.35V, 1.5V

3.3V
C923 22uF
C924 22uF
R880 DNI
R883 0
R884 DNI
3.3V
C926 15nF
R887 0
R888 DNI
R893 DNI
R894 DNI
C927 0.22uF

U24
EN6360QI
8A

35	PVIN	
36	PVIN	
37	PVIN	
38	PVIN	
39	PVIN	
40	PVIN	
41	PVIN	
42	PVIN	
43	PVIN	
51	ENABLE	
52	AVIN	
57	SS	
44	NC44	
45	NC45	
59	NC59	
64	NC64	
65	NC65	
66	NC66	
67	NC67	
68	NC68	
26	NC(SW)26	
27	NC(SW)27	
62	NC(SW)62	
63	NC(SW)63	
61	EN_PB	
48	S_IN	
54	M/S	
46	VDDB	
47	BGND	
16–24	VOUT	
55	VFB	
50	POK	
56	EAOUT	
1–15, 25	NC1 … NC15, NC25	
58	VSENSE	
60	FQADJ	
49	S_OUT	
28–34, 69	PGND, PGND(THRM)	
53	AGND	

MEM_VDDQ
C919 22uF
C920 22uF
C921 47uf
R879 0.003
A10_VCCIO_MEM
C922 100UF
C925 22pF
R881 160K
R882 15K
R886 160K
3.3V
A10_VCCIO_MEM_PGOOD
R885 10.0K
R892 0
R895 3.57K
R889 1.87M
R890 634K
R891 316K
VDDQ_1.25V_SET
VDDQ_1.35V_SET
VDDQ_1.5V_SET

External Memory Interface Connector will GND the required SET pin to generate VDDQ voltage for memory interface. The default vaule is 1.2V.

EN6360QI

connect AGND to PGND through a single via

EN_A10_VCCIO

Title: **Arria 10 GX FPGA Development Kit**
PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 45 of 49

Arria 10 Power

U28R — ARRIA 10 - POWER

CORE PWR (0.83V, 0.86V, 0.9V)

A10_VCC

VCC: R24, T15, T17, T18, T19, T20, T22, T24, T29, Y29, Y27, Y26, Y25, Y24, Y22, Y21, Y20, Y19, Y17, Y16, W29, W28, W27, W26, W24, W23, W22, W21, W19, W18, W17, W16, V29, V28, V24, V23, V19, V18, V16, U27, U17, T30, T28, T27, T25, T23, R29, R27, R19, R16, AK27, AK24, AK19, AK16, AJ28, AJ26, AJ23, AJ18, R22, R17, AK29, AK26, AK20, AK17, AJ29, AJ27, AJ24, AJ21, AJ19, AJ17, AH29, AH24

A10_VCC

VCC: AA15, AA17, AA18, AA19, AA20, AA22, AA23, AA24, AA25, AA27, AA28, AA29, AB15, AB16, AB17, AB18, AB20, AB21, AB25, AB26, AB27, AB28, AC14, AC19, AC20, AC24, AC25, AC30, AD16, AD17, AD18, AD19, AD21, AD22, AD23, AD24, AD26, AD27, AD28, AD29, AE16, AE17, AE19, AE20, AE21, AE22, AE24, AE25, AE26, AE27, AE29, AF17, AF18, AF19, AF20, AF24, AF27, AF29, AG17, AG22, AG26, AG28, AH23, AH26, AJ16, AF25, AF28, AG16, AG18, AG23, AG27, AH18

Periphery PWR (0.83V, 0.86V, 0.9V)

VCCP: AG15, AG20, AG21, AG25, AG30, AH15, AH20, AH30, U15

VCCP: U21, U25, U30, V15, V20, V21, V25, V26, V30

A10_VCC_VCCLSENSE_P — AF22 — VCCLSENSE

A10_VCC_VCCLSENSE_N — AF23 — GNDSENSE

ADCGND — R20 — FB1 (120ohm, 800mA)

10AX115F1932C

U28S — ARRIA 10 - POWER

VCCIO (1.2V, 1.5V, 1.8V)

A10_VCCIO_1.8V

VCCIO2A: AR28, AU29, AV27, AT27

VCCIO2A: AR23, AU24, AV22, AN23

VCCIO3A

VREFB2AN0: AK33

VREFB3AN0

A10_VCCIO_FMCA

VCCIO2I: AL31, AM29, AR30

VCCIO3B: AM19, AP20, AR18, AN18

VREF_FMCA

A10_VCCIO_MEM

VREFB2IN0: AA31

VREFB3BN0

MEM_VREF

VCCIO2J: AD30, W30, AB30

VCCIO3C: AN12, AP15, AR13, AT12

VREFB2JN0

VREFB3CN0

A10_VCCIO_1.8V

VCCIO2K: P30, T31, V32, R32

VCCIO3D: AC12, AD15, AE13, AD11

VREFB2KN0

VREFB3DN0

A10_VCCIO_1.8V

VCCIO2L: J30, K28, M29, K32

VCCIO3E: AB14, W15, Y13, AA12

VREFB2LN0

VREFB3EN0

A10_VCCIO_FMCB

VCCIO3F: K13, M14, N12, K15

VREF_FMCB

A10_1.8V

ANALOG PWR (1.8V)

VCCA_PLL: AB23, AB22

VREFB3FN0

A10_VCCIO_1.8V

CONFIG PWR (1.2V, 1.5V, 1.8V)

VCCPGM: AK21, AK22

VCCIO3G: K18, L21, M19, L17

VREFB3GN0

A10_VCCIO_1.8V

A10_VCCPT

IO PRE-DRIVER PWR (1.8V)

VCCPT: AH16, AH19, AH21, AH25, AH28, AJ22, U16, U18, U20, U22, U23, U26, U28

VCCIO3H: J25, K23, M24, M22

VREFB3HN0

BATTERY PWR (1.5V, 1.8V)

VCCBAT: AL23

A10_VCCPT

A10_VCCRAM

MEM PWR 0.95VES/0.9V

VCCERAM: AC15, AC16, AC18, AC23, AC29, AC21, AC26, AC28

VREFP_ADC: R21

VREFN_ADC: P21

VSIGP_0: N19

VSIGN_0: P19

VSIGP_1: P18

VSIGN_1: N18

10AX115F1932C

A10_VREF_ADC_P — 1 — V8 SENSE_PAD (RSNS SNS) — 2 — C36 0.1uF — 6 — D40 LT1389 (VOUT GND GND NC7 NC8 NC1 NC2 NC3)

A10_VREF_ADC_N — 1 — V7 SENSE_PAD (RSNS SNS) — 2

A10_VCCIO_1.8V — R284 27 — IS THIS VREFP_ADC/VREFN_ADC? VREFP_ADC up to 10mA? VFEF_ADC R value based on 20ma for 1.25V zener

U28T — ARRIA 10 - TRANSCEIVER PWR

A10_1.8V

TX BUFFER PWR (1.8V)

VCCH_GXBL: AB36, AF36, AK36, K36, P36, V36

VCCH_GXBR: V9, P9, K9, AK9, AF9, AB9

RREF_TR — A10 — RREF_TR R332 2.0K

RREF_TL — A35 — RREF_TL R447 2.0K

RREF_BR — BD10 — RREF_BR R337 2.0K

RREF_BL — BD35 — RREF_BL R451 2.0K

A10_VCCRT_GXB

ANALOG RX PWR (0.9V, 1.0V, 1.1V)

VCCR_GXBL1C: AM37, AM38

VCCR_GXBL1D: AH37, AH38

VCCR_GXBL1E: AD37, AD38

VCCR_GXBL1F: Y37, Y38

VCCR_GXBL1G: T37, T38

VCCR_GXBL1H: M37, M38

VCCR_GXBR4C: AM7, AM8

VCCR_GXBR4D: AH7, AH8

VCCR_GXBR4E: AD7, AD8

VCCR_GXBR4F: Y7, Y8

VCCR_GXBR4G: T7, T8

VCCR_GXBR4H: M7, M8

ANALOG TX PWR (0.9V, 1.0V, 1.1V)

A10_VCCRT_GXB

VCCT_GXBL1C: AK37, AK38

VCCT_GXBL1D: AF37, AF38

VCCT_GXBL1E: AB37, AB38

VCCT_GXBL1F: V37, V38

VCCT_GXBL1G: P37, P38

VCCT_GXBL1H: K38, K37

VCCT_GXBR4C: AK7, AK8

VCCT_GXBR4D: AF7, AF8

VCCT_GXBR4E: AB7, AB8

VCCT_GXBR4F: V7, V8

VCCT_GXBR4G: P7, P8

VCCT_GXBR4H: K7, K8

10AX115F1932C

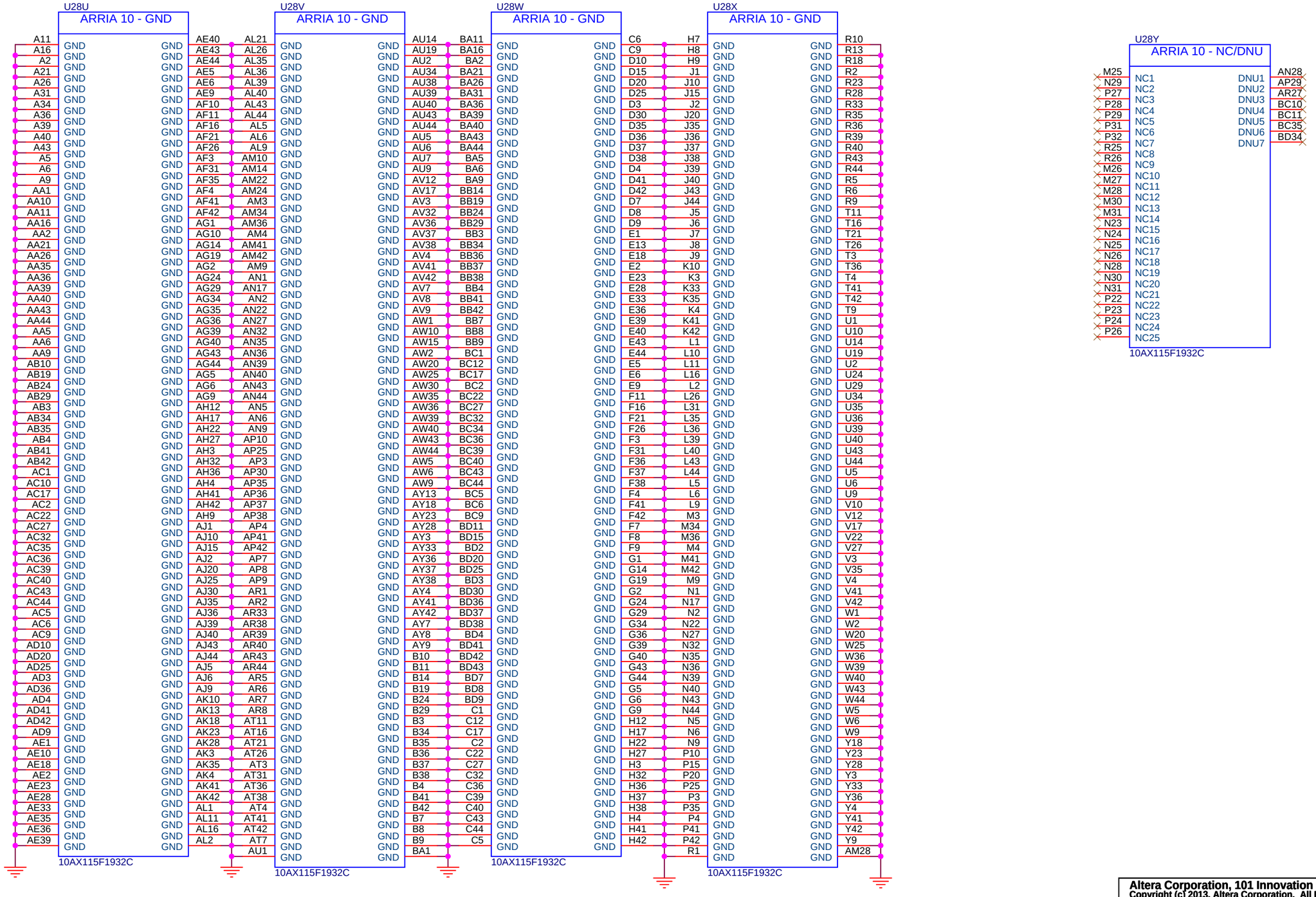
Title: Arria 10 GX FPGA Development Kit

PRE-RELEASED SCHEMATIC DO NOT COPY

Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 46 of 49

Arria 10 Ground



Title: Arria 10 GX FPGA Development Kit

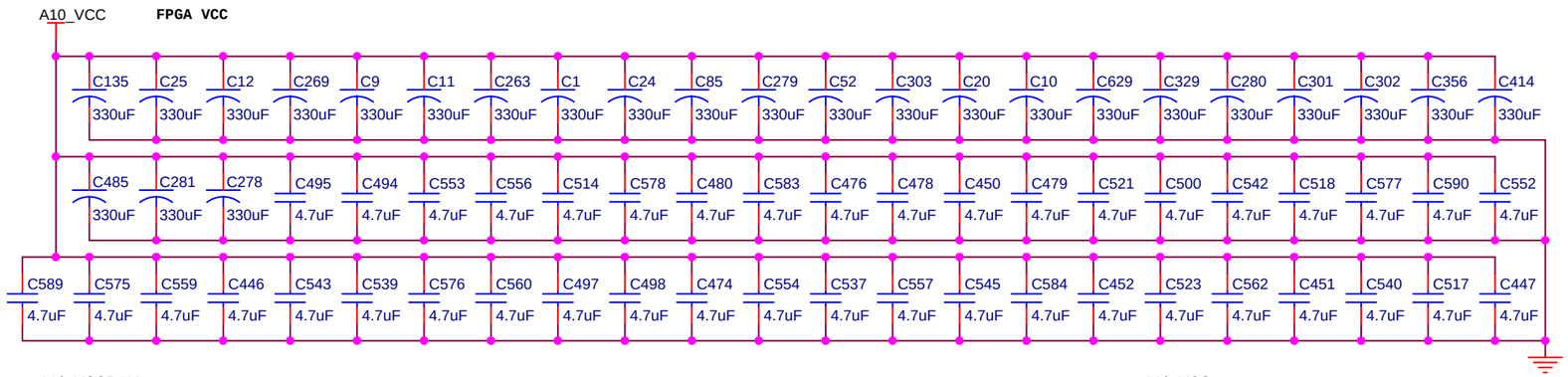
PRE-RELEASED SCHEMATIC DO NOT COPY

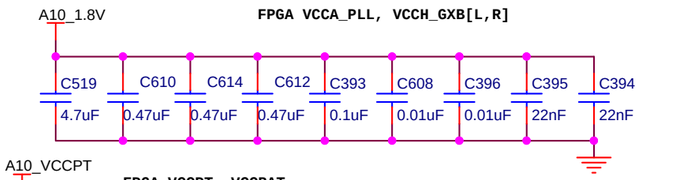
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

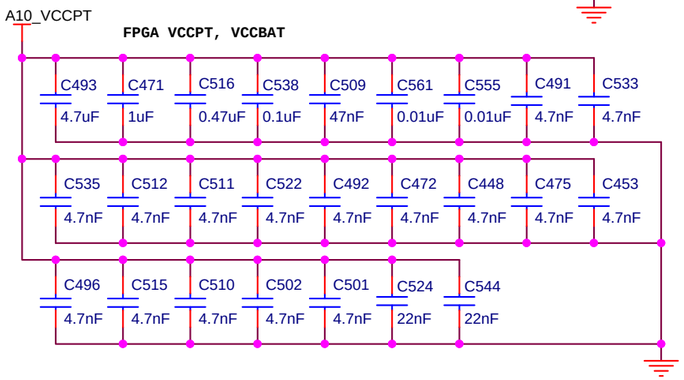
Date: Thursday, May 28, 2015 Sheet 47 of 49

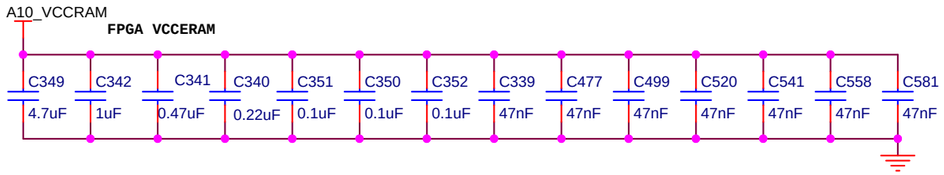
Decoupling

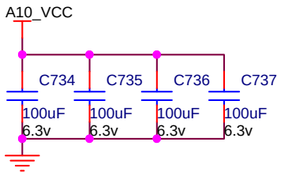
Do Not Copy. Decoupling requirements is design specific. Please use the Early Power Estimator and PDN Tool available on Altera.com to determine your specific decoupling requirements.

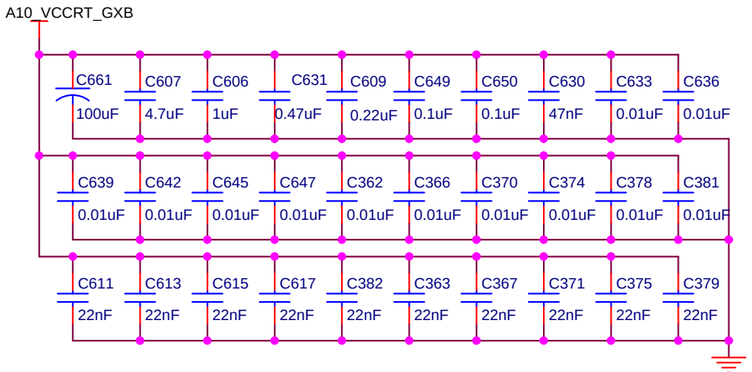


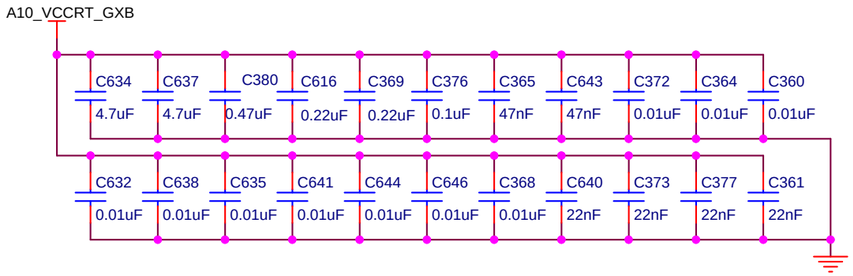


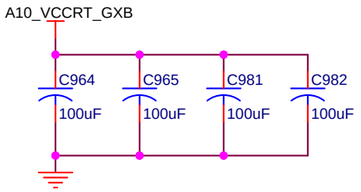


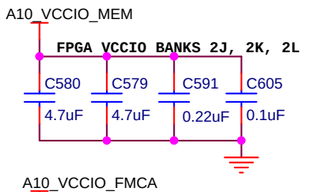


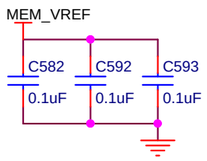


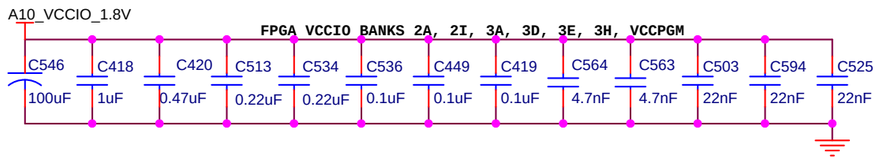


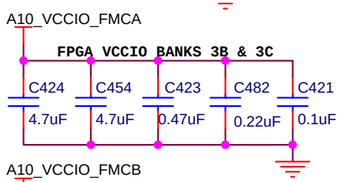


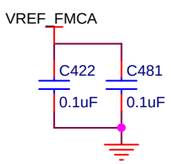


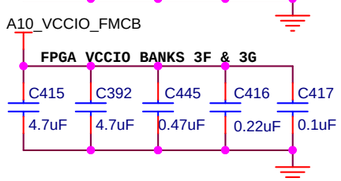


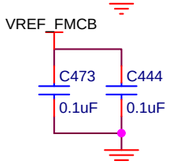


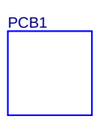












Title: **Arria 10 GX FPGA Development Kit**

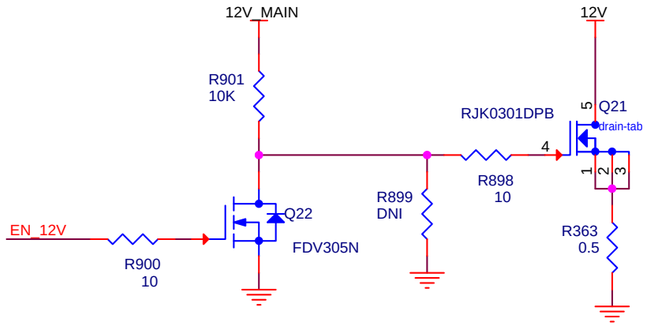
PRE-RELEASED SCHEMATIC DO NOT COPY

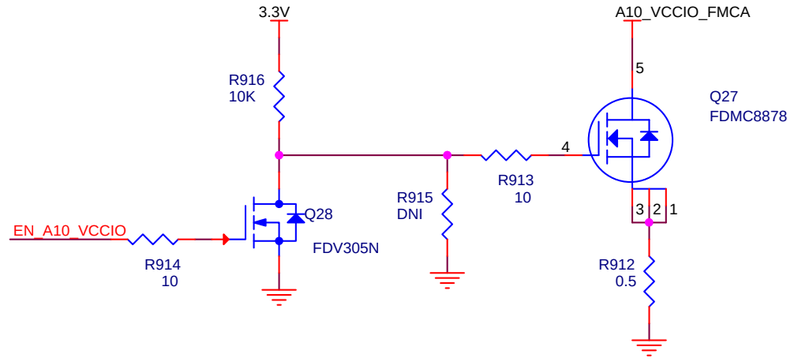
Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

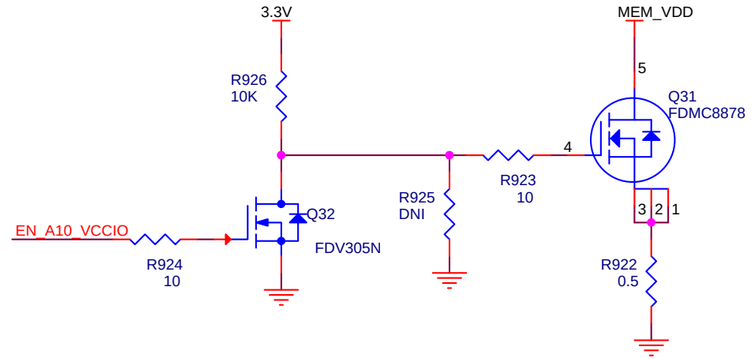
Date: Thursday, May 28, 2015 Sheet 48 of 49

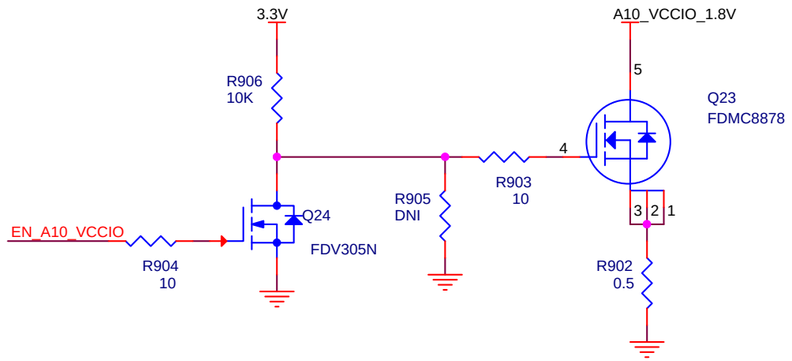
Power-down Fast Discharge

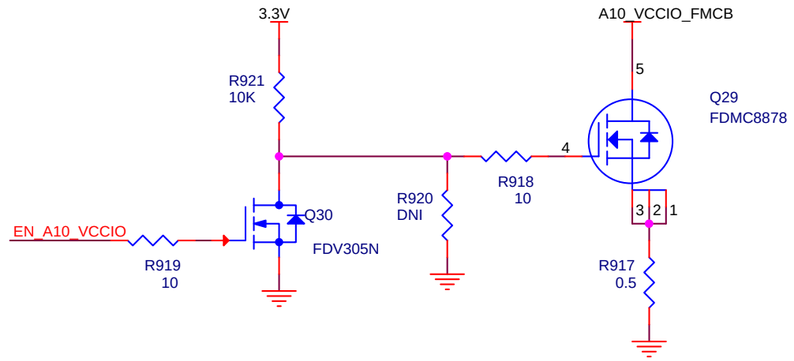
EN_12V 30,31
EN_A10_VCCIO 30,34,42,43,44,45
EN_3.3V_LDO 30,32
EN_1.8V_LDO 30,32

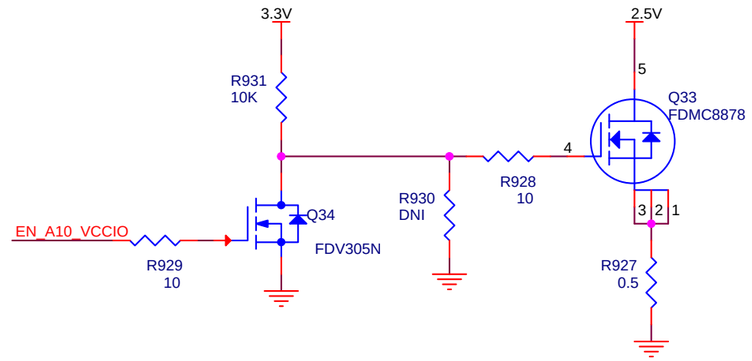


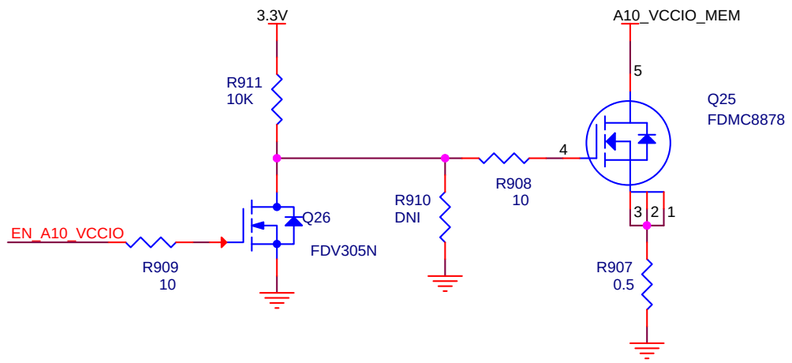


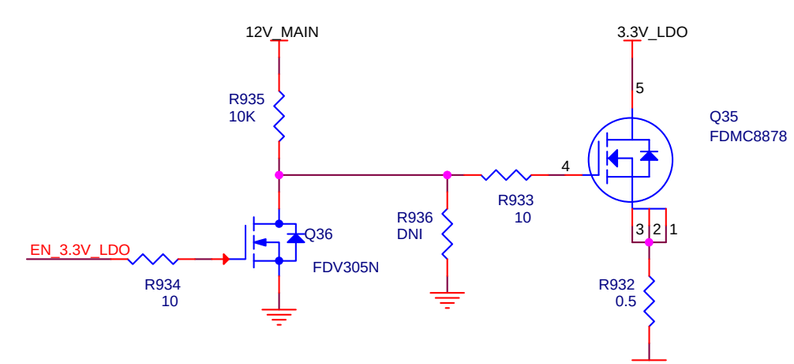


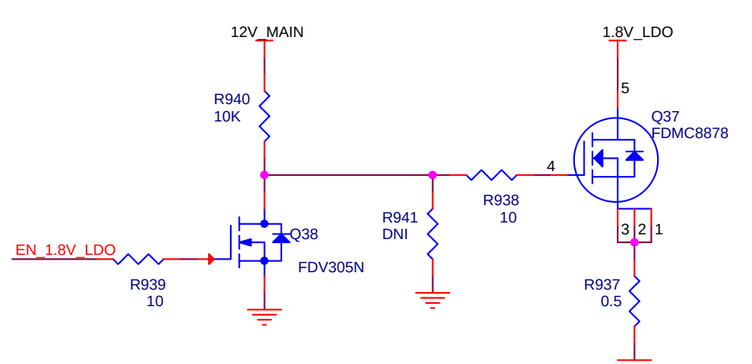












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Size	Document Number	Rev
B	150-0321301-E1 (6XX-44362R)	E1.2

Date: Thursday, May 28, 2015 Sheet 49 of 49