Intel® Iris® Xe and UHD Graphics Open Source

Programmer's Reference Manual

For the 2020-2021 11th Generation Intel Xeon®, Core™, Celeron®, Pentium® Gold Processors based on the "Tiger Lake" Platform

Volume 2c: Command Reference: Registers
Part 1 – Registers A through L

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Active Doorbell Register 0

DRB0ACT - Active Doorbell Register 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01900h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(0*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+31) has been rung.
	30	**Doorbell #(0*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+30) has been rung.
	29	**Doorbell #(0*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+29) has been rung.
	28	**Doorbell #(0*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+28) has been rung.
	27	**Doorbell #(0*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+27) has been rung.
	26	**Doorbell #(0*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+26) has been rung.
	25	**Doorbell #(0*32+25) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+25) has been rung.
	24	**Doorbell #(0*32+24) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+24) has been rung.

DRB0ACT - Active Doorbell Register 0

23	**Doorbell #(0*32+23) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+23) has been rung.
22	**Doorbell #(0*32+22) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+22) has been rung.
21	**Doorbell #(0*32+21) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+21) has been rung.
20	**Doorbell #(0*32+20) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+20) has been rung.
19	**Doorbell #(0*32+19) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+19) has been rung.
18	**Doorbell #(0*32+18) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+18) has been rung.
17	**Doorbell #(0*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+17) has been rung.
16	**Doorbell #(0*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+16) has been rung.
15	**Doorbell #(0*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+15) has been rung.
14	**Doorbell #(0*32+14) Active** Access: RO

DRB0ACT - Active Doorbell Register 0

		_Custom_GTIReset: BUS Doorbell #(0*32+14) has been rung.
	13	**Doorbell #(0*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+13) has been rung.
	12	**Doorbell #(0*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+12) has been rung.
	11	**Doorbell #(0*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+11) has been rung.
	10	**Doorbell #(0*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+10) has been rung.
	9	**Doorbell #(0*32+9) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+9) has been rung.
	8	**Doorbell #(0*32+8) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+8) has been rung.
	7	**Doorbell #(0*32+7) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+7) has been rung.
	6	**Doorbell #(0*32+6) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+6) has been rung.
	5	**Doorbell #(0*32+5) Active** Access: RO _Custom_GTIReset: BUS

DRB0ACT - Active Doorbell Register 0

		Doorbell #(0*32+5) has been rung.
	4	**Doorbell #(0*32+4) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+4) has been rung.
	3	**Doorbell #(0*32+3) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+3) has been rung.
	2	**Doorbell #(0*32+2) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+2) has been rung.
	1	**Doorbell #(0*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+1) has been rung.
	0	**Doorbell #(0*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+0) has been rung.

Active Doorbell Register 1

DRB1ACT - Active Doorbell Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01904h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(1*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+31) has been rung.
	30	**Doorbell #(1*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+30) has been rung.
	29	**Doorbell #(1*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+29) has been rung.
	28	**Doorbell #(1*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+28) has been rung.
	27	**Doorbell #(1*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+27) has been rung.
	26	**Doorbell #(1*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+26) has been rung.

DRB1ACT - Active Doorbell Register 1

	25	**Doorbell #(1*32+25) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+25) has been rung.
	24	**Doorbell #(1*32+24) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+24) has been rung.
	23	**Doorbell #(1*32+23) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+23) has been rung.
	22	**Doorbell #(1*32+22) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+22) has been rung.
	21	**Doorbell #(1*32+21) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+21) has been rung.
	20	**Doorbell #(1*32+20) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+20) has been rung.
	19	**Doorbell #(1*32+19) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+19) has been rung.
	18	**Doorbell #(1*32+18) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+18) has been rung.

DRB1ACT - Active Doorbell Register 1

17	**Doorbell #(1*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+17) has been rung.
16	**Doorbell #(1*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+16) has been rung.
15	**Doorbell #(1*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+15) has been rung.
14	**Doorbell #(1*32+14) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+14) has been rung.
13	**Doorbell #(1*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+13) has been rung.
12	**Doorbell #(1*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+12) has been rung.
11	**Doorbell #(1*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+11) has been rung.
10	**Doorbell #(1*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+10) has been rung.

DRB1ACT - Active Doorbell Register 1

9	**Doorbell #(1*32+9) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+9) has been rung.
8	**Doorbell #(1*32+8) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+8) has been rung.
7	**Doorbell #(1*32+7) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+7) has been rung.
6	**Doorbell #(1*32+6) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+6) has been rung.
5	**Doorbell #(1*32+5) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+5) has been rung.
4	**Doorbell #(1*32+4) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+4) has been rung.
3	**Doorbell #(1*32+3) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+3) has been rung.
2	**Doorbell #(1*32+2) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+2) has been rung.

DRB1ACT - Active Doorbell Register 1

	1	**Doorbell #(1*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+1) has been rung.
	0	**Doorbell #(1*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+0) has been rung.

Active Doorbell Register 2

DRB2ACT - Active Doorbell Register 2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01908h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(2*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+31) has been rung.
	30	**Doorbell #(2*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+30) has been rung.
	29	**Doorbell #(2*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+29) has been rung.
	28	**Doorbell #(2*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+28) has been rung.
	27	**Doorbell #(2*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+27) has been rung.
	26	**Doorbell #(2*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+26) has been rung.

DRB2ACT - Active Doorbell Register 2

25	**Doorbell #(2*32+25) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+25) has been rung.	
24	**Doorbell #(2*32+24) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+24) has been rung.	
23	**Doorbell #(2*32+23) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+23) has been rung.	
22	**Doorbell #(2*32+22) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+22) has been rung.	
21	**Doorbell #(2*32+21) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+21) has been rung.	
20	**Doorbell #(2*32+20) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+20) has been rung.	
19	**Doorbell #(2*32+19) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+19) has been rung.	
18	**Doorbell #(2*32+18) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+18) has been rung.	

DRB2ACT - Active Doorbell Register 2

	17	**Doorbell #(2*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+17) has been rung.
	16	**Doorbell #(2*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+16) has been rung.
	15	**Doorbell #(2*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+15) has been rung.
	14	**Doorbell #(2*32+14) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+14) has been rung.
	13	**Doorbell #(2*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+13) has been rung.
	12	**Doorbell #(2*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+12) has been rung.
	11	**Doorbell #(2*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+11) has been rung.
	10	**Doorbell #(2*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+10) has been rung.

DRB2ACT - Active Doorbell Register 2

9	**Doorbell #(2*32+9) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+9) has been rung.	
8	**Doorbell #(2*32+8) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+8) has been rung.	
7	**Doorbell #(2*32+7) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+7) has been rung.	
6	**Doorbell #(2*32+6) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+6) has been rung.	
5	**Doorbell #(2*32+5) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+5) has been rung.	
4	**Doorbell #(2*32+4) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+4) has been rung.	
3	**Doorbell #(2*32+3) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+3) has been rung.	
2	**Doorbell #(2*32+2) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(2*32+2) has been rung.	

DRB2ACT - Active Doorbell Register 2

	1	**Doorbell #(2*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+1) has been rung.
	0	**Doorbell #(2*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+0) has been rung.

Active Doorbell Register 3

DRB3ACT - Active Doorbell Register 3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0190Ch	
DWord	**Bit**	**Description**
0	31	**Doorbell #(3*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+31) has been rung.
	30	**Doorbell #(3*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+30) has been rung.
	29	**Doorbell #(3*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+29) has been rung.
	28	**Doorbell #(3*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+28) has been rung.
	27	**Doorbell #(3*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+27) has been rung.
	26	**Doorbell #(3*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+26) has been rung.

DRB3ACT - Active Doorbell Register 3

25	**Doorbell #(3*32+25) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+25) has been rung.
24	**Doorbell #(3*32+24) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+24) has been rung.
23	**Doorbell #(3*32+23) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+23) has been rung.
22	**Doorbell #(3*32+22) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+22) has been rung.
21	**Doorbell #(3*32+21) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+21) has been rung.
20	**Doorbell #(3*32+20) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+20) has been rung.
19	**Doorbell #(3*32+19) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+19) has been rung.
18	**Doorbell #(3*32+18) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+18) has been rung.

DRB3ACT - Active Doorbell Register 3

17	**Doorbell #(3*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+17) has been rung.
16	**Doorbell #(3*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+16) has been rung.
15	**Doorbell #(3*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+15) has been rung.
14	**Doorbell #(3*32+14) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+14) has been rung.
13	**Doorbell #(3*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+13) has been rung.
12	**Doorbell #(3*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+12) has been rung.
11	**Doorbell #(3*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+11) has been rung.
10	**Doorbell #(3*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+10) has been rung.

DRB3ACT - Active Doorbell Register 3

9	**Doorbell #(3*32+9) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+9) has been rung.	
8	**Doorbell #(3*32+8) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+8) has been rung.	
7	**Doorbell #(3*32+7) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+7) has been rung.	
6	**Doorbell #(3*32+6) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+6) has been rung.	
5	**Doorbell #(3*32+5) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+5) has been rung.	
4	**Doorbell #(3*32+4) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+4) has been rung.	
3	**Doorbell #(3*32+3) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+3) has been rung.	
2	**Doorbell #(3*32+2) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(3*32+2) has been rung.	

DRB3ACT - Active Doorbell Register 3

	1	**Doorbell #(3*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+1) has been rung.
	0	**Doorbell #(3*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+0) has been rung.

Active Doorbell Register 4

DRB4ACT - Active Doorbell Register 4		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01910h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(4*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+31) has been rung.
	30	**Doorbell #(4*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+30) has been rung.
	29	**Doorbell #(4*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+29) has been rung.
	28	**Doorbell #(4*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+28) has been rung.
	27	**Doorbell #(4*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+27) has been rung.
	26	**Doorbell #(4*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+26) has been rung.

DRB4ACT - Active Doorbell Register 4

25	**Doorbell #(4*32+25) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+25) has been rung.	
24	**Doorbell #(4*32+24) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+24) has been rung.	
23	**Doorbell #(4*32+23) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+23) has been rung.	
22	**Doorbell #(4*32+22) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+22) has been rung.	
21	**Doorbell #(4*32+21) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+21) has been rung.	
20	**Doorbell #(4*32+20) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+20) has been rung.	
19	**Doorbell #(4*32+19) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+19) has been rung.	
18	**Doorbell #(4*32+18) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+18) has been rung.	

DRB4ACT - Active Doorbell Register 4

17	**Doorbell #(4*32+17) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+17) has been rung.	
16	**Doorbell #(4*32+16) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+16) has been rung.	
15	**Doorbell #(4*32+15) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+15) has been rung.	
14	**Doorbell #(4*32+14) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+14) has been rung.	
13	**Doorbell #(4*32+13) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+13) has been rung.	
12	**Doorbell #(4*32+12) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+12) has been rung.	
11	**Doorbell #(4*32+11) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+11) has been rung.	
10	**Doorbell #(4*32+10) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(4*32+10) has been rung.	

DRB4ACT - Active Doorbell Register 4

	9	**Doorbell #(4*32+9) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+9) has been rung.
	8	**Doorbell #(4*32+8) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+8) has been rung.
	7	**Doorbell #(4*32+7) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+7) has been rung.
	6	**Doorbell #(4*32+6) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+6) has been rung.
	5	**Doorbell #(4*32+5) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+5) has been rung.
	4	**Doorbell #(4*32+4) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+4) has been rung.
	3	**Doorbell #(4*32+3) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+3) has been rung.
	2	**Doorbell #(4*32+2) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+2) has been rung.

DRB4ACT - Active Doorbell Register 4

	1	**Doorbell #(4*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+1) has been rung.
	0	**Doorbell #(4*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+0) has been rung.

Active Doorbell Register 5

DRB5ACT - Active Doorbell Register 5		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01914h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(5*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+31) has been rung.
	30	**Doorbell #(5*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+30) has been rung.
	29	**Doorbell #(5*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+29) has been rung.
	28	**Doorbell #(5*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+28) has been rung.
	27	**Doorbell #(5*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+27) has been rung.
	26	**Doorbell #(5*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+26) has been rung.

DRB5ACT - Active Doorbell Register 5

25	**Doorbell #(5*32+25) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+25) has been rung.	
24	**Doorbell #(5*32+24) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+24) has been rung.	
23	**Doorbell #(5*32+23) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+23) has been rung.	
22	**Doorbell #(5*32+22) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+22) has been rung.	
21	**Doorbell #(5*32+21) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+21) has been rung.	
20	**Doorbell #(5*32+20) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+20) has been rung.	
19	**Doorbell #(5*32+19) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+19) has been rung.	
18	**Doorbell #(5*32+18) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(5*32+18) has been rung.	

DRB5ACT - Active Doorbell Register 5

	17	**Doorbell #(5*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+17) has been rung.
	16	**Doorbell #(5*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+16) has been rung.
	15	**Doorbell #(5*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+15) has been rung.
	14	**Doorbell #(5*32+14) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+14) has been rung.
	13	**Doorbell #(5*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+13) has been rung.
	12	**Doorbell #(5*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+12) has been rung.
	11	**Doorbell #(5*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+11) has been rung.
	10	**Doorbell #(5*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+10) has been rung.

DRB5ACT - Active Doorbell Register 5

9	**Doorbell #(5*32+9) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+9) has been rung.
8	**Doorbell #(5*32+8) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+8) has been rung.
7	**Doorbell #(5*32+7) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+7) has been rung.
6	**Doorbell #(5*32+6) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+6) has been rung.
5	**Doorbell #(5*32+5) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+5) has been rung.
4	**Doorbell #(5*32+4) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+4) has been rung.
3	**Doorbell #(5*32+3) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+3) has been rung.
2	**Doorbell #(5*32+2) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+2) has been rung.

DRB5ACT - Active Doorbell Register 5

	1	**Doorbell #(5*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+1) has been rung.
	0	**Doorbell #(5*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+0) has been rung.

Active Doorbell Register 6

DRB6ACT - Active Doorbell Register 6		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01918h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(6*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+31) has been rung.
	30	**Doorbell #(6*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+30) has been rung.
	29	**Doorbell #(6*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+29) has been rung.
	28	**Doorbell #(6*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+28) has been rung.
	27	**Doorbell #(6*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+27) has been rung.
	26	**Doorbell #(6*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+26) has been rung.

DRB6ACT - Active Doorbell Register 6

25	**Doorbell #(6*32+25) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+25) has been rung.
24	**Doorbell #(6*32+24) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+24) has been rung.
23	**Doorbell #(6*32+23) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+23) has been rung.
22	**Doorbell #(6*32+22) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+22) has been rung.
21	**Doorbell #(6*32+21) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+21) has been rung.
20	**Doorbell #(6*32+20) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+20) has been rung.
19	**Doorbell #(6*32+19) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+19) has been rung.
18	**Doorbell #(6*32+18) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+18) has been rung.

DRB6ACT - Active Doorbell Register 6

	17	**Doorbell #(6*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+17) has been rung.
	16	**Doorbell #(6*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+16) has been rung.
	15	**Doorbell #(6*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+15) has been rung.
	14	**Doorbell #(6*32+14) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+14) has been rung.
	13	**Doorbell #(6*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+13) has been rung.
	12	**Doorbell #(6*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+12) has been rung.
	11	**Doorbell #(6*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+11) has been rung.
	10	**Doorbell #(6*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+10) has been rung.

DRB6ACT - Active Doorbell Register 6

9	**Doorbell #(6*32+9) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+9) has been rung.	
8	**Doorbell #(6*32+8) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+8) has been rung.	
7	**Doorbell #(6*32+7) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+7) has been rung.	
6	**Doorbell #(6*32+6) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+6) has been rung.	
5	**Doorbell #(6*32+5) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+5) has been rung.	
4	**Doorbell #(6*32+4) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+4) has been rung.	
3	**Doorbell #(6*32+3) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+3) has been rung.	
2	**Doorbell #(6*32+2) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(6*32+2) has been rung.	

DRB6ACT - Active Doorbell Register 6

	1	**Doorbell #(6*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+1) has been rung.
	0	**Doorbell #(6*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+0) has been rung.

Active Doorbell Register 7

DRB7ACT - Active Doorbell Register 7

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0191Ch

DWord	Bit	Description
0	31	**Doorbell #(7*32+31) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+31) has been rung.
	30	**Doorbell #(7*32+30) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+30) has been rung.
	29	**Doorbell #(7*32+29) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+29) has been rung.
	28	**Doorbell #(7*32+28) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+28) has been rung.
	27	**Doorbell #(7*32+27) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+27) has been rung.
	26	**Doorbell #(7*32+26) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+26) has been rung.

DRB7ACT - Active Doorbell Register 7

25	**Doorbell #(7*32+25) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+25) has been rung.	
24	**Doorbell #(7*32+24) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+24) has been rung.	
23	**Doorbell #(7*32+23) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+23) has been rung.	
22	**Doorbell #(7*32+22) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+22) has been rung.	
21	**Doorbell #(7*32+21) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+21) has been rung.	
20	**Doorbell #(7*32+20) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+20) has been rung.	
19	**Doorbell #(7*32+19) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+19) has been rung.	
18	**Doorbell #(7*32+18) Active**	
	Access:	RO
	_Custom_GTIReset:	BUS
	Doorbell #(7*32+18) has been rung.	

DRB7ACT - Active Doorbell Register 7

	17	**Doorbell #(7*32+17) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+17) has been rung.
	16	**Doorbell #(7*32+16) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+16) has been rung.
	15	**Doorbell #(7*32+15) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+15) has been rung.
	14	**Doorbell #(7*32+14) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+14) has been rung.
	13	**Doorbell #(7*32+13) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+13) has been rung.
	12	**Doorbell #(7*32+12) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+12) has been rung.
	11	**Doorbell #(7*32+11) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+11) has been rung.
	10	**Doorbell #(7*32+10) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+10) has been rung.

DRB7ACT - Active Doorbell Register 7

9	**Doorbell #(7*32+9) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+9) has been rung.
8	**Doorbell #(7*32+8) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+8) has been rung.
7	**Doorbell #(7*32+7) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+7) has been rung.
6	**Doorbell #(7*32+6) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+6) has been rung.
5	**Doorbell #(7*32+5) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+5) has been rung.
4	**Doorbell #(7*32+4) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+4) has been rung.
3	**Doorbell #(7*32+3) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+3) has been rung.
2	**Doorbell #(7*32+2) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+2) has been rung.

DRB7ACT - Active Doorbell Register 7

	1	**Doorbell #(7*32+1) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+1) has been rung.
	0	**Doorbell #(7*32+0) Active** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+0) has been rung.

Active Head Pointer Register

ACTHD - Active Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
_Custom_GTIStorage:	FLOP
Address:	02074h-02077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_RCSUNIT
Address:	18074h-18077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_POCSUNIT
Address:	22074h-22077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_BCSUNIT
Address:	1C0074h-1C0077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT0
Address:	1C4074h-1C4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT1
Address:	1C8074h-1C8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT0
Address:	1D0074h-1D0077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT2
Address:	1D4074h-1D4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT3
Address:	1D8074h-1D8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT1
Address:	1E0074h-1E0077h
Name:	Active Head Pointer Register

ACTHD - Active Head Pointer Register

ShortName:	ACTHD_VCSUNIT4
Address:	1E4074h-1E4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT5
Address:	1E8074h-1E8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT2
Address:	1F0074h-1F0077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT6
Address:	1F4074h-1F4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT7
Address:	1F8074h-1F8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT3
Address:	1A074h-1A077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_CCSUNIT0

This register contains the address details of the data dword being parsed by command streamer.

- When the commands are being executed from a batch buffer this register contains the Dword aligned Graphics Memory Address.
- When the commands are being executed from a ring buffer this register contains the Dword aligned offset into the ring buffer (offset from Ring Buffer start address).

DWord	Bit	Description
0	31:2	**Head Pointer** Format: GraphicsAddress[31:2] • When the commands are being executed from a batch buffer this register contains the Dword aligned Graphics Memory Address. • When the commands are being executed from a ring buffer this register contains the Dword aligned offset into the ring buffer (offset from Ring Buffer start address).
	1:0	**Reserved** Access: RO Format: MBZ

Advanced Scheduler Reset Request Messages

SSRREQ - Advanced Scheduler Reset Request Messages

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 0810Ch

Hardware (CS, VCS) initiated Advanced Scheduler reset request messages.

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:14	**Reserved** Access: RO Format: MBZ
	13	**SFC3 gracefull reset request message** Access: R/W Set _Custom_GTIReset: BUS SFC3 gracefull Reset Request Message for 2nd Vbox: '1' : cmsfc Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : cmsfc Reset Not Requested
	12	**SFC2 gracefull reset request message** Access: R/W Set _Custom_GTIReset: BUS SFC2 gracefull Reset Request Message for 2nd Vbox: '1' : cmsfc Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : cmsfc Reset Not Requested
	11	**SFC1 gracefull reset request message (2nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS SFC1 gracefull Reset Request Message for 2nd Vbox: '1' : cmsfc Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : cmsfc Reset Not Requested

SSRREQ - Advanced Scheduler Reset Request Messages

	10	**SFC0 gracefull reset request message (1st Vbox)** Access: R/W Set _Custom_GTIReset: BUS SFC0 gracefull Reset Request Message for 1st Vbox: '1' : cmsfc Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : cmsfc Reset Not Requested
	9	**VINunit cmfxrst reset request message (8nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 8nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	8	**VINunit cmfxrst reset request message (7nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 7nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	7	**VINunit cmfxrst reset request message (6nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 6nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	6	**VINunit cmfxrst reset request message (5nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 5nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	5	**VINunit cmfxrst reset request message (4nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 4nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request

SSRREQ - Advanced Scheduler Reset Request Messages

		'0' : CMFX Reset Not Requested
	4	**VINunit cmfxrst reset request message (3nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 3nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	3	**VINunit cmfxrst reset request message (2nd Vbox)** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit in 2nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	2	**VINunit cmfxrst Reset Request message** Access: R/W Set _Custom_GTIReset: BUS CMFX Reset Request Message from the VINunit: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	1	**Render AS Reset Request Message** Access: R/W Set _Custom_GTIReset: BUS Render AS Reset Request Message from the CSunit: '1' : Render AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Render AS Reset Not Requested
	0	**Media AS Reset Request Message** Access: R/W Set _Custom_GTIReset: BUS Media AS Reset Request Message from the VCSunit: '1' : Media AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Media AS Reset Not Requested

Aggregate Perf Counter SPM0 Lower DWord Free

OAPERF_SPM0_LOWER_FREE - Aggregate Perf Counter SPM0 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02980h

This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter SPM0 Upper DWord Free

OAPERF_SPM0_UPPER_FREE - Aggregate Perf Counter SPM0 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02984h

This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC _Custom_GTIReset: DEV
	7:0	**Upper Value** Format: U8 _Custom_GTIReset: DEV This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter SPM1 Lower DWord Free

OAPERF_SPM1_LOWER_FREE - Aggregate Perf Counter SPM1 Lower DWord Free		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02988h	
This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter SPM1 Upper DWord Free

OAPERF_SPM1_UPPER_FREE - Aggregate Perf Counter SPM1 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0298Ch

This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC _Custom_GTIReset: DEV
	7:0	**Upper Value** Format: U8 _Custom_GTIReset: DEV This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

ARAT C6 Disallow Threshold

ARAT_C6DIS - ARAT C6 Disallow Threshold		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 0A178h		
DWord	**Bit**	**Description**
0	31:0	**C6 Disallow Threshold for ARAT** Access: R/W _Custom_GTIReset: DEV Threshold, in 10ns increments to prevent short C6.

ARAT Delta (LSB)

ARAT_TDELTA_LOW - ARAT Delta (LSB)		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A174h	
DWord	**Bit**	**Description**
0	31:2	**Lower Bits of Delta Time for ARAT** Access: R/W _Custom_GTIReset: DEV Bits [31:2] of Delta Time, in 10ns increments. Bits 1:0 dropped. This means the granularity is 40ns increments. For example, [31:2]=b1 means the delta time is 40ns.
	1	**ARAT Mode** Access: R/W _Custom_GTIReset: DEV 0b: One-Shot Mode (default). 1b: Periodic Mode.
	0	**ARAT Enable** Access: R/W _Custom_GTIReset: DEV 0b: ARAT Disabled (default). 1b: ARAT Enabled.

ARB_CTL

ARB_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45000h-45003h
Name:	Display Arbitration Control 1
ShortName:	ARB_CTL
Reset:	soft
Address:	45800h-45803h
Name:	Display Arbitration Control 1 Abox 1
ShortName:	ARB_CTL_ABOX1
Reset:	soft
Address:	45808h-4580Bh
Name:	Display Arbitration Control 1 Abox 2
ShortName:	ARB_CTL_ABOX2
Reset:	soft

DWord	Bit	Description
0	31	**FBC Memory Wake** Setting this bit allows FBC compressed write requests to wake memory. Value: 1b — Name: Wake On **[Default]** Value: 0b — Name: Wake Off
	30	**Reserved**
	29	**Reserved** Access: RO Format: MBZ
	28:26	**HP Queue Watermark** The value in this register indicates the number of entries the high priority queue should have before it can be read. The value is zero based. Program the values as N-1, where 3'b011 indicates 4 entries. Value: 011b — Name: 4 entries **[Default]** Value: [0,7] — Name:
	25:24	**LP Write Request Limit** The value in this register indicates the maximum number of back-to-back LP write requests that will be accepted from a single client before re-arbitrating.

ARB_CTL

Value	Name
00b	1
01b	2
10b	4 **[Default]**
11b	8

23:20 **TLB Request Limit**

The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Zero is not a valid programming.

Value	Name
0110b	6 **[Default]**
[1,15]	

19:16 **TLB Request InFlight Limit**

The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Zero is not a valid programming.

Value	Name
0110b	6 **[Default]**
[1,15]	

15 **FBC Watermark Disable**

Setting this bit disables the FBC watermarks.

Value	Name
0b	Enable
1b	Disable

14:13 **Tiled Address Swizzling**

DRAM configuration registers show if memory address swizzling is needed.

Value	Name	Description
00b	No Display	No display request address swizzling
01b	Reserved	Address bit[6] swizzling for tiled surfaces is not used
10b	Reserved	
11b	Reserved	

12:8 **HP Page Break Limit**

The value in this register represents the maximum number of page breaks allowed in a HP request chain. Zero is not a valid programming.

Value	Name
10000b	16 **[Default]**
[1,31]	

7 **Reserved**

Access:	RO
Format:	MBZ

ARB_CTL

	6:0	**HP Data Request Limit** The value in this register represents the maximum number of cachelines allowed in a HP request chain. **Value** / **Name** 1010110b / 86 **[Default]** [1,127] / **Restriction** This value must always be programmed greater than 8.

ARB_CTL2

ARB_CTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45004h-45007h
Name:	Display Arbitration Control 2
ShortName:	ARB_CTL2
Reset:	soft
Address:	45804h-45807h
Name:	Display Arbitration Control 2 Abox 1
ShortName:	ARB_CTL2_ABOX1
Reset:	soft
Address:	4580Ch-4580Fh
Name:	Display Arbitration Control 2 Abox 2
ShortName:	ARB_CTL2_ABOX2
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved** Access: RO Format: MBZ
	29:28	**LP WD Write Request Limit** The value in this register indicates the maximum number of back to back LP write requests that will be accepted from WD before re-arbitrating. Value / Name: 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	27:26	**DSB LP Write Request Limit** The value in this register indicates the maximum number of back to back DSB LP write requests that will be accepted by a single client before re-arbitrating. Value / Name: 00b: 1 01b: 2 10b: 4 **[Default]**

ARB_CTL2

	11b	8

25:23 Reserved

Access:	RO
Format:	MBZ

22:20 Reserved

Access:	RO
Format:	MBZ

19:18 Par5 Request Limit

This field sets the maximum number of par5 requests before arbitration switches to another client.

Value	Name
00b	1
01b	2
10b	4 **[Default]**
11b	16

17:16 FBC Request Limit

This field sets the maximum number of FBC requests before arbitration switches to another client.

Value	Name
00b	1
01b	2 **[Default]**
10b	4
11b	8

15:14 Reserved

Access:	RO
Format:	MBZ

13 Reserved

12 Arbiter Trickle Feed Allow On HP Request

If enabled, Arbiter will allow trickle feed request from all clients if any of the client sends a high priority request

Value	Name
0b	Disable **[Default]**
1b	Enable

11 Reserved

10:9 Inflight LP Read Request Limit

The value in this register represents the maximum number of LP read request transactions that can be inflight at any given time.

ARB_CTL2

Value	Name
00b	1 LP
01b	2 LP
10b	3 LP
11b	4 LP **[Default]**

8:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Inflight HP Read Request Limit**

The value in this register represents the maximum number of HP read request transactions that can be inflight at any given time.

Value	Name
00b	128 HP
01b	64 HP
10b	32 HP
11b	16 HP

3 **Enable IPC**

Enables the Isochronous Priority Control. If enabled, Display sends demoted requests once the transition watermark is reached. If transition watermark is not enabled, Display sends demoted requests when the display buffer is full.

Value	Name
0b	Disable
1b	Enable

Programming Notes
This field is not connected in ARB_CTL2_ABOX1 andARB_CTL2_ABOX2. The "Enable IPC" field in ARB_CTL2 enables/disabled IPC in all ABOXs.

2 **Reserved**

Access:	RO
Format:	MBZ

1:0 **RTID FIFO Watermark**

The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark.

Value	Name
00b	8 RTIDs
01b	16 RTIDs
10b	32 RTIDs
11b	Reserved

ASL Storage

ASLS_0_2_0_PCI - ASL Storage

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	000FCh

This is a software scratch register. The exact bit register usage must be worked out in common between System BIOS and driver software. For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

DWord	Bit	Description
0	31:0	**Device Switching Storage** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS Software controlled usage to support device switching.

ATS Capability

ATS_CAP_0_2_0_PCI - ATS Capability

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00204h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

DWord	Bit	Description
0	15:7	**Reserved** Access: RO Format: MBZ
	6	**Global Invalidate Supported** Default Value: 1b Access: RO _Custom_GTIReset: BUS If Set, the Function supports Invalidation Requests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate requests. Reserved
	5	**Page Aligned Request** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.
	4:0	**Invalidate Queue Depth** Default Value: 00000b Access: RO _Custom_GTIReset: BUS The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.

ATS Control

ATS_CTRL_0_2_0_PCI - ATS Control

Register Space: PCI: 0/2/0
Size (in bits): 16

Address: 00206h

DWord	Bit	Description
0	15	**ATS Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemented as RW as software can read it to determine ATS enable status.
	14:5	**Reserved** Access: RO Format: MBZ
	4:0	**Smallest Translation Unit** Default Value: 00000b Access: R/W _Custom_GTIReset: BUS This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^STU. A value of 0 indicates one block and value 1F indicates 2^31 blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.

ATS Extended Capability Header

ATS_EXTCAP_0_2_0_PCI - ATS Extended Capability Header

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00200h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ats specification.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 001100000000b Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000001111b Access: RO _Custom_GTIReset: BUS Hardwired to the ATS Extended Capability ID

AUD_CONFIG

AUD_CONFIG	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65000h-65003h
Name:	Audio Configuration Transcoder A
ShortName:	AUD_TCA_CONFIG
Reset:	soft
Address:	65100h-65103h
Name:	Audio Configuration Transcoder B
ShortName:	AUD_TCB_CONFIG
Reset:	soft
Address:	65200h-65203h
Name:	Audio Configuration Transcoder C
ShortName:	AUD_TCC_CONFIG
Reset:	soft
Address:	65300h-65303h
Name:	Audio Configuration Transcoder D
ShortName:	AUD_TCD_CONFIG
Reset:	soft

This register configures the audio output. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**N value Index** 0b – HDMI **[Default]** – N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set. 1b – DisplayPort – N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000 when bit 28 is not set.

AUD_CONFIG

28	**N programming enable** This bit enables programming of N values for non-CEA modes. Please note that the transcoder to which audio is attached must be disabled when changing this field.
27:20	**Upper N value** Default Value: 00000111b These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values.
19:16	**Pixel Clock HDMI** This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming. Note: The transcoder on which audio is attached must be disabled when changing this field.

Value	Name	Description
0b	**[Default]**	
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz
0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)
0010b	27 MHz	27 MHz
0011b	27 * 1.001 MHz	27 * 1.001 MHz
0100b	54 MHz	54 MHz
0101b	54 * 1.001 MHz	54 * 1.001 MHz
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz
0111b	74.25 MHz	74.25 MHz
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz
1001b	148.5 MHz	148.5 MHz
1010b	297 / 1.001 MHz	297 / 1.001 MHz
1011b	297 MHz	297 MHz
1100b	594 / 1.001 MHz	594 / 1.001 MHz
1101b	594 MHz	594 MHz
Others	Reserved	Reserved

15:4	**Lower N value** Default Value: 111110100110b These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
3	**Reserved**
2:0	**Reserved** Access: RO Format: MBZ

AUD_CONFIG_2

AUD_CONFIG_2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65004h-65007h
Name:	Audio Configuration Register 2 Transcoder A
ShortName:	AUD_TCA_CONFIG_2
Reset:	soft
Address:	65104h-65107h
Name:	Audio Configuration Register 2 Transcoder B
ShortName:	AUD_TCB_CONFIG_2
Reset:	soft
Address:	65204h-65207h
Name:	Audio Configuration Register 2 Transcoder C
ShortName:	AUD_TCC_CONFIG_2
Reset:	soft
Address:	65304h-65307h
Name:	Audio Configuration Register 2 Transcoder D
ShortName:	AUD_TCD_CONFIG_2
Reset:	soft

This is a new register to add 297 and 584MHz frequencies support for HDMI TMDS clocks. These are programmed along with the other lower bits of the N and CTS values in the Audio Config register. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31	**Reserved**
	30:21	**Reserved** Access: RO Format: MBZ
	20:16	**DPSpecVersion** Default Value: 00010010b DP spec version number that goes in the header of the samples. Default 12h for DP MST. Currently DP Compliance is expecting this field to be 00010001 (DP1.1) as the Compliance spec has not been updated. SW must program this register to "00010001" to overcome this compliance failure. This programming can be updated after the Compliance Specification is updated.

AUD_CONFIG_2		
	15:12	**Reserved** Access: RO Format: MBZ
	11:8	**Upper bits for N value** These are bits are concatenated as the upper 4 bits to the N value in the AUD_CONFIG register. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
	7:4	**Reserved** Access: RO Format: MBZ
	3:0	**Upper bits for MCTS value** These are the upper 4bits concatenated to CTS or M generation for CTM modes.

AUD_CONFIG_BE

AUD_CONFIG_BE

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

Address: 65EF0h-65EF3h
Name: Audio Config Register for Dacbeunit
ShortName: AUD_CONFIG_BE
Reset: soft

DWord	Bit	Description
0	31	**Delay sample count latch Pipe D** Access: R/W Pipe D Hblank SM arc delay for samplecount. Value / Name / Description: 0b / Delay by 16 clocks **[Default]** / When set to 0, sample count latch is delayed by 16 clocks after Hblank starts. 1b / Delay by 32 clocks / When set to 1, sample count latch is delayed by 32 clocks after Hblank starts.
	30	**Delay sample count latch Pipe C** Access: R/W Pipe C Hblank SM arc delay for samplecount. Value / Name / Description: 0b / Delay by 16 clocks **[Default]** / When set to 0, sample count latch is delayed by 16 clocks after Hblank starts. 1b / Delay by 32 clocks / When set to 1, sample count latch is delayed by 32 clocks after Hblank starts.
	29	**Delay sample count latch Pipe B** Access: R/W Pipe B Hblank SM arc delay for samplecount. Value / Name / Description: 0b / Delay by 16 clocks **[Default]** / When set to 0, sample count latch is delayed by 16 clocks after Hblank starts. 1b / Delay by 32 clocks / When set to 1, sample count latch is delayed by 32 clocks after Hblank starts.
	28	**Delay sample count latch Pipe A** Access: R/W Pipe A Hblank SM arc delay for samplecount.

Value	Name	Description
0b	Delay by 16 clocks **[Default]**	When set to 0, sample count latch is delayed by 16 clocks after Hblank starts.
1b	Delay by 32 clocks	When set to 1, sample count latch is delayed by 32 clocks after Hblank starts.

27 **HBlank Early Enable for PipeD**

Access:	R/W

Enables using the HBlank_start count bit-field value for triggering the samplecount calculation.

Value	Name	Description
0b	Hblank Early Disable **[Default]**	The default Hblank is used and a delay of 16 tcclks is added before the SM arcs during each hblank for Pipe D
1b	Hblank Early Enable	The early hblank programmed by fields hblank_start count for Pipe D will be used to trigger samplecount calculation for Pipe D.

26 **HBlank Early Enable for PipeC**

Access:	R/W

Enables using the HBlank_start count bit-field value for triggering the samplecount calculation.

Value	Name	Description
0b	Hblank Early Disable **[Default]**	The default Hblank is used and a delay of 16 tcclks is added before the SM arcs during each hblank for Pipe C
1b	Hblank Early Enable	The early hblank programmed by fields hblank_start count for Pipe C will be used to trigger samplecount calculation for Pipe C.

25 **HBlank Early Enable for PipeB**

Access:	R/W

Enables using the HBlank_start count bit-field value for triggering the samplecount calculation.

Value	Name	Description
0b	Hblank Early Disable **[Default]**	The default Hblank is used and a delay of 16 tcclks is added before the SM arcs during each hblank for Pipe B
1b	Hblank Early Enable	The early hblank programmed by fields hblank_start count for Pipe B will be used to trigger samplecount calculation for Pipe B.

24 **HBlank Early Enable for PipeA**

Access:	R/W

Enables using the HBlank_start count bit-field value for triggering the samplecount calculation.

Value	Name	Description
0b	Hblank Early Disable **[Default]**	The default Hblank is used and a delay of 16 tcclks is added before the SM arcs during each hblank for Pipe A.
1b	Hblank Early Enable	The early hblank programmed by fields hblank_start count for Pipe A will be used to trigger samplecount calculation for Pipe A.

AUD_CONFIG_BE

23:21 HBlank_start count for Pipe D

Access:	R/W

The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tcaclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tcaclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tcaclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tcaclks	Hblank is generated 64 tcclks early.
100b	Delay of 96 tcaclks	Hblank is generated 96 tcclks early.
101b	Delay of 128 tcaclks	Hblank is generated 128 tcclks early.

20 DP Mixer Mainstream priority enable for Pipe D

Access:	R/W

When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank..

19:18 Number of samples per line for Pipe D

Access:	R/W

When prorgammed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.
01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

17:15 HBlank_start count for Pipe C

Access:	R/W

The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tccclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tccclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tccclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tccclks	Hblank is generated 64 tcclks early.
100b	Delay of 96 tccclks	Hblank is generated 96 tcclks early.
101b	Delay of 128 tccclks	Hblank is generated 128 tcclks early.

AUD_CONFIG_BE

	14	**DP Mixer Mainstream priority enable for Pipe C** Access: R/W When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank..
	13:12	**Number of samples per line for Pipe C** Access: R/W When prorgammed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.
01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

	11:9	**HBlank_start count for Pipe B** Access: R/W The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tcbclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tcbclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tcbclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tcbclks	Hblank is generated 64 tcclks early.
100b	Delay of 96 tcbclks	Hblank is generated 96 tcclks early.
101b	Delay of 128 tcbclks	Hblank is generated 128 tcclks early.

	8	**DP Mixer Mainstream priority enable for Pipe B** Access: R/W When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank..
	7:6	**Number of samples per line for Pipe B** Access: R/W When programmed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.

		01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
		10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

5:3 HBlank_start count for Pipe A

Access:	R/W

The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tcaclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tcaclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tcaclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tcaclks	Hblank is generated 64 tcclks early.
100b	Delay of 96 tcaclks	Hblank is generated 96 tcclks early.
101b	Delay of 128 tcaclks	Hblank is generated 128 tcclks early.

2 DP Mixer Mainstream priority enable for Pipe A

Access:	R/W

When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank.

1:0 Number of samples per line for Pipe A

Access:	R/W

When programmed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.
01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

AUD_DIP_ELD_CTRL_ST

AUD_DIP_ELD_CTRL_ST

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	650B4h-650B7h
Name:	Audio Control State for DIP and ELD Transcoder A
ShortName:	AUD_TCA_DIP_ELD_CTRL_ST
Reset:	soft
Address:	651B4h-651B7h
Name:	Audio Control State for DIP and ELD Transcoder B
ShortName:	AUD_TCB_DIP_ELD_CTRL_ST
Reset:	soft
Address:	652B4h-652B7h
Name:	Audio Control State for DIP and ELD Transcoder C
ShortName:	AUD_TCC_DIP_ELD_CTRL_ST
Reset:	soft
Address:	653B4h-653B7h
Name:	Audio Control State for DIP and ELD Transcoder D
ShortName:	AUD_TCD_DIP_ELD_CTRL_ST
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:28	**DIP Port Select** Access: RO This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. For DP MST, this is the device select/pipe select.

Value	Name	Description
0000b	Reserved **[Default]**	Reserved
0001b	Digital Port B	Digital Port B
0010b	Digital Port C	Digital Port C
0011b	USBC1	USBC1
0100b	USBC2	USBC2
0101b	USBC3	USBC3
0110b	USBC4	USBC4

0111b	USBC5	USBC5
1000b	USBC6	USBC6

27:25 **Reserved**

Access:	RO
Format:	MBZ

24:21 **DIP type enable status**

Access:	RO

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description
0000b	**[Default]**	
XXX0b	DIP Disable	Audio DIP disabled
XXX1b	DIP Enable	Audio DIP enabled
XX0Xb	ACP Disable	Generic 1 (ACP) DIP disabled
XX1Xb	ACP Enable	Generic 1 (ACP) DIP enabled
X0XXb	Generic 2 Disable	Generic 2 DIP disabled
X1XXb	Generic 2 Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
1XXXb	Reserved	Reserved

20:18 **DIP buffer index**

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s.

Value	Name	Description
000b	Audio **[Default]**	Audio DIP (31 bytes of address space, 31 bytes of data)
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)
Others	Reserved	Reserved

17:16 **DIP transmission frequency**

Access:	RO

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

AUD_DIP_ELD_CTRL_ST

		Value / **Name** / **Description** 00b / Disable **[Default]** / Disabled 01b / Reserved / Reserved 10b / Send Once / Send Once 11b / Best Effort / Best effort (Send at least every other vsync)
	15	**Reserved** Access: RO Format: MBZ
	14:10	**ELD buffer size** Default Value: 10101b Access: RO This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
	9:5	**ELD access address** Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.
	4	**ELD ACK** Acknowledgement from the audio driver that ELD read has been completed
	3:0	**DIP access address** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_EDID_DATA

AUD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65050h-65053h
Name:	Audio EDID Data Block Transcoder A
ShortName:	AUD_TCA_EDID_DATA
Reset:	soft
Address:	65150h-65153h
Name:	Audio EDID Data Block Transcoder B
ShortName:	AUD_TCB_EDID_DATA
Reset:	soft
Address:	65250h-65253h
Name:	Audio EDID Data Block Transcoder C
ShortName:	AUD_TCC_EDID_DATA
Reset:	soft
Address:	65350h-65353h
Name:	Audio EDID Data Block Transcoder D
ShortName:	AUD_TCD_EDID_DATA
Reset:	soft

These registers contain the HDMI/DP data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get HDMI/DP Widget command. Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.
- Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

AUD_EDID_DATA

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:0	**EDID Data Block** Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during FLR.

AUD_FREQ_CNTRL

AUD_FREQ_CNTRL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	65900h-65903h
Name:	Audio BCLK Frequency Control
ShortName:	AUD_FREQ_CNTRL
Reset:	soft

Please refer "Audio Link Settings" of the **"Audio Bios Programming Sequence"** section for details about per-project programming requirements for this register.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:14	**T-Mode** Indicates the T mode SDI is operating in. BIOS or System Software must pre-program the T-mode register.a. before the iDISPLAY Audio Link is brought out from Link Reset,b. to a value which is consistent with the value of the its counterpart T-mode bit in the Audio Controller.c. to a value which is within the electrical capabilities of the platform. Note that even T modes are prohibited from being used with any BCLK frequency which has an odd number of bit cells. Example, 2T mode is incompatible with BCLK=6MHz (125 bit cells). **Value** / **Name** / **Description** 00b / 4T / 4T mode with sdi data held for 4 bit clks. 01b / 2T / 2T Mode with sdi data held for 2 bit clocks. To use 2T mode, the bclk has to be 48MHz and flop in the IO needs to bypass by setting bit 13 of this register. BIOS has to program 48MHz in the controller also to use this mode. 10b / 8T **[Default]** / 8T Mode with sdi data held for 8 bit clocks. 11b / 16T / 16T Mode with sdi data held for 16 bit clocks.
	13	**Bypass Flop** Setting this bit will bypass the flop in the IO in the Audout path. **Value** / **Name** / **Description** 0b / No bypass **[Default]** / Flop in the AUDIO OUT IO is not bypassed. 1b / Bypass / Flop in the AUDIO OUT IO is bypassed.
	12:11	**Detect Frame sync early** These bits are used to pullin the frame sync detection logic earlier to compensate for PV issues if any. Audio codec starts driving the SDI pin earlier by the number of clocks programmed by this register.

AUD_FREQ_CNTRL

Value	Name	Description
00b	Pull in by 0 bclks	Frame sync is detected at bclk = 1998.
01b	Pull in by 1 bclks	Frame sync is detected at bclk = 1997.
10b	Pull in by 2 bclks **[Default]**	Frame sync is detected at bclk = 1996.
11b	Pull in by 3 bclks	Frame sync is detected at bclk = 1995.

10:5 Reserved

Access:	RO
Format:	MBZ

4 96MHz BCLK

Default Value:	1b

Indicates that iDISPLAY Audio Link will run at 96MHz. This bit is defaulted to 1. BIOS or System Software must pre-program B96 before the iDISPLAY Audio Link is brought out from reset.

3 48MHz BCLK

Default Value:	0b

Indicates that iDISPLAY Audio Link will run at 48MHz. This bit is defaulted to 0. BIOS or System Software must pre-program B96 before the iDISPLAY Audio Link is brought out from reset.

2:0 Reserved

Access:	RO
Format:	MBZ

AUD_INFOFR

AUD_INFOFR	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	65054h-65057h
Name:	Audio Widget Data Island Packet Transcoder A
ShortName:	AUD_TCA_INFOFR
Reset:	soft
Address:	65154h-65157h
Name:	Audio Widget Data Island Packet Transcoder B
ShortName:	AUD_TCB_INFOFR
Reset:	soft
Address:	65254h-65257h
Name:	Audio Widget Data Island Packet Transcoder C
ShortName:	AUD_TCC_INFOFR
Reset:	soft
Address:	65354h-65357h
Name:	Audio Widget Data Island Packet Transcoder D
ShortName:	AUD_TCD_INFOFR
Reset:	soft

When the IF type or dword index is not valid, the contents of the DIP will return all 0s.
These values are programmed by the audio driver in an HDMI/DP Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI/DP DIP response to a Get HDMI/DP Widget command. To fetch a specific byte, the audio driver should send an HDMI/DP Widget HDMI/DP DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI/DP DIP get.

DWord	Bit	Description
0	31:0	**Data Island Packet Data** This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_M_CTS_ENABLE

AUD_M_CTS_ENABLE

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65028h-6502Bh
Name:	Audio M and CTS Programming Enable Transcoder A
ShortName:	AUD_TCA_M_CTS_ENABLE
Reset:	soft
Address:	65128h-6512Bh
Name:	Audio M and CTS Programming Enable Transcoder B
ShortName:	AUD_TCB_M_CTS_ENABLE
Reset:	soft
Address:	65228h-6522Bh
Name:	Audio M and CTS Programming Enable Transcoder C
ShortName:	AUD_TCC_M_CTS_ENABLE
Reset:	soft
Address:	65328h-6532Bh
Name:	Audio M and CTS Programming Enable Transcoder D
ShortName:	AUD_TCD_M_CTS_ENABLE
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21	**CTS M value Index** 0b – CTS **[Default]** – CTS value read on bits 19:0 reflects CTS value. Bit 19:0 is programmable to any CTS value. default is 0 1b – M – M value read on bits 19:0 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 19:0 will reflect the current M value
	20	**Enable CTS or M prog** When set will enable CTS or M programming.

AUD_M_CTS_ENABLE		
	19:0	**CTS programming** These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field.

AUD_MISC_CTRL

AUD_MISC_CTRL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65010h-65013h
Name:	Audio Converter 1 Misc Control
ShortName:	AUD_C1_MISC_CTRL
Reset:	soft
Address:	65110h-65113h
Name:	Audio Converter 2 Misc Control
ShortName:	AUD_C2_MISC_CTRL
Reset:	soft
Address:	65210h-65213h
Name:	Audio Converter 3 Misc Control
ShortName:	AUD_C3_MISC_CTRL
Reset:	soft
Address:	65310h-65313h
Name:	Audio Converter 4 Misc Control
ShortName:	AUD_C4_MISC_CTRL
Reset:	soft

There is one instance of this register per audio converter 1/2/3.

DWord	Bit	Description
0	31:9	**Reserved** Access: RO Format: MBZ
	8	**Reserved**
	7:4	**Output Delay** Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
	3	**Reserved** Access: RO Format: MBZ
	2	**Sample Fabrication EN bit** Access: R/W This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

AUD_MISC_CTRL

Value	Name	Description
0b	Disable	Audio fabrication disabled
1b	Enable **[Default]**	Audio fabrication enabled

1 **Pro Allowed**

Access:	R/W

By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode. Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.

Value	Name	Description
0b	Consumer **[Default]**	Consumer use only
1b	Professional	Professional use allowed

0 **Reserved**

Access:	RO
Format:	MBZ

AUD_PIN_ELD_CP_VLD

AUD_PIN_ELD_CP_VLD

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	650C0h-650C3h
Name:	Audio Pin ELD and CP Ready Status
ShortName:	AUD_PIN_ELD_CP_VLD
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Audio InactiveD** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. 0b – Disable – Device is active for streaming audio data 1b – Enable – Device is connected but not active
	14	**Audio Output EnableD** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. 0b – Disable – No Audio output 1b – Valid – Audio is enabled
	13	**CP ReadyD** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based. Software should add a delay of 1ms before updating the CP ready bit. This is needed to make sure that all the pending unsolicited responses are cleared (transmitted to HD audio) before CP ready unsolicited responses is generated. This is needed in case of DP MST is enabled and when many changes to PD, ELDV and CP ready bits are done during mode set. 0b – Pending or Not Ready – CP request pending or not ready to receive requests. 1b – Ready – CP request ready

AUD_PIN_ELD_CP_VLD

12 **ELD validD**

This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

11 **Audio InactiveC**

Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

10 **Audio Output EnableC**

This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver.

Value	Name	Description
0b	Disable	No Audio output
1b	Valid	Audio is enabled

9 **CP ReadyC**

This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based. Software should add a delay of 1ms before updating the CP ready bit. This is needed to make sure that all the pending unsolicited responses are cleared (transmitted to HD audio) before CP ready unsolicited responses is generated. This is needed in case of DP MST is enabled and when many changes to PD, ELDV and CP ready bits are done during mode set.

Value	Name	Description
0b	Pending or Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

8 **ELD validC**

This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

AUD_PIN_ELD_CP_VLD

7	**Audio InactiveB** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

6	**Audio Output EnableB** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.

Value	Name	Description
0b	Disable	No audio output
1b	Enable	Audio is enabled

5	**CP ReadyB** See CP_ReadyC description.

Value	Name	Description
0b	Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

4	**ELD validB** See ELD_validC descripion.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

3	**Audio InactiveA** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

2	**Audio Output EnableA** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.

Value	Name	Description
0b	Disable	No audio output
1b	Enable	Audio is enabled

AUD_PIN_ELD_CP_VLD

	1	**CP ReadyA** See CP_ReadyC description. **Value** / **Name** / **Description** 0b / Not Ready / CP request pending or not ready to receive requests 1b / Ready / CP request ready
	0	**ELD validA** See ELD_validC descripion. **Value** / **Name** / **Description** 0b / Invalid / ELD data invalid (default, when writing ELD data, set 0 by software) 1b / Valid / ELD data valid (Set by video software only)

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	650A8h-650ABh
Name:	Audio Connection List Entry and Length Transcoder A
ShortName:	AUD_TCA_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft
Address:	651A8h-651ABh
Name:	Audio Connection List Entry and Length Transcoder B
ShortName:	AUD_TCB_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft
Address:	652A8h-652ABh
Name:	Audio Connection List Entry and Length Transcoder C
ShortName:	AUD_TCC_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft
Address:	653A8h-653ABh
Name:	Audio Connection List Entry and Length Transcoder D
ShortName:	AUD_TCD_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command if DP MST. There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**Connection List Entry** Connection to Convertor Widget Node 0x03
	7	**Long Form** This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
	6:0	**Connection List Length** Default Value: 0000001b This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

AUD_PIPE_CONN_SEL_CTRL

AUD_PIPE_CONN_SEL_CTRL	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	650ACh-650AFh
Name:	Audio Pipe Connection Select Control
ShortName:	AUD_PIN_PIPE_CONN_SEL_CTRL_RO
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command for DP MST.

DWord	Bit	Description
0	31:24	**Connection select Control PipeD** Default Value: 0Fh Connection Index Currently Set [Default 0x00], PipeD Widget is set to 0x03
	23:16	**Connection select Control PipeC** Default Value: 0Fh Connection Index Currently Set [Default 0x00], PipeC Widget is set to 0x02
	15:8	**Connection select Control PipeB** Default Value: 0Fh Connection Index Currently Set [Default 0x00], PipeB Widget is set to 0x01
	7:0	**Connection select Control PipeA** Default Value: 0Fh Connection Index Currently Set [Default 0x00], PipeA Widget is set to 0x00

AUD_PWRST

AUD_PWRST

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	6504Ch-6504Fh
Name:	Audio Power State Read Only
ShortName:	AUD_PWRST_RO
Reset:	soft

These values are returned from the device as the Power State response to a Get Audio Function Group command.

DWord	Bit	Description
0	31:30	**Converter4 Widget PwrSt Curr** Format: **Audio Power State Format** Converter4 Widget current power state Value: 11b — Name:
	29:28	**Converter4 Widget PwrSt Req** Format: **Audio Power State Format** Converter4 Widget power state that was requested by audio software Value: 11b — Name:
	27:26	**Func Grp Dev PwrSt Curr** Format: **Audio Power State Format** Function Group Device current power state Value: 11b — Name:
	25:24	**Func Grp Dev PwrSt Set** Format: **Audio Power State Format** Function Group Device power state that was set Value: 11b — Name:
	23:22	**Converter3 Widget PwrSt Curr** Format: **Audio Power State Format** Converter3 Widget current power state Value: 11b — Name:

AUD_PWRST

	21:20	**Converter3 Widget PwrSt Req** Format: **Audio Power State Format** Converter3 Widget power state that was requested by audio software **Value** / **Name** 11b
	19:18	**Convertor2 Widget PwrSt Curr** Format: **Audio Power State Format** Converor2 Widget current power state **Value** / **Name** 11b
	17:16	**Convertor2 Widget PwrSt Req** Format: **Audio Power State Format** Converter2 Widget power state that was requested by audio software **Value** / **Name** 11b
	15:14	**Convertor1 Widget PwrSt Curr** Format: **Audio Power State Format** Converter1 Widget current power state **Value** / **Name** 11b
	13:12	**Convertor1 Widget PwrSt Req** Format: **Audio Power State Format** Converter1 Widget power state that was requested by audio software **Value** / **Name** 11b
	11:10	**PinD Widget PwrSt Curr** Format: **Audio Power State Format** PinD Widget current power stateFor DP MST this represents Device3 power state **Value** / **Name** 11b
	9:8	**PinD Widget PwrSt Set** Format: **Audio Power State Format** PinD Widget power state that was setFor DP MST this represents Device3 power state **Value** / **Name** 11b
	7:6	**PinC Widget PwrSt Curr** Format: **Audio Power State Format** PinC Widget current power stateFor DP MST this represents Device2 power state

AUD_PWRST

		Value: 11b — Name:
	5:4	**PinC Widget PwrSt Set** Format: Audio Power State Format PinC Widget power state that was setFor DP MST this represents Device2 power state Value: 11b — Name:
	3:2	**PinB Widget PwrSt Curr** Format: Audio Power State Format PinB Widget current power stateFor DP MST this represents Device1 power state Value: 11b — Name:
	1:0	**PinB Widget PwrSt Set** Format: Audio Power State Format PinB Widget power state that was setFor DP MST this represents Device1 power state Value: 11b — Name:

AUD_RID

AUD_RID	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	65024h-65027h
Name:	Audio Revision ID Read Only
ShortName:	AUD_RID_RO
Reset:	soft

These values are returned from the device as the Revision ID response to a Get Root Node command.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:20	**Major Revision** Default Value: 1h The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	19:16	**Minor Revision** Default Value: 0h The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	15:8	**Revision ID** Default Value: 00h The vendor revision number for this given Device ID. This field is hardwired within the device.
	7:0	**Stepping ID** Default Value: 00h An optional vendor stepping number within the given Revision ID. This field is hardwired within the device.

AUD_VID_DID

AUD_VID_DID	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	65020h-65023h
Name:	Audio Vendor ID / Device ID Read Only
ShortName:	AUD_VID_DID_RO
Reset:	soft

These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.

DWord	Bit	Description
0	31:16	**Vendor ID** Default Value: 8086h Used to identify the codec within the PnP system. This field is hardwired within the device.
	15:8	**Device ID Upper byte** Default Value: 28h Constant used to identify the codec within the PnP system. This field is set by the device hardware.
	7:0	**Device ID Lower byte** Constant used to identify the codec within the PnP system. This field is set by fuse download. For correct values refer to the Codec root node parameter 00h.

AUD_WD_CNTRL

AUD_WD_CNTRL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6580Ch-6580Fh
Name:	Audio WD Control for slice 1
ShortName:	AUD_WD_CNTRL_1
Reset:	soft
Address:	6590Ch-6590Fh
Name:	Audio WD Control for slice 2
ShortName:	AUD_WD_CNTRL_2
Reset:	soft

There are two sets of these registers. One for each Wireless Audio Slice

DWord	Bit	Description
0	31	**Audio Inactive WD** Inactive: When this bit is set, wireless display device has been attached but not active for streaming audio. Value / Name / Description: 0b / Disable / Device is active for streaming audio data 1b / Enable / Device is connected but not active
	30	**Audio Output Enable WD** This bit directs audio to the Wireless Device. When enabled along with Inactive set to 0 and audio data is available, the audio data will be sent to the Wireless memory where WDBOX can read and send it to the Wireless NIC. Value / Name / Description: 0b / Disable / No Audio output 1b / Valid / Audio is enabled
	29	**CP Ready WD** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the display software to indicate that the CP request has been serviced. Value / Name / Description: 0b / Pending or Not Ready / CP request pending or not ready to receive requests 1b / Ready / CP request ready
	28	**ELD valid WD** This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is

AUD_WD_CNTRL

reflected in the audio pin complex widget as the ELD valid status bit.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

27:24 **Reserved**

Access:	RO
Format:	MBZ

23 **WiGig Widi Mode**

Access:	R/W

This field indicates Wigig or Widi Mode.

Value	Name	Description
0b	WidiMode **[Default]**	default mode is Widi mode. When bit 30 is set to 1 and this bit is set to 0 Widi is enabled
1b	WiGigMode	When bit 30 is set to 1 and this bit is set to 1 WiGig is enabled

22:20 **WiGig TFD Size**

Access:	R/W

This is TFD size. The total circular buffer should be a multiple of this number.

Value	Name	Description
000b	512B **[Default]**	default size of TFD is 512B
001b	1024B	TFD Size is 1024B
010b	2048B	TFD Size is 2048B
011b	4096B	TFD Size is 4096B
100b	8192B	TFD Size is 8192B
101b	Reserved	Reserved
110b	Reserved	Reserved
111b	Reserved	Reserved

19:11 **Reserved**

Access:	RO
Format:	MBZ

10:6 **ELD buffer size**

Default Value:	10101b
Access:	RO

This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

5:1 **ELD access address**

Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_WD_CNTRL		
	0	**ELD ACK** Acknowledgement from the audio driver that ELD read has been completed

AUD_WD_DMA_HDPTR

AUD_WD_DMA_HDPTR		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	65880h-65883h	
Name:	Audio WD Input DMA Head Pointer for slice 1	
ShortName:	AUD_WD_DMA_HDPTR_1	
Reset:	soft	
Address:	65980h-65983h	
Name:	Audio WD Input DMA Head Pointer for slice 2	
ShortName:	AUD_WD_DMA_HDPTR_2	
Reset:	soft	

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Aud WD HEAD PTR** Access: R/W This field provides write of the head pointer from WDBOX/WNIC. Comes in as message to Display Engine. Head Pointer always rolls over after it reaches the Audio WD Buffer size.

AUD_WD_DMA_TAILPTR

AUD_WD_DMA_TAILPTR	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	65890h-65893h
Name:	Audio WD Input DMA Tail Pointer for slice 1
ShortName:	AUD_WD_DMA_TAILPTR_1
Reset:	soft
Address:	65990h-65993h
Name:	Audio WD Input DMA Tail Pointer for slice 2
ShortName:	AUD_WD_DMA_TAILPTR_2
Reset:	soft

There are two sets of these registers. One for each wireless Audio slice.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Aud WD TAILPTR** Access: RO This field provides readback of the tail pointer sent to the WDBOX. Tail Pointer always rolls over after it reaches the Audio WD Buffer size.

AUD_WD_EDID_DATA

AUD_WD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65810h-65813h
Name:	Audio WD EDID Data for slice 1
ShortName:	AUD_WD_EDID_DATA_1
Reset:	soft
Address:	65910h-65913h
Name:	Audio WD EDID Data for slice 2
ShortName:	AUD_WD_EDID_DATA_2
Reset:	soft

THere are two sets of these registers. One for each Wireless Audio Slice.

This register contains the Wireless data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get Wireless Widget command. Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size has been reached.
- Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size has been reached.

DWord	Bit	Description
0	31:0	**EDID Data Block** This field specifies the EDID data block. Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during a device 2 FLR.

AUD_WNIC_2_AUD_RESET

AUD_WNIC_2_AUD_RESET	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6589Ch-6589Fh
Name:	WNIC to Audio RESET
ShortName:	AUD_WNIC_2_AUD_RESET_1
Reset:	soft
Address:	6599Ch-6599Fh
Name:	WNIC to Audio RESET
ShortName:	AUD_WNIC_2_AUD_RESET_2
Reset:	soft

There are two sets of these registers. One for each Audio wireless slice.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**WNIC to AUDIO Reset** When set, • HW shall reset the audio TFD head and tail pointers. • Audio immediately stops sending audio TFD tail pointer to WNIC. • HW shall drain and throw away any remaining audio WDE packets left in the pipeline. Audio packets continue to stream internally; however, none of these shall be put in the TFD. • When reset request is clear, WDBOX resumes transmission as soon as enough audio packets exist.

AUD_WNIC_PCR_LOWADDROFFSET

AUD_WNIC_PCR_LOWADDROFFSET	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	658A0h-658A3h
Name:	Audio WNIC PCR Low offset address for slice 1
ShortName:	AUD_WNIC_PCR_LOWADDROFFSET_1
Reset:	soft
Address:	659A0h-659A3h
Name:	Audio WNIC PCR Low offset address for slice 2
ShortName:	AUD_WNIC_PCR_LOWADDROFFSET_2
Reset:	soft
There are two sets of these registers. One for each Audio wireless slice.	

DWord	Bit	Description
0	31:0	**Aud WNIC PCR LOW ADDRESS OFFSET** This field provides low base address offset which will be used to sent the PCR updates to WNIC.

AUD_WNIC_PCR_UPADDROFFSET

AUD_WNIC_PCR_UPADDROFFSET	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	658A4h-658A7h
Name:	Audio WNIC PCR Upper offset address for slice 1
ShortName:	AUD_WNIC_PCR_UPADDROFFSET_1
Reset:	soft
Address:	659A4h-659A7h
Name:	Audio WNIC PCR Upper offset address for slice 2
ShortName:	AUD_WNIC_PCR_UPADDROFFSET_2
Reset:	soft
There are two sets of these registers. One for each Audio Wireless slice.	

DWord	Bit	Description
0	31:0	**Aud WNIC PCR UPPER ADDRESS OFFSET** This field provides upper base address offset which will be used to sent the PCR updates to WNIC. Only bits 7:0 should be programmed as total address space of 39:0 is available.

AUD_WNIC_TAILPTR_ADDROFFSET

AUD_WNIC_TAILPTR_ADDROFFSET	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65894h-65897h
Name:	Audio WNIC Tail Pointer offset address for slice 1
ShortName:	AUD_WNIC_TAILPTR_ADDROFFSET_1
Reset:	soft
Address:	65994h-65997h
Name:	Audio WNIC Tail Pointer offset address for slice 2
ShortName:	AUD_WNIC_TAILPTR_ADDROFFSET_2
Reset:	soft
There are two sets of these registers. One for each Audio Wireless slice.	

DWord	Bit	Description
0	31:0	**Aud WNIC TAIL PTR OFFSET** This field provides address offset which will be used to sent the tail point updates to WNIC.

AUD_WNIC_TAILPTR_UPADDROFFSET

AUD_WNIC_TAILPTR_UPADDROFFSET	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65898h-6589Bh
Name:	Audio WNIC Tail Pointer offset upper address for slice 1
ShortName:	AUD_WNIC_TAILPTR_UPADDROFFSET_1
Reset:	soft
Address:	65998h-6599Bh
Name:	Audio WNIC Tail Pointer offset upper address for slice 2
ShortName:	AUD_WNIC_TAILPTR_UPADDROFFSET_2
Reset:	soft
There are two sets of these registers. One for each Audio Wireless Slice.	

DWord	Bit	Description
0	31:0	**Aud WNIC TAIL PTR Upper address offset** This field provides upper address offset which will be used to sent the tail point updates to WNIC. Only bits 7:0 should be programmed as total address space of 39:0 is available.

AUDIO_PIN_BUF_CTL

AUDIO_PIN_BUF_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	48414h-48417h
Name:	Audio Pins Buffer Control
ShortName:	AUDIO_PIN_BUF_CTL
Reset:	soft

This register controls the display audio pins I/O buffers.

DWord	Bit	Description
0	31	**Enable** This field enables the audio buffer. Value: 0b = Disable; 1b = Enable
	30	**Reserved** Access: RO Format: MBZ
	29:28	**Hysteresis**
	27	**Reserved** Access: RO Format: MBZ
	26:24	**Spare**
	23:21	**Reserved** Access: RO Format: MBZ
	20:16	**Pulldown Strength**
	15:12	**Pulldown Slew**
	11:9	**Reserved** Access: RO Format: MBZ
	8:4	**Pullup Strength**
	3:0	**Pullup Slew**

Audio Codec Interrupt Definition

Audio Codec Interrupt Definition	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	44480h-4448Fh
Name:	Audio Codec Interrupts
ShortName:	AUD_INTERRUPT
Reset:	soft

This table indicates which events are mapped to each bit of the Audio Codec Interrupt registers.
0x44480 = ISR
0x44484 = IMR
0x44488 = IIR
0x4448C = IER

DWord	Bit	Description
0	31	**Audio_Power_State_change_Transcoder_D** The ISR is an active high pulse when there is a power state change for audio for DDI D.
	30	**Audio_Power_State_change_Transcoder_C** The ISR is an active high pulse when there is a power state change for audio for DDI C.
	29	**Audio_Power_State_change_Transcoder_B** The ISR is an active high pulse when there is a power state change for audio for DDI B.
	28	**Reserved**
	27	**Reserved**
	26	**Audio_Function_Group_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of function group widget.
	25	**Audio_Conv1_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 1 widget.
	24	**Audio_Conv2_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 2 widget.
	23	**Audio_Conv3_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 3 widget.
	22	**Audio_Conv4_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 4 widget.
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Reserved**
	17	**Reserved**
	16	**Reserved**

Audio Codec Interrupt Definition		
	15	**Reserved**
	14	**Reserved**
	13	**Reserved**
	12	**Spare 12**
	11	**Audio_Power_State_change_Transcoder_A** The ISR is an active high pulse when there is a power state change for audio for DDI F.
	10	**Reserved**
	9	**Reserved**
	8	**Reserved**
	7	**Reserved**
	6	**Reserved**
	5	**Reserved**
	4:3	**Unused_Int_4_3** These interrupts are currently unused.
	2	**Reserved**
	1	**Reserved**
	0	**Audio_Mailbox_Write** The ISR is an active high pulse when there is a write to any of the four Audio Mail box verbs in vendor defined node ID 8

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02420h-02423h
Name:	Auto Draw End Offset
ShortName:	3DPRIM_END_OFFSET_RCSUNIT_BE_GEOMETRY
Address:	18420h-18423h
Name:	Auto Draw End Offset
ShortName:	3DPRIM_END_OFFSET_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**End Offset** Format: U32 This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.

AVP av1 status

AVP_STATUS_ADDR - AVP av1 status	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1C2B04h-1C2B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG0
Address:	1C6B04h-1C6B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG1
Address:	1D2B04h-1D2B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG2
Address:	1D6B04h-1D6B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG3
Address:	1E2B04h-1E2B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG4
Address:	1E6B04h-1E6B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG5
Address:	1F2B04h-1F2B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG6
Address:	1F6B04h-1F6B07h
Name:	AVP av1 status
ShortName:	AVP_STATUS_ADDR_AWM_REG7

This register stores the number of clock cycles spent decoding/encoding the current frame.

DWord	Bit	Description
0	31	**AVP Pipe Active** Access: RO Indicate AVP Pipe is currently active in processing the frame/tile

AVP_STATUS_ADDR - AVP av1 status		
	30:2	**Reserved** Access: RO Format: MBZ
	1	**Final MV Overflow Error** Access: RO Format: U1 Indicate the final MV is overflowing
	0	**Bitstream Upper Bound Error** Access: RO Format: U1 Indicate the bitstream access has reached the upper bound of the buffer and overflow

AVP av1 unit done

AVP_UNIT_DONE_ADDR - AVP av1 unit done	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1C2B00h-1C2B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG0
Address:	1C6B00h-1C6B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG1
Address:	1D2B00h-1D2B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG2
Address:	1D6B00h-1D6B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG3
Address:	1E2B00h-1E2B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG4
Address:	1E6B00h-1E6B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG5
Address:	1F2B00h-1F2B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG6
Address:	1F6B00h-1F6B03h
Name:	AVP av1 unit done
ShortName:	AVP_UNIT_DONE_ADDR_AWM_REG7

This register stores all the done signals for AVP pipe.
"0" means unit is done and idle; "1" means unit is active.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ

AVP_UNIT_DONE_ADDR - AVP av1 unit done

	17	**APP Done Signal (Inverted)** Access: RO Format: U1
	16	**APR Done Signal (Inverted)** Access: RO Format: U1
	15	**AIT Done Signal (Inverted)** Access: RO Format: U1
	14	**AIQ Done Signal (Inverted)** Access: RO Format: U1
	13	**AMC Done Signal (Inverted)** Access: RO Format: U1
	12	**AED Done Signal (Inverted)** Access: RO Format: U1
	11	**AMX Done Signal (Inverted)** Access: RO Format: U1
	10	**ALF Done Signal (Inverted)** Access: RO Format: U1
	9	**ALN Done Signal (Inverted)** Access: RO Format: U1
	8:0	**Reserved** Access: RO Format: MBZ

Base of DMA Protected Range

BDPR - Base of DMA Protected Range

Register Space:	MMIO: 0/2/0
Size (in bits):	64
SOC_Consumer:	BIOS
Address:	108140h

This register indicates the Base of DMA Protected Range. It contains TSEGMB, lowered by the DPR size (if enabled).

DWord	Bit	Description
0..1	63:32	**BDPR_MSB** Default Value: 000h Access: RO _Custom_GTIReset: BUS 1MB aligned base of DMA Range.
	31:20	**BDPR_LSB** Default Value: 000h Access: RO _Custom_GTIReset: BUS 1MB aligned base of DMA Protected Memory Range.
	19:0	**Reserved** Access: RO Format: MBZ

Batch Address Difference Register

BB_ADDR_DIFF - Batch Address Difference Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02154h-02157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_RCSUNIT
Address:	18154h-18157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_POCSUNIT
Address:	22154h-22157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_BCSUNIT
Address:	1C0154h-1C0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT0
Address:	1C4154h-1C4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT1
Address:	1C8154h-1C8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT0
Address:	1D0154h-1D0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT2
Address:	1D4154h-1D4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT3
Address:	1D8154h-1D8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT1
Address:	1E0154h-1E0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT4

BB_ADDR_DIFF - Batch Address Difference Register

Address:	1E4154h-1E4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT5

Address:	1E8154h-1E8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT2

Address:	1F0154h-1F0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT6

Address:	1F4154h-1F4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT7

Address:	1F8154h-1F8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT3

Address:	1A154h-1A157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_CCSUNIT0

This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Address Difference** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1:0	**Reserved** Access: RO Format: MBZ

Batch Buffer Head Pointer Preemption Register

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02148h-0214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_RCSUNIT
Address:	18148h-1814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_POCSUNIT
Address:	22148h-2214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_BCSUNIT
Address:	1C0148h-1C014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT0
Address:	1C4148h-1C414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT1
Address:	1C8148h-1C814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT0
Address:	1D0148h-1D014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT2
Address:	1D4148h-1D414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT3
Address:	1D8148h-1D814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT1
Address:	1E0148h-1E014Bh

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT4

Address:	1E4148h-1E414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT5

Address:	1E8148h-1E814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT2

Address:	1F0148h-1F014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT6

Address:	1F4148h-1F414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT7

Address:	1F8148h-1F814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT3

Address:	1A148h-1A14Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_CCSUNIT0

This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the batch buffer on which preemption has occurred.
This register gets updated with the DWord-aligned graphics memory address of the command following the MI_BATCH_START corresponding to the second level batch buffer, when the preemption has occurred in the second level batch buffer.
This register value should be looked at only when the preemption has occurred in the batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer.
Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling.
This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH	RenderCS

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE commandin a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Access: RO Format: MBZ

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02140h-02143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_RCSUNIT
Address:	18140h-18143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_POCSUNIT
Address:	22140h-22143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_BCSUNIT
Address:	1C0140h-1C0143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT0
Address:	1C4140h-1C4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT1
Address:	1C8140h-1C8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT0
Address:	1D0140h-1D0143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT2
Address:	1D4140h-1D4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT3
Address:	1D8140h-1D8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT1
Address:	1E0140h-1E0143h
Name:	Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register

ShortName:	BB_ADDR_VCSUNIT4
Address:	1E4140h-1E4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT5
Address:	1E8140h-1E8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT2
Address:	1F0140h-1F0143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT6
Address:	1F4140h-1F4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT7
Address:	1F8140h-1F8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT3
Address:	1A140h-1A143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_CCSUNIT0

Description

This field specifies the DWord-aligned Graphics Memory Address of commands being fetched for the most recently initiated batch buffer. This register has valid values only when the Valid bit is set to0. Level of the batch buffer is indicated based on the Batch Buffer Stack Pointer value in BB_STATE register.

- Stack Pointer holding a value 0 indicates First Level batch buffer.
- Stack Pointer holding a value 1 indicates Second Level batch buffer.
- Stack Pointer holding a value 2 indicates Third Level batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of commands being fetched for the most recently initiated batch buffer. This register have valid values only when the Valid bit is set to0. Level of the batch buffer is indicated based on the Batch Buffer Stack Pointer value in BB_STATE register.

BB_ADDR - Batch Buffer Head Pointer Register

- Stack Pointer holding a value 0 indicates First Level batch buffer.
- Stack Pointer holding a value 1 indicates Second Level batch buffer.
- Stack Pointer holding a value 2 indicates Third Level batch buffer.

1 Reserved

Access:	RO
Format:	MBZ

0 Valid

Format:	U1

Value	Name	Description
0h	Invalid **[Default]**	Batch buffer Invalid
1h	Valid	Batch buffer Valid

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	021C0h-021C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_RCSUNIT
Address:	181C0h-181C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_POCSUNIT
Address:	221C0h-221C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_BCSUNIT
Address:	1C01C0h-1C01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT0
Address:	1C41C0h-1C41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT1
Address:	1C81C0h-1C81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT0
Address:	1D01C0h-1D01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT2
Address:	1D41C0h-1D41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT3
Address:	1D81C0h-1D81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT1
Address:	1E01C0h-1E01C3h
Name:	Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

ShortName:	BB_PER_CTX_PTR_VCSUNIT4
Address:	1E41C0h-1E41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT5
Address:	1E81C0h-1E81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT2
Address:	1F01C0h-1F01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT6
Address:	1F41C0h-1F41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT7
Address:	1F81C0h-1F81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT3
Address:	1A1C0h-1A1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_CCSUNIT0

This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.

Programming Notes

BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.

Render CS: Per Context Batch Buffer execution must not look at the MI_RS_CONTROL or Wait For Event status that are restored for the corresponding context. Ex: A context with MI_RS_CONTROL status with RS disabled doesn't stop Render CS from triggering Resource Streamer to execute Per Context Batch Buffer when "**RS Enabled Batch Buffer Per Context**" is set.

RenderCS: The following commands are not supported within a Per Context Batch Buffer:

Command Name
MI_WAIT_FOR_EVENT
MI_ARB_CHECK
MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC
MI_SUSPEND_FLUSH

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

MI_TOPOLOGY_FILTER
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT (Memory Poll Mode). Note: MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_SEMAPHORE_SIGNAL
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS
3DSTATE_BINDING_TABLE_POINTERS_HS
3DSTATE_BINDING_TABLE_POINTERS_DS
3DSTATE_BINDING_TABLE_POINTERS_GS
3DSTATE_BINDING_TABLE_POINTERS_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
PIPECONTROL

DWord	Bit	Description
0	31:12	**Batch Buffer Per Context Address** Format: U20 Pointer to the Context in memory to be executed as a batch.
	11:3	**Reserved** Access: RO Format: MBZ
	2	**FORCE BB_PER_CTX_PTR** On detecting a context restore (not lite restore) with head pointer equals to tail pointer, command stream optimizes context switch process by not doing engine context restore and context save for the corresponding context. As part of this optimization command stream doesn't execute batch buffer per context pointer (BB_PER_CTX_PTR). Setting this bit allows command stream to execute BB_PER_CTX_PT even on context restore flows with head pointer equals to tail pointer. **Value** / **Name** / **Description** 0 / **[Default]** / Command stream does not execute BB_PER_CTX_PTR on context restore with head pointer equals to tail pointer.

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

	1	Command stream does execute BB_PER_CTX_PTR on context restore with head pointer equals to tail pointer.

Reserved

Access:	RO
Format:	MBZ

Batch Buffer Per Context Valid

Format:	U1

If set, the command stream will execute the context from the **Batch Buffer Per Context Address** prior to the execution of actual submitted workloads.

Batch Buffer Stack Write Port

BB_STACK_WRITE_PORT - Batch Buffer Stack Write Port	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02588h-0258Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_RCSUNIT
Address:	18588h-1858Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_POCSUNIT
Address:	22588h-2258Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_BCSUNIT
Address:	1C0588h-1C058Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT0
Address:	1C4588h-1C458Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT1
Address:	1C8588h-1C858Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VECSUNIT0
Address:	1D0588h-1D058Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT2
Address:	1D4588h-1D458Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT3
Address:	1D8588h-1D858Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VECSUNIT1
Address:	1E0588h-1E058Bh
Name:	BB_STACK_WRITE_PORT

BB_STACK_WRITE_PORT - Batch Buffer Stack Write Port

ShortName:	BB_STACK_WRITE_PORT_VCSUNIT4
Address:	1E4588h-1E458Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT5
Address:	1E8588h-1E858Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VECSUNIT2
Address:	1F0588h-1F058Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT6
Address:	1F4588h-1F458Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VCSUNIT7
Address:	1F8588h-1F858Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_VECSUNIT3
Address:	1A588h-1A58Bh
Name:	BB_STACK_WRITE_PORT
ShortName:	BB_STACK_WRITE_PORT_CCSUNIT0

DWord	Bit	Description
0	31:0	**Batch Buffer Stack Pointer** Format: U32 This register provides a mechanism to update the entries of the Batch Buffer Stack in hardware. Consecutive writes to this register results in updating consecutive entries of the Batch Buffer Stack, starts fromEntry0(bottom of the stack) of the stack, reaches the last entry of the stack (top of the stack) and wraps around to Entry0. Note that each entry of the stack is a qword and two consecutive MMIO writes are required to update an entry of a stack. This register must not be written by SW and is only meant for hardware internal usage to context save/restore batch buffer stack values. BATCH_BUFFER_STACK_STRUCTURE defines the structure of the batch buffer stack implemented in hardware.

Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02150h-02153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_RCSUNIT
Address:	18150h-18153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_POCSUNIT
Address:	22150h-22153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_BCSUNIT
Address:	1C0150h-1C0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT0
Address:	1C4150h-1C4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT1
Address:	1C8150h-1C8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT0
Address:	1D0150h-1D0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT2
Address:	1D4150h-1D4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT3
Address:	1D8150h-1D8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT1
Address:	1E0150h-1E0153h
Name:	Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register

ShortName:	BB_START_ADDR_VCSUNIT4
Address:	1E4150h-1E4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT5
Address:	1E8150h-1E8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT2
Address:	1F0150h-1F0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT6
Address:	1F4150h-1F4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT7
Address:	1F8150h-1F8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT3
Address:	1A150h-1A153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_CCSUNIT0

This register contains the address specified in the last MI_BATCH_BUFFER_START command executed for the first level batch buffer or chained first level batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Start Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer starting address.
	1:0	**Reserved** Access: RO Format: MBZ

Batch Buffer Start Upper Head Pointer Register

BB_START_ADDR_UDW - Batch Buffer Start Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02170h-02173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_RCSUNIT
Address:	18170h-18173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_POCSUNIT
Address:	22170h-22173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_BCSUNIT
Address:	1C0170h-1C0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT0
Address:	1C4170h-1C4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT1
Address:	1C8170h-1C8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT0
Address:	1D0170h-1D0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT2
Address:	1D4170h-1D4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT3
Address:	1D8170h-1D8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT1
Address:	1E0170h-1E0173h

BB_START_ADDR_UDW - Batch Buffer Start Upper Head Pointer Register

Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT4

Address:	1E4170h-1E4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT5

Address:	1E8170h-1E8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT2

Address:	1F0170h-1F0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT6

Address:	1F4170h-1F4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT7

Address:	1F8170h-1F8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT3

Address:	1A170h-1A173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_CCSUNIT0

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24:16	**Reserved** Access: RO Format: MBZ
	15:0	**Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Batch Buffer State Register

BB_STATE - Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02110h-02113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_RCSUNIT
Address:	18110h-18113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_POCSUNIT
Address:	22110h-22113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_BCSUNIT
Address:	1C0110h-1C0113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT0
Address:	1C4110h-1C4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT1
Address:	1C8110h-1C8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT0
Address:	1D0110h-1D0113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT2
Address:	1D4110h-1D4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT3
Address:	1D8110h-1D8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT1
Address:	1E0110h-1E0113h
Name:	Batch Buffer State Register

BB_STATE - Batch Buffer State Register

ShortName:	BB_STATE_VCSUNIT4
Address:	1E4110h-1E4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT5
Address:	1E8110h-1E8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT2
Address:	1F0110h-1F0113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT6
Address:	1F4110h-1F4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT7
Address:	1F8110h-1F8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT3
Address:	1A110h-1A113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_CCSUNIT0

Description

This register specifies the state of the most recently executed batch buffer. Contents of this register are only valid when Valid bit in BB_ADDR register is set.
Level of the batch buffer is indicated by the Batch Buffer Stack Pointer value in BB_STATE register.
Stack Pointer holding a value 0 indicates First Level batch buffer.
Stack Pointer holding a value 1 indicates Second Level batch buffer.
Stack Pointer holding a value 2 indicates Third Level batch buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

Programming Notes

Contents of this register are valid only when "Valid" bit in BB_ADDR register is set.

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Format: MBZ

BB_STATE - Batch Buffer State Register

9 — POSH Start

Exists If:	//RCS, POCS

This bit reflects the POSH Start value programmed by the active first level MI_BATCH_BUFFER_START command.

8 — POSH Enable

Exists If:	//RCS, POCS

This bit reflects the POSH Enable value programmed by the active first level MI_BATCH_BUFFER_START command.

7 — Reserved

Access:	RO
Format:	MBZ

6 — Clear Command Buffer Enable

Source:	RenderCS
Format:	U1

5 — Address Space Indicator

Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	GGTT **[Default]**	This Batch buffer is located in GGTT memory and is privileged
1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.

4 — Reserved

3:2 — Reserved

Access:	RO
Format:	MBZ

1:0 — Batch Buffer Stack Pointer

Format:	U2

This field holds the index of the stack entry which got recently updated on executing a next level batch buffer (stack push). This index points to the entry on top of the stack. Stack pointer having a value of '00b indicates stack empty and a value of '11b indicates stack full.

Value	Name	Description
0h		Stack has no data and is empty.
1h		Stack has one valid entry and have first level batch buffer details.
2h		Stack has two valid entries and have first and second level batch buffer details.
3h		Stack has three valid entries and have first, second and third level batch buffer details.

Batch Buffer Upper Head Pointer Preemption Register

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0216Ch-0216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_RCSUNIT
Address:	1816Ch-1816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_POCSUNIT
Address:	2216Ch-2216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_BCSUNIT
Address:	1C016Ch-1C016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT0
Address:	1C416Ch-1C416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT1
Address:	1C816Ch-1C816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT0
Address:	1D016Ch-1D016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT2
Address:	1D416Ch-1D416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT3
Address:	1D816Ch-1D816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT1
Address:	1E016Ch-1E016Fh

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register

Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT4
Address:	1E416Ch-1E416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT5
Address:	1E816Ch-1E816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT2
Address:	1F016Ch-1F016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT6
Address:	1F416Ch-1F416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT7
Address:	1F816Ch-1F816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT3
Address:	1A16Ch-1A16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_CCSUNIT0

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer. This register follows the same rules as the BB_PREEMPT_ADDR register.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer.

Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02168h-0216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_RCSUNIT
Address:	18168h-1816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_POCSUNIT
Address:	22168h-2216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_BCSUNIT
Address:	1C0168h-1C016Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT0
Address:	1C4168h-1C416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT1
Address:	1C8168h-1C816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT0
Address:	1D0168h-1D016Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT2
Address:	1D4168h-1D416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT3
Address:	1D8168h-1D816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT1
Address:	1E0168h-1E016Bh
Name:	Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register

ShortName:	BB_ADDR_UDW_VCSUNIT4
Address:	1E4168h-1E416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT5
Address:	1E8168h-1E816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT2
Address:	1F0168h-1F016Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT6
Address:	1F4168h-1F416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT7
Address:	1F8168h-1F816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT3
Address:	1A168h-1A16Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_CCSUNIT0

Description

This register specifies the upper 32 bits of the 4GB aligned base address, within the 64-bit host virtual address space of the commands being fetched from the most recently initiated batch buffer. This register have valid values only when the Valid bit in BB_ADDR register is set to1. Level of the batch buffer is indicated based on the Batch Buffer Stack Pointer value in BB_STATE register. GraphicsAddress is 64-bit value [63:0], but only a portion of it is used by hardware. The uppermost reserved bits are ignored and MBZ.
Stack Pointer holding a value 0 indicates First Level batch buffer.
Stack Pointer holding a value 1 indicates Second Level batch buffer.
Stack Pointer holding a value 2 indicates Third Level batch buffer.

Programming Notes

This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24:16	**Reserved** Access: RO Format: MBZ

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register		
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Batch Offset Register

BB_OFFSET - Batch Offset Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02158h-0215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_RCSUNIT
Address:	18158h-1815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_POCSUNIT
Address:	22158h-2215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_BCSUNIT
Address:	1C0158h-1C015Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT0
Address:	1C4158h-1C415Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT1
Address:	1C8158h-1C815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT0
Address:	1D0158h-1D015Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT2
Address:	1D4158h-1D415Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT3
Address:	1D8158h-1D815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT1
Address:	1E0158h-1E015Bh
Name:	Batch Offset Register

BB_OFFSET - Batch Offset Register

ShortName:	BB_OFFSET_VCSUNIT4
Address:	1E4158h-1E415Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT5
Address:	1E8158h-1E815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT2
Address:	1F0158h-1F015Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT6
Address:	1F4158h-1F415Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT7
Address:	1F8158h-1F815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT3
Address:	1A158h-1A15Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_CCSUNIT0

This register contains the offset value to be added to the Batch Buffer Start Address in the MI_BATCH_BUFFER_START command when the Enable Offset bit in MI_BATCH_BUFFER_START command is set.

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

On preemption occurring within a primary/chain batch buffer this register is loaded with the offset value of the preempted command header from the batch start address when the Enable Load is set. Preemption of 3D or

BB_OFFSET - Batch Offset Register

GP_GPU workloads can only occur on preemptable commands. Batch buffer offset always points to the preemptable command if preempted on preemption or the immediate command following it if not preempted on preemption. EX: Preemption occurs on 3D_PRIMITVE command

- If the 3D_PRIMTIVE command is completely processed by render pipe then the BB_OFFSET points to the command following 3D_PRIMITIVE
- If the 3D_PRIMTIVE command is not completely processed by render pipe then the BB_OFFSET points to the 3D_PRIMITIVE command.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned offset between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1	**Reserved** Access: RO Format: MBZ
	0	**Enable Load** Default Value: 1 Format: Enable If this bit is set then the Batch Buffer Offset is loaded with the preempted command offset or the following command whenever a batch buffer is ended due to a Preemptable command.

BCS Context Sizes

BCS_CXT_SIZE - BCS Context Sizes			
Register Space:	MMIO: 0/2/0		
Access:	Read/32 bit Write Only		
Size (in bits):	32		
Address:	221A8h		
DWord	**Bit**	**Description**	
0	31:13	**Reserved**	
		Access:	RO
		Format:	MBZ
	12:8	**BCS Context Size**	
		Format:	U5
	7:5	**Reserved**	
		Access:	RO
		Format:	MBZ
	4:0	**Execlist Context Size**	
		Format:	U5

BCS CSB

BCS_CSB - BCS CSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SW reads this offset to read the Context Status Buffer entry at the top of the CSB FIFO. Reads must occur in pairs to obtain a single 64 bit CSB entry. The second read of a pair pops the CSB entry off the CSB fifo.		
DWord	**Bit**	**Description**
0	31:0	**Context Status Buffer DW** Access: RO This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.

BCS CSB Fifo Status Register

BCS_CSB_FSR - BCS CSB Fifo Status Register

Register Space: MMIO: 0/2/0

Size (in bits): 32

This RO register holds status of the CSB fifo.

DWord	Bit	Description
0	31	**Not Empty** Access: RO
	30:16	**Reserved** Access: RO Format: MBZ
	15:8	**FIFO Maximum Occupancy Count** This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.
	7:0	**FIFO Occupancy Count** Access: RO This is a second bit field in a register template

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	22198h-2219Fh

This register contains the *next* ring context ID associated with the ring buffer.

Programming Notes

The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).

DWord	Bit	Description
0	63:0	**Unnamed** See Context Descriptor for BCS

BCS SW Control

BCS_SWCTRL - BCS SW Control

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	22200h

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: BUS
	15:4	**Reserved** Access: RO Format: MBZ
	3	**Shrink Blitter Cache** Format: U1 _Custom_GTIReset: BUS This bit is primarily used for validation purposes to speed up the test time. The full cache depth of 128 CLs should be used for production. This bit is part of the context save/restore. This bit only applies to the XY_FAST_COPY_BLT command. **Value** / **Name** / **Description** 0 / **[Default]** / Blitter/BCS flush will flush and invalidate all cachelines in the Blitter/BLB cache (default). 1 / / Blitter Cache depth will be shortened from 128 CLs to 16 CLs.
	2	**Not Invalidate Blitter Cache on BCS Flush** Format: U1 _Custom_GTIReset: BUS Programming this bit allows optimal/maximal cache hit usage, when the destination surface of a Fast Copy Blit, is to be used as the Source for a follow on Fast Copy blit, even if the destination surface is flushed out for Display coherency reasons (where the destination surface is also needed to be Displayed). Such a flush with clean cacheline state is suggested when the intermediate blit operation results are being required to maintain memory coherency. The legacy method of cache invalidation on flush can be still pursued at the end of all blit operations or when switching happens due to other prescribed legacy reasons, or when switching from the new Fast Copy Engine blit, to legacy Engine blits. This bit should be programmed set only when used with Fast Copy Blit commands. This bit is part of the context save/restore. This bit only applies to the XY_FAST_COPY_BLT command.

BCS_SWCTRL - BCS SW Control

Value	Name	Description
0	**[Default]**	Blitter/BLB Cache will be 128 cache lines in depth (default).
1		BCS flush will put all dirty CL in the Blitter cache in the clean state. Any CL already in the clean state will remain clean.

1 **Tile Y Destination**

Description
Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore. This bit does not impact the operations of the XY_FAST_COPY_BLT command.

0 **Tile Y Source**

Description
Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore. This bit does not impact the operations of the XY_FAST_COPY_BLT command.

BIOS2DRIVER Scratch0

B2D_SCRATCH0 - BIOS2DRIVER Scratch0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	102000h

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31	**Display HD Audio Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	30	**Spare_16** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	29	**Spare_15** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	28	**Spare_14** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	27	**Spare_13** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	26	**Spare_12** Default Value: 0b Access: R/W _Custom_GTIReset: BUS

B2D_SCRATCH0 - BIOS2DRIVER Scratch0

	25	**ECC Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	24	**Force DRAM ECC Enabled** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	23	**Spare_11** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	22	**Spare_10** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	21	**Spare_9** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	20:19	**DDR Size** Default Value: 00b Access: R/W _Custom_GTIReset: BUS
	18	**Bclk overclocking disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	17	**Disable 1N Mode** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	16	**Spare_8** Default Value: 0b Access: R/W _Custom_GTIReset: BUS

B2D_SCRATCH0 - BIOS2DRIVER Scratch0

	15	**Spare_7** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	14	**2 DIMMS per Channel Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	13	**Spare_6** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	12	**Performance Dual Channel Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	11	**Spare_5** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	10	**Spare_4** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	9:8	**Spare_3** Default Value: 00b Access: R/W _Custom_GTIReset: BUS
	7:4	**Spare_2** Default Value: 0000b Access: R/W _Custom_GTIReset: BUS
	3	**DDR Overclocking** Default Value: 0b Access: R/W _Custom_GTIReset: BUS

B2D_SCRATCH0 - BIOS2DRIVER Scratch0		
	2	**IA Overclocking Enabled b** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	1	**Spare_1** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	0	**DDR3L Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS

BIOS2DRIVER Scratch1

B2D_SCRATCH1 - BIOS2DRIVER Scratch1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	102004h

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description	
0	31	**Spare_14**	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
	30	**IA Overclocking DSKU Control Disable**	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
	29	**IA Overclocking Enable**	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
	28	**Spare_13**	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
	27:25	**Cache Size Capability**	
		Default Value:	000b
		Access:	R/W
		_Custom_GTIReset:	BUS
	24	**Spare_12**	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS

B2D_SCRATCH1 - BIOS2DRIVER Scratch1

	23:21	**DDR3 Maximum Frequency Capability with 100 Memory** Default Value: 000b Access: R/W _Custom_GTIReset: BUS
	20	**Spare_11** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	19	**Spare_10** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	18	**Spare_9** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	17	**Spare_8** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	16	**Spare_7** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	15:12	**Spare_6** Default Value: 0000b Access: R/W _Custom_GTIReset: BUS
	11	**Reserved**
	10:8	**Spare_5** Default Value: 000b Access: R/W _Custom_GTIReset: BUS

B2D_SCRATCH1 - BIOS2DRIVER Scratch1

	7	**Spare_4** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	6:4	**DDR3 Maximum Frequency Capability** Default Value: 000b Access: R/W _Custom_GTIReset: BUS
	3	**Spare_3** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	2	**DDR4 DSKU Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	1	**Spare_2** Default Value: 0b Access: R/W _Custom_GTIReset: BUS
	0	**Spare_1** Default Value: 0b Access: R/W _Custom_GTIReset: BUS

BIOS2DRIVER Scratch2

B2D_SCRATCH2 - BIOS2DRIVER Scratch2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	102008h

Programming Notes

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31:0	**Spare** _Custom_GTIReset: BUS Reserved.

BIOS2DRIVER Scratch3

B2D_SCRATCH3 - BIOS2DRIVER Scratch3

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	10200Ch

Programming Notes

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31:0	**Spare** _Custom_GTIReset: BUS Reserved.

BIOS2DRIVER Scratch4

B2D_SCRATCH4 - BIOS2DRIVER Scratch4

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	102010h

Programming Notes

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31:0	**Spare** _Custom_GTIReset: BUS Reserved.

BIOS2DRIVER Scratch5

B2D_SCRATCH5 - BIOS2DRIVER Scratch5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	102014h

Programming Notes

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31:0	**Spare** _Custom_GTIReset: BUS Reserved.

BIOS2DRIVER Scratch6

B2D_SCRATCH6 - BIOS2DRIVER Scratch6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	102018h

Programming Notes

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31:0	**Spare** _Custom_GTIReset: BUS Reserved.

BIOS2DRIVER Scratch7

B2D_SCRATCH7 - BIOS2DRIVER Scratch7

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	10201Ch

Programming Notes

This register is used by Software and for software purposes only. Preliminary definition. The bit definitions may change later as the driver team has better clarity on what information is required and how best to format. Any updates will have no effect on the hardware.

DWord	Bit	Description
0	31:0	**Spare** _Custom_GTIReset: BUS Reserved.

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	128D4h
Name:	SE Output Bit Count
ShortName:	SE_Output_Bit_Count

This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Bit Count** Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128D0h	
This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	31:0	**MFC Bitstream Byte Count** Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12814h
Name:	Minimal Size Padding
ShortName:	Minimal_Size_Padding

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC AVC MinSize Padding Count** Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

BLC_PWM_CTL

BLC_PWM_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	48250h-48253h
Name:	Backlight PWM Control
ShortName:	BLC_PWM_CTL
Reset:	soft

This register controls the backlight PWM logic going to the display utility pin on the CPU.

DWord	Bit	Description
0	31	**PWM Enable** This bit enables the PWM logic.

Value	Name	Description
0b	Disable	PWM disabled
1b	Enable	PWM enabled

Restriction
The display utility pin must be configured correctly to output the PWM. Program the frequency and duty cycle before enabling PWM.

DWord	Bit	Description
	30:29	**Pipe Select** This field selects which vertical blank will be used for backlight blinking.

Value	Name	Description
00b	Pipe A	Use Pipe A
01b	Pipe B	Use Pipe B
10b	Pipe C	Use Pipe C
11b	Pipe D	

DWord	Bit	Description
	28	**Blinking Enable** This bit enables backlight blinking. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active.

Value	Name
0b	Disable
1b	Enable

BLC_PWM_CTL

	27	**PWM Granularity** This field controls the granularity (minimum increment) of the PWM backlight control counter. **Value** / **Name** / **Description** 0b / 128 / PWM frequency adjustment on 128 clock increments 1b / 8 / PWM frequency adjustment on 8 clock increments
	26:0	**Reserved** Access: RO Format: MBZ

BLC_PWM_DATA

BLC_PWM_DATA		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	48254h-48257h	
Name:	Backlight PWM Data	
ShortName:	BLC_PWM_DATA	
Reset:	soft	

DWord	Bit	Description
0	31:16	**Backlight Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is programmed based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity).
	15:0	**Backlight Duty Cycle** This field determines the number of time base events for the active portion of the PWM backlight control. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. Updates will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in CD clock periods multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity). **Restriction** This should never be larger than the frequency field.

Blitter Cache Control Register

BLIT_CCTL - Blitter Cache Control Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	22204h

DWord	Bit	Description
0	31:23	**Reserved** Access: RO Format: MBZ
	22:16	**Pattern MOCS** Format: MEMORY_OBJECT_CONTROL_STATE MOCS for blitter pattern operands.
	15	**Pattern MOCS Select** This bit is used to select what MOCS bits (pattern or source) are driven on the shared pattern/source MOCS bus. Value 0b: **[Default]** Drive source MOCS bits on the shared MOCS bus. Value 1b: Drive pattern MOCS bits on the shared MOCS bus.
	14:8	**Destination MOCS** Format: MEMORY_OBJECT_CONTROL_STATE MOCS for blitter destination operands.
	7	**Reserved** Access: RO Format: MBZ
	6:0	**Source MOCS** Format: MEMORY_OBJECT_CONTROL_STATE MOCS for blitter source operands.

Boot Hash Check Status

BOOT_HASH_CHK - Boot Hash Check Status

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Programming Notes

This register is saved in the power context

DWord	Bit	Description
0	31	**Valid uKernel Loaded** Whether there is a valid uKernel loaded into the SRAM. During boot this bit is set when the ukernel is moved from graphics memory to WOPCM & SRAM. During RC6 resume this bit is set when the uKernel is moved from WOPCM to SRAM. On initial Boot: BootROM code shall check this bit during the process of bringing up MinuteIA to determine when the uKernel is in-place in the SRAM before transferring control to it. On RC6 exit: If C068[4] is 0 (Early Jump): Bootrom code does not poll on C010[31] before jumping to ukernel in SRAM. Any reads/writes to SRAM area not yet restored by DMA are stalled based on "CL data present" bit for that cacheline. If C068[4] is 1 (Skip Early Jump): C010[31] is used same as in initial boot case.
	30:9	**Reserved** Access: RO Format: MBZ
	8	**Reserved**
	7:3	**Reserved** Access: RO Format: MBZ
	2	**Reserved**
	1	**Reserved**
	0	**uKernel Hash Ready** Indicates HW has completed SHA computation and loaded the value into the uKernel hash register

BOOT VECTOR

BOOTMSG - BOOT VECTOR

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	08504h

Boot Message Register
This register gets locked by the Hardware once written and is cleared only during the reset. This is extra protection given against Illegal Programming.

DWord	Bit	Description
0	31:0	**Boot Vector Message** Access: R/W Lock _Custom_GTIReset: BUS Boot vector is pass through. MBC gets the boot message from GPMunit and forwards it to MSQC. Breakdown of message is done in MSQC. Details: if b[26] = 1 C6SliceA = b[20:17]; C6SliceB= d[13:10] C6Way = 0 C6Area = 0 if b[26] = 0 C6Way = b[25:21], C6Slice = d[20:17]; C6Area = d[17:10] Context Restore = b[7] Reset Type = b[6:5] Ring Stop ID = b[4:0]

Built In Self Test

BIST_0_2_0_PCI - Built In Self Test		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0000Fh	
This register is used for control and status of Built In Self Test (BIST).		
DWord	**Bit**	**Description**
0	7	**BIST Supported** Default Value: 0b Access: RO _Custom_GTIReset: BUS BIST is not supported. This bit is hardwired to 0.
	6:0	**Reserved** Access: RO Format: MBZ

BW_BUDDY_CTL

BW_BUDDY_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	45140h-45143h
Name:	Bandwidth Buddy1 Control
ShortName:	BW_BUDDY1_CTL
Reset:	soft

Address:	45150h-45153h
Name:	Bandwidth Buddy2 Control
ShortName:	BW_BUDDY2_CTL
Reset:	soft

DWord	Bit	Description
0	31	**BW Buddy Disable** Access: R/W This field indicates if the address buddy logic is disabled. 0b: Enabled **[Default]** 1b: Disabled
	30	**Reserved**
	29	**Reserved** Access: RO Format: MBZ
	28:23	**Plane Request Timer** Access: R/W This is the timer to pick when a tracker gets allocated by a regular HP plane Request and starts to wait for its buddy (based on the mask) to come in. 010000b: 16 **[Default]** [1,63]
	22	**Reserved** Access: RO Format: MBZ

BW_BUDDY_CTL

	21:16	**TLB Request Timer** Access: R/W This is the timer to pick when a tracker gets allocated by a TLB Request and starts to wait for its buddy (based on the mask) to come in. Value: 0010000b — Name: 8 **[Default]** Value: [1,63] — Name:
	15	**Reserved**
	14:0	**Reserved** Access: RO Format: MBZ

BW_BUDDY_PAGE_MASK

BW_BUDDY_PAGE_MASK			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	45144h-45147h		
Name:	Bandwidth Buddy1 Page Mask		
ShortName:	BW_BUDDY1_PAGE_MASK		
Reset:	soft		
Address:	45154h-45157h		
Name:	Bandwidth Buddy2 Page Mask		
ShortName:	BW_BUDDY2_PAGE_MASK		
Reset:	soft		
DWord	**Bit**	**Description**	
0	31:28	**Reserved**	
		Access:	RO
		Format:	MBZ
	27:0	**BW Buddy Page Mask**	
		Default Value:	0000000h All address bits are not Masked
		Access:	R/W
		When set, bits in this register will cause Address bits to be excluded from the buddy address comparison. Mask bit[0] is associated with address bit[9], mask bit[1] is associated with address bit[10] and so on. For example, if bit [0] of the mask register is set, then address bit[9] is not used in the buddy address comparison. The default is to compare all address bits.	
		Programming Notes	
		Optimal programming will depend on the memory configuration used. See **Arbiter** page for details.	

C6 Entry latency

C6_ENTRY_LATENCY - C6 Entry latency

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 00D80h
Name: C6 Entry latency
ShortName: C6_ENTRY_LATENCY
_Custom_GTIContextMappedUnit: mgsr

The C6 Entry Latency written by GPMunit

DWord	Bit	Description
0	31:0	**Count for C6 entry Latency** Access: R/W _Custom_GTIReset: BUS C6 Entry Latency written by GPM Measure latency of C6 entry in terms usec pulses

Cache Line Size

CLS_0_2_0_PCI - Cache Line Size		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0000Ch	
DWord	**Bit**	**Description**
0	7:0	**Cache Line Size Value** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	07000h
Name:	Cache Mode Register 0
ShortName:	CACHE_MODE_0

This register is used to control the operation of the Render and Sampler L2 Caches. All reserved bits are implemented as read/write.
Before changing the value of this register, GFX pipeline must be idle i.e. full flush is required.
This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: DEV A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	14:12	**MSAA Compression Plane Number Threshold for eLLC** Access: R/W _Custom_GTIReset: DEV

Value	Name	Description
0h	threshold0 **[Default]**	Cache only planeID = 0 in eLLC.
1h	threshold1	Cache only planeID = 0, 1 in eLLC.
2h	threshold2	Cache only planeID = 0..2 in eLLC.
3h	threshold3	Cache only planeID = 0..3 in eLLC.
4h	threshold4	Cache only planeID = 0..4 in eLLC.
5h	threshold5	Cache only planeID = 0..5 in eLLC.
6h	threshold6	Cache only planeID = 0..6 in eLLC.
7h	threshold7	Cache only planeID = 0..7 in eLLC.

CACHE_MODE_0 - Cache Mode Register 0

Programming Notes
This bit-field is programmed based on MSAA. When MSAA compression is enabled, these settingsaffect HW, else it is ignored. For 16X MSAA only lower 8 planes can be cached in eLLC.

11 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

10 RCZ PMA Not-Promoted Allocation stall optimization Disable due to change in depth parameters

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Setting this bit will force the RCZ cache to stall at the allocation of a CL if any of the values in {Depth-mode, DTE, DWE, DTF} are different between the old and new requests to the same CL. The default is a smart stall depending on the New requests depth-test and depth write fields.

Value	Name	Description
0h	**[Default]**	Optimization is enabled
1h		Optimization is disabled

9 Sampler L2 TLB Prefetch Enable

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	TLB Prefetch Disabled
1h		TLB Prefetch Enabled

8 Reserved

7 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

6:5 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

CACHE_MODE_0 - Cache Mode Register 0

4 — RCC Eviction Policy

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e.(when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

3 — Reserved

2 — Hierarchical Z RAW Stall Optimization Disable

Access:	R/W

Description
The Hierarchical Z RAW Stall Optimization allows non-overlapping polygons in the same 8x4 pixel/sample area to be processed without stalling waiting for the earlier ones to write to Hierarchical Z buffer.

Value	Name	Description
0h	Enable **[Default]**	Enables the hierarchical Z RAW Stall Optimization.
1h	Disable	Disables the hierarchical Z RAW Stall Optimization.

Programming Notes
This bit must be set to 0 to enable the Hierarchical Z RAW stall optimization.

1 — Disable clock gating in the pixel backend

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1,the instruction/state caches must be invalidated. [DevGT:{WKA}]

0 — Disable Byte sharing for 3D TYF LOD1 surfaces for 32/64/128 bpp

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
1		Enable byte sharing for 3D TYF LOD1 surfaces - 32/64/128 bpp
0	**[Default]**	Disable Byte Sharing for 3D TYF surfaces LOD1 , 32/64/128 bpp

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Reset:	DEV
Address:	07004h
Name:	Cache Mode Register 1
ShortName:	CACHE_MODE_1

RegisterType: MMIO_SVL

Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Mask: MASK Format: Mask _Custom_GTIReset: DEV Must be set to modify corresponding data bit. Reads to this field returns zero.
	15	**Color Compression Disable** Access: R/W _Custom_GTIReset: DEV Setting this bit causes Lossless Render Target Color Compression to be disabled in Classic Clear (1x) Mode of Operation. Default value, i.e. resetting this bit, Enables Color Compression in Classic Clear Mode (1x) when CCS is Enabled.

Value	Name	Description
0h	**[Default]**	Enables Color Compression in Classic Clear Mode (1x) when CCS is Enabled.
1h		Causes Lossless Render Target Color Compression to be disabled in Classic Clear (1x) Mode of Operation

Programming Notes

The Below programming forces Color Compression to be disabled for MSAA modes explicitly as a HW WA. When switching from 1x ==> MSAA. Program this bit to 1 When switching from MSAA ==> 1x. Program this bit to 0

CACHE_MODE_1 - Cache Mode Register 1

14 Render Target 64B Read Disabled by RCC

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Setting this bit causes RCC to disable 64B reads and switch to legacy 128B Reads per RCC CL

Value	Name
1h	
0h	**[Default]**

13 NP EARLY Z FAILS DISABLE

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	IZ does conservatively fail any NP/R pixels.
1h		Disables IZ to conservatively fail pixels.

12 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

11 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

10 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

9 MSC RAW Hazard Avoidance Bit

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

When this field is set, MSC will enable RAW Hazard prevention mechanism, when lossless compression is enabled.

Value	Name	Programming Notes
0h	**[Default]**	
1h		This field should be programmed to 1 only if need arise to avoid RAW hazard when lossless compression is enabled

CACHE_MODE_1 - Cache Mode Register 1

8 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

7 Reserved

_Custom_GTIReset:	DEV

6 Shader Independent Evaluate Enable

When this bit is enabled, any shader stage can send evaluate messages. Hardware ignores AMFS state programming.

Value	Name	Description
0	Shader Independent Evaluate Disabled **[Default]**	Only Pixel Shaders can do evaluate
1		ALl shader stages can do evaluate

5 MCS Cache Disable

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

For Programming restrictions please refer to the 3D Pipeline.

Value	Name	Description
0h	**[Default]**	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.

4 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

3 RCZ PMA Promoted 2 Not-Promoted Allocation stall optimization Disable

Access:	R/W
_Custom_GTIReset:	DEV

Setting this bit will force the RCZ cache to stall at the allocation of a CL until the old Promoted writes retire in the RCZ$. Default mode is to stall at the IZ-read point until promoted writes are complete.

Value	Name	Description
0h	**[Default]**	Optimization is enabled
1h		Optimization is disabled

CACHE_MODE_1 - Cache Mode Register 1

2 **AMFS Disable Overshading**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0	**[Default]**
1	

Programming Notes
SW must set this bit to disable Overshading in AMFS control cache If this bit is set to 1, every eval message is allocated in the Control Cache. If this bit to set to 0, eval messages bypass control cache and all texels in the cacheline are shaded

1 **YCoCg DIsable**

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	YCoCg will be enabled by Defualt
1h		Setting this bit to 1 will disable YCoCg Compression and only compress using legacy RGB color space

0 **Disable Lossless Compression of partial Evictions on Previous Uncompressed Cache line**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	Lossless Compression of partial Evictions on Previous Uncompressed Cache line is Enabled
1h		Lossless Compression of partial Evictions on Previous Uncompressed Cache line is Disabled

Cache Mode Subslice Register

CACHE_MODE_SS - Cache Mode Subslice Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E420h

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:13	**Reserved** Access: RO Format: MBZ
	12	**Reserved** Access: RO Format: MBZ
	11	**Reserved** Format: PBC
	10:5	**Reserved** Access: RO Format: MBZ
	4	**Reserved** Format: PBC
	3:2	**Reserved** Access: RO Format: MBZ
	1	**Instruction Level 1 Cache and In-Flight Queue Disable** Format: Disable Value / Name / Description: 0h / **[Default]** / Cache is enabled. 1h / / Reserved

CACHE_MODE_SS - Cache Mode Subslice Register

	0	**Instruction Level 1 Cache Disable** Format: Disable **Value** / **Name** / **Description** 0h / **[Default]** / Cache is enabled. 1h / / Reserved

Capabilities A

CAPID0_A_0_2_0_PCI - Capabilities A

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00044h

Populated by pulling relevant fuses.

DWord	Bit	Description
0	31:25	**Spare Fuses 1** Default Value: 00h Access: RO Variant _Custom_GTIReset: BUS Spare Fuse
	24	**Display FuSa disable** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS Fuse to disable FuSa
	23:4	**Spare Fuses 2** Default Value: 00000h Access: RO Variant _Custom_GTIReset: BUS Spare Fuses
	3	**VGT Enable Fuse** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS
	2	**Use Dedicated Memory Path** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS This bit indicates if the direct memory path is enabled or not. 1'b0 (Default) - Dedicated memory path is disabled 1'b1 - Dedicated memory path is enabled.

CAPID0_A_0_2_0_PCI - Capabilities A			
	1	**SVM Disable Fuse**	
		Default Value:	0b
		Access:	RO Variant
		_Custom_GTIReset:	BUS
	0	**Vtd Disable Fuse**	
		Default Value:	0b
		Access:	RO Variant
		_Custom_GTIReset:	BUS

Capabilities B

CAPID0_B_0_2_0_PCI - Capabilities B		
Register Space: PCI: 0/2/0 Size (in bits): 32		
Address: 00048h		
Populated by pulling relevant fuses.		
DWord	**Bit**	**Description**
0	31:0	**Reserved Fuses** Default Value: 0b Access: RO _Custom_GTIReset: BUS

Capabilities Control

CAPCTRL0_0_2_0_PCI - Capabilities Control		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	00042h	
DWord	**Bit**	**Description**
0	15:12	**Reserved** Access: RO Format: MBZ
	11:8	**CAPID Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
	7:0	**CAPID Length** Default Value: 00001100b Access: RO _Custom_GTIReset: BUS This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).

Capabilities Pointer

CAPPOINT_0_2_0_PCI - Capabilities Pointer		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	00034h	
This register points to a linked list of capabilities implemented by this device.		
DWord	**Bit**	**Description**
0	7:0	**Capabilities Pointer Value** Default Value: 01000000b Access: RO _Custom_GTIReset: BUS This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.

Capability Identifier

CAPID0_0_2_0_PCI - Capability Identifier

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00040h

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 01110000b Access: RO _Custom_GTIReset: BUS This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
	7:0	**Capability Identifier** Default Value: 00001001b Access: RO _Custom_GTIReset: BUS This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

CAPTURE_0_DSSM0

CAPTURE_0_DSSM0 - CAPTURE_0_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 0		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_0_DSSM1

CAPTURE_0_DSSM1 - CAPTURE_0_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 0		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_0_L3

CAPTURE_0_L3 - CAPTURE_0_L3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 0		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_1_DSSM0

CAPTURE_1_DSSM0 - CAPTURE_1_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 1		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_1_DSSM1

CAPTURE_1_DSSM1 - CAPTURE_1_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 0		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_1_L3

CAPTURE_1_L3 - CAPTURE_1_L3

Register Space: MMIO: 0/2/0

Size (in bits): 32

Capture Buffer DW 1

DWord	Bit	Description
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_2_DSSM0

CAPTURE_2_DSSM0 - CAPTURE_2_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 2		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_2_DSSM1

CAPTURE_2_DSSM1 - CAPTURE_2_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 2		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_2_L3

CAPTURE_2_L3 - CAPTURE_2_L3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 2		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_3_DSSM0

CAPTURE_3_DSSM0 - CAPTURE_3_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 3		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_3_DSSM1

CAPTURE_3_DSSM1 - CAPTURE_3_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 3		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_3_L3

CAPTURE_3_L3 - CAPTURE_3_L3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 3		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_4_DSSM0

CAPTURE_4_DSSM0 - CAPTURE_4_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 4		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_4_DSSM1

CAPTURE_4_DSSM1 - CAPTURE_4_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 4		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_4_L3

CAPTURE_4_L3 - CAPTURE_4_L3

Register Space: MMIO: 0/2/0

Size (in bits): 32

Capture Buffer DW 4

DWord	Bit	Description
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_5_DSSM0

CAPTURE_5_DSSM0 - CAPTURE_5_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 5		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_5_DSSM1

CAPTURE_5_DSSM1 - CAPTURE_5_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 5		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_5_L3

CAPTURE_5_L3 - CAPTURE_5_L3

Register Space: MMIO: 0/2/0

Size (in bits): 32

Capture Buffer DW 5

DWord	Bit	Description
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_6_DSSM0

CAPTURE_6_DSSM0 - CAPTURE_6_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 6		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_6_DSSM1

CAPTURE_6_DSSM1 - CAPTURE_6_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 6		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_6_L3

CAPTURE_6_L3 - CAPTURE_6_L3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 6		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_7_DSSM0

CAPTURE_7_DSSM0 - CAPTURE_7_DSSM0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 7		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_7_DSSM1

CAPTURE_7_DSSM1 - CAPTURE_7_DSSM1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Capture Buffer DW 7		
DWord	**Bit**	**Description**
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

CAPTURE_7_L3

CAPTURE_7_L3 - CAPTURE_7_L3

Register Space: MMIO: 0/2/0

Size (in bits): 32

Capture Buffer DW 7

DWord	Bit	Description
0	31:24	**Byte_3** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	23:16	**Byte_2** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	15:8	**Byte1** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS
	7:0	**Byte_0** Default Value: 00000000b default Access: RO _Custom_GTIReset: BUS

Catastrophic Event FIFO Status

CT_FIFO_STATUS - Catastrophic Event FIFO Status

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Status of the catastrophic event FIFO.

Programming Notes

When servicing page response interrupts is done, a '1' will be written to the "Done Reading" field. Note that "Done Reading" can be set before "FIFO Occupancy Count" becomes 0 (i.e. the interrupt handler may choose to not service all of the pending catastrophic events). If "Done Reading" is set prior to the FIFO going empty, then there will be a catastrophic event interrupt arbitration in the IOMMU to produce another interrupt (since catastrophic events have the highest priority).The Interrupt-Routing bit is sampled by HW when a 1 is written by SW to the Done-Reading bit. As a result, SW shall program Interrupt-Routing bit appropriately to maintain the routing of the interrupts (Host shall write 0) when updating the Done-Reading bit. This register is saved in the power context.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24	**Done Reading** Set by host CPU at the end of servicing the IOMMU page response event interrupt. Setting this field will lead to a new catastrophic event interrupt if the FIFO has at least one valid entry. "Done Reading" is cleared by hardware when the IOMMU interrupt is accepted. Note that there is a programming requirement for the Interrupt-routing bit when this bit is set by SW. 0h – Not done – Not done reading the event FIFO. 1h – Done **[Default]** – Done reading the event FIFO, so a new interrupt can be generated if the FIFO is not empty.
	23:18	**Reserved** Access: RO Format: MBZ
	17	**Mask** This bit, when set, causes HW to not report an interrupt to SW even when valid entries exist. HW continues to accumulate FIFO data when this bit is set. An interrupt is generated when this bit is cleared. SW must periodically clear bit and consume data to prevent HW stalls resulting from lack of credits. This bit being set when valid data is present will prevent RC6 entry.

CT_FIFO_STATUS - Catastrophic Event FIFO Status

16 — Interrupt Routing

Where interrupts will be routed. This field can be read or written by the host CPU.

Value	Name	Description
0h	Host **[Default]**	Interrupts will be routed to the host CPU.
1h	Reserved	Reserved

15:9 — Reserved

Access:	RO
Format:	MBZ

8 — Not Empty

Whether the catastrophic event FIFO has at least one valid entry. This field is written by the graphics hardware and can be read by the host CPU.

Value	Name
0h	FIFO empty **[Default]**
1h	FIFO not empty

7:2 — Reserved

Access:	RO
Format:	MBZ

1:0 — FIFO Occupancy Count

The number of valid entries in the catastrophic event FIFO. This field is updated every time the host CPU reads the FIFO or an IOMMU catastrophic event message write is received from the IOMMU/GAM. It is written by the graphics hardware and can be read by the host CPU.

Value	Name
[0,2]	Number of valid FIFO entries

Catastrophic Interrupt Context ID

CT_INTR_CTX_ID - Catastrophic Interrupt Context ID

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Reports the context ID at the top of the catastrophic interrupt FIFO. It is written by the graphics hardware and is read by the microkernel and host CPU.

Programming Notes

Catastrophic interrupt FIFO output's a qword data consisting of CTX_INTR_ERR_ID and CT_INTR_CTX_ID registers.
As part of the CAT Error interrupt service routine, SW/FW must first read to CT_INTR_ERR_ID register prior to reading this register.
Each read of this register results in a pop of the catastrophic interrupt FIFO.

DWord	Bit	Description
0	31:0	**Context ID** The context ID at the top of the catastrophic interrupt FIFO. This FIFO collects information about contexts that caused catastrophic faults.

CCS CSB

CCS_CSB - CCS CSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SW reads this offset to read the CSB entry at the top of the CSB fifo. Reads must occur in pairs to obtain a single 64 bit entry. The second read pops the entry off the CSB fifo.		
DWord	**Bit**	**Description**
0	31:0	**Context Status Buffer DW** Access: RO This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.

CCS CSB Fifo Status Register

CCS_CSB_FSR - CCS CSB Fifo Status Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
This RO register holds status of the CSB fifo.		
DWord	**Bit**	**Description**
0	31	**Not Empty** Access: RO
	30:16	**Reserved** Access: RO Format: MBZ
	15:8	**FIFO Maximum Occupancy Count** This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.
	7:0	**FIFO Occupancy Count** Access: RO

CDCLK_CTL

CDCLK_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	46000h-46003h
Name:	CD Clock Control
ShortName:	CDCLK_CTL
Reset:	global

This register is not reset by the device 2 FLR.

Restriction
These fields should only be changed as part of the Display Sequences for Changing CD Clock Frequency.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:22	**CD2X Divider Select** Access: Double Buffered _Custom_Display_DoubleBufferUpdatePoint: Pipe off or start of vertical blank This field selects how the CDCLK PLL output is divided before driving the display CD2X clock. This field is double buffered to align with the pipe from CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected. Value: 00b – Name: Divide by 1 Value: 10b – Name: Divide by 2 **[Default]** **Restriction** CD2X Divider Select must not be changed while more than one pipe is enabled. When one pipe is enabled, the CD2X Pipe Select must be set to that pipe before changing CD2X Divider Select.
	21:19	**CD2X Pipe Select** This field selects the pipe enable and vertical blank to be used for double buffering the CD2X Divider Select. Value: 000b – Name: Pipe A Value: 010b – Name: Pipe B

100b	Pipe C	
110b	Pipe D	
111b	None	Double buffer enable is tied to 1 so that writes to the CD2X Divider Select will take effect immediately.

18	**Reserved**
17	**Reserved**
16	**SSA Precharge Enable** This field is unused.

Value	Name
0b	Disable

15	**Reserved**
14:11	**Reserved**

Access:	RO
Format:	MBZ

10:0 **CD Frequency Decimal**

Format:	U10.1

This field selects the decimal value of the frequency for CD clock, which is used to generate divided down clocks for some display engine timers. This value is represented in a 10.1 format with 10 integer bits and 1 fractional bit.
Many possible values are listed here, and not all valid values are included. To find which values are valid for a project, refer to the clocks page for that project.

Program this field to select the pre-defined value that matches the CD frequency chosen by the CDCLK PLL and CD2X Divider. If no value is defined, program this field with the CD frequency, rounded to the closest 0.5, then minus one.

Value	Name	Description
00 1010 0111 0b	168 MHz CD **[Default]**	This value is default, but not valid.
00101011000b	172.8 MHz CD	
00101100100b	179.2 MHz CD	
00101100110b	180 MHz CD	
00101111110b	192 MHz CD	
01001100100b	307.2 MHz CD	
01 0011 0111 0b	312 MHz CD	
01010000110b	324 MHz CD	
01010001011b	326.4MHz CD	
01110111110b	480MHz CD	
10 0010 0111 0b	552 MHz CD	

CDCLK_CTL				
		10 0010 1100 0b	556.8 MHz CD	
		10 1000 0111 0b	648 MHz CD	
		10 1000 1100 0b	652.8 MHz CD	

CDCLK_PLL_ENABLE

CDCLK_PLL_ENABLE

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
CrashLogSaved:	true
CrashLogPriority:	2
CrashLogVisibility:	public
ExternalLongName:	DE CDCLK PLL Enable
ExternalDescription:	Display engine core PLL enable

Address:	46070h-46073h
Name:	CDCLK PLL Enable
ShortName:	CDCLK_PLL_ENABLE
Reset:	soft

This register is used to control the CDCLK PLL.

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the CDCLK PLL. Value: 0b – Disable; 1b – Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the CDCLK PLL Lock. Value: 0b – Not locked or not enabled; 1b – Locked
	29:28	**Reserved** Access: RO Format: MBZ
	27	**Slow Clock Enable** This field enables or disables the slow clock that can be used when the CDCLK PLL is disabled. If the CDCLK PLL is disabled, and slow clock is disabled or not locked, then the crystal clock will be used instead. Value: 0b – Disable; 1b – Enable

CDCLK_PLL_ENABLE

26 — Slow Clock Lock

Access:	RO

This fields indicates the status of the slow clock lock.

Value	Name
0b	Not locked or not enabled
1b	Locked

25:24 — Reserved

Access:	RO
Format:	MBZ

23:22 — Reserved

Access:	RO
Format:	MBZ

21:12 — Reserved

Access:	RO
Format:	MBZ

11 — Reserved

Access:	RO
Format:	MBZ

10:8 — Reserved

Access:	RO
Format:	MBZ

7:0 — PLL Ratio

This field selects the CDCLK PLL divider ratio, controlling the output frequency.
Refer to the Clocks page for valid ratios to program.

Value	Name	Description
1Ch	28 default **[Default]**	Default value. Refer to the Clocks page for valid ratios to program.

Restriction
This field must be configured before enabling CDCLK PLL and not changed while it is enabled.

CGE_CTRL

CGE_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank

Address:	49080h-49083h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_A
Reset:	soft

Address:	49180h-49183h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_B
Reset:	soft

Address:	49280h-49283h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_C
Reset:	soft

Address:	49380h-49383h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_D
Reset:	soft

DWord	Bit	Description
0	31	**CGE Enable** This bit enables the Color Gamut Enhancement logic. Value: 0b – Disable; 1b – Enable
	30	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for the CGE registers that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled. Value: 0b – Not Allowed; 1b – Allowed **[Default]**

CGE_CTRL		
	29:0	**Reserved** Access: RO Format: MBZ

CGE_WEIGHT

CGE_WEIGHT	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	160
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	49090h-490A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_A
Reset:	soft
Address:	49190h-491A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_B
Reset:	soft
Address:	49290h-492A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_C
Reset:	soft
Address:	49390h-493A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_D
Reset:	soft

These are the weights contained in the lookup up table (LUT) used in pipe color gamut enhancement. LUT index 0 contains the weight for the least saturated colors, and LUT index 16 contains the weight for the most saturated colors. Weight values can range from 00000b (100% of the enhanced output color is from the pipe gamma and CSC output corrected color) to 100000b (100% of the enhanced output color is from the pipe gamma and CSC input color).

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 3** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Access: RO Format: MBZ

CGE_WEIGHT

	21:16	**CGE Weight Index 2** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**CGE Weight Index 1** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**CGE Weight Index 0** This is the weight value for this color gamut enhancement LUT index.
1	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 7** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**CGE Weight Index 6** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**CGE Weight Index 5** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**CGE Weight Index 4** This is the weight value for this color gamut enhancement LUT index.
2	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 11** This is the weight value for this color gamut enhancement LUT index.

CGE_WEIGHT		
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**CGE Weight Index 10** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**CGE Weight Index 9** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**CGE Weight Index 8** This is the weight value for this color gamut enhancement LUT index.
3	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 15** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**CGE Weight Index 14** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**CGE Weight Index 13** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**CGE Weight Index 12** This is the weight value for this color gamut enhancement LUT index.
4	31:6	**Reserved** Access: RO Format: MBZ

CGE_WEIGHT		
	5:0	**CGE Weight Index 16** This is the weight value for this color gamut enhancement LUT index.

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02338h-0233Fh
Name:	Clipper Invocation Counter
ShortName:	CL_INVOCATION_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18338h-1833Fh
Name:	Clipper Invocation Counter
ShortName:	CL_INVOCATION_COUNT_POCSUNIT_BE_GEOMETRY

This register stores the count of objects entering the Clipper stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**CL Invocation Count Report UDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)
	31:0	**CL Invocation Count Report LDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02340h-02347h
Name:	Clipper Primitives Counter
ShortName:	CL_PRIMITIVES_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18340h-18347h
Name:	Clipper Primitives Counter
ShortName:	CL_PRIMITIVES_COUNT_POCSUNIT_BE_GEOMETRY

This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**Clipped Primitives Output Count UDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)
	31:0	**Clipped Primitives Output Count LDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)

Command Buffer Caching Control Register

CMD_BUF_CCTL - Command Buffer Caching Control Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02084h-02087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_RCSUNIT
Address:	18084h-18087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_POCSUNIT
Address:	22084h-22087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_BCSUNIT
Address:	1C0084h-1C0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT0
Address:	1C4084h-1C4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT1
Address:	1C8084h-1C8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT0
Address:	1D0084h-1D0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT2
Address:	1D4084h-1D4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT3
Address:	1D8084h-1D8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT1
Address:	1E0084h-1E0087h
Name:	CMD_BUF_CCTL

CMD_BUF_CCTL - Command Buffer Caching Control Register

ShortName:	CMD_BUF_CCTL_VCSUNIT4
Address:	1E4084h-1E4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT5
Address:	1E8084h-1E8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT2
Address:	1F0084h-1F0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT6
Address:	1F4084h-1F4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT7
Address:	1F8084h-1F8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT3
Address:	1A084h-1A087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_CCSUNIT0

This register informs the size of the command buffer cache allocated in L3 for DMA requests from Command Streamer. This register also defines the MOCS index that need be send on command buffer read request to be cached in L3.

Programming Notes

This register only functionally impacts the render command streamer as the **Enable Command Cache** bit in PIPE_CONTROL is only supported for the render command streamer. Only render command streamer enables this register a non-privilege.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Mask bits act as write enables for the bits in the lower bits of this register
	15:14	**Reserved** Access: RO Format: MBZ

CMD_BUF_CCTL - Command Buffer Caching Control Register

13:12 **Reserved**

Access:	RO
Format:	MBZ

11:8 **Command Buffer Cache Size**

Format:	U4

The value programmed to this field should be less than or equal to the actual physical cache space reserved in L3 for command buffercaching through L3 configuration. Command buffer DMA engine uses the cache size programmed in this field to limit the read requests of a cacheable batch buffer to be cached in L3. DMA engine does this by tracking the amount of read requests made cacheable and stops caching when the read requested data size equals to the size of the command cache allocated. DMA engine resets the command caching tracker on events listed below. This avoids thrashing of cache for Batch Buffers larger in size compared to the command buffer cache allocated in L3.

- On an End Of Tile in PTRBR/POSH mode of operation.
- On a context save of a context.
- On command cache invalidation through PIPE_CONTROL.

Value	Name	Description
1h	Cache Size 16 KB **[Default]**	Size of the command buffer cache allocated in L3 is 16KB
2h	Cache Size 32 KB	Size of the command buffer cache allocated in L3 is 32KB
3h	Cache Size 64 KB	Size of the command buffer cache allocated in L3 is 64KB
4h	Cache Size 128 KB	Size of the command buffer cache allocated in L3 is 128KB
5h	Cache Size 256 KB	Size of the command buffer cache allocated in L3 is 256KB
6h	Cache Size 512 KB	Size of the command buffer cache allocated in L3 is 512KB
0h,7h,8h,9h, Ah, Bh, Ch, Dh, Eh, Fh	Reserved	Reserved.

7 **Reserved**

Access:	RO
Format:	MBZ

6:0 **Memory Object Control State MOCS for Command Buffer Caching**

Format:	MEMORY_OBJECT_CONTROL_STATE

This field has the standard format defined for MOCS globally. Index to MOCS Tables field of MOCS is used for L3 and System cache memory properties.
Index to MOCS Tables attribute of this field is used for defining the caching properties for requests made for batch buffer command fetches.

Comp Ctx TLB Invalidation Register

COMPCTX_TLB_INV_CR - Comp Ctx TLB Invalidation Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CF04h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000000000000000b Access: R/W
	15:8	**Reserved** Access: RO Format: MBZ
	7	**Invalidate Compute Ctx TLBs bit7** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.
	6	**Invalidate Compute Ctx TLBs bit6** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.
	5	**Invalidate Compute Ctx TLBs bit5** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.

COMPCTX_TLB_INV_CR - Comp Ctx TLB Invalidation Register

	4	**Invalidate Compute Ctx TLBs bit4** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.
	3	**Invalidate Compute Ctx TLBs bit3** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.
	2	**Invalidate Compute Ctx TLBs bit2** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bitwhen invalidation is complete. To ensure proper invalidation of the TLBs, SW has toensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all itsmemory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.
	1	**Invalidate Compute Ctx TLBs bit1** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.
	0	**Invalidate Compute Ctx TLBs bit0** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated Compute Context and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's (compute context's) HW pipeline is flushed and cleared from all its

COMPCTX_TLB_INV_CR - Comp Ctx TLB Invalidation Register		
		memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. Bit[7:0] invalidates Compute Context[7:0] TLBs. No Effect on non-existent Compute Contexts. These bits self clear.

Compute Engine DSS Reservation

CE_DSS_RSERVATION - Compute Engine DSS Reservation

Register Space: MMIO: 0/2/0

Size (in bits): 32

This register indicates the number of DSSs to be reserved for compute engine. This register is privileged and power context save/restored by HW.

DWord	Bit	Description
0	31:16	**MASK** Access: RO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:8	**Reserved** Format: PBC
	7:0	**Number ComputeEngine DSS Reservation** Format: U8 This field indicates the number of DSSs to be reserved for compute engine. These DSSs will be exclusively reserved for compute engine and will never be allocated for render engine. **Programming Notes** Value programmed must be less than the maximum number of DSS's available on a given GT SKU.

Config to MCI HI

CFGTOMCIDFTHI - Config to MCI HI		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	098A0h	
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31	**CFG to MCI HI dispatch** Access: R/WC _Custom_GTIReset: BUS
	30	**CFG to MCI HI error clear** Access: R/WC _Custom_GTIReset: BUS
	29:20	**RSVD_29_20** Access: R/WC _Custom_GTIReset: BUS
	19:0	**BitField: MCI DFT Ring Write data[39:20]. When dispatch is hi, then [39:20] is taken from here and [19:0] is taken from CFGTOMCIDFTLO** Access: R/WC _Custom_GTIReset: BUS

Config to MCI LO

CFGTOMCIDFTLO - Config to MCI LO		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 0989Ch		
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31	**CFG to MCI LO dispatch** Access: R/WC _Custom_GTIReset: BUS
	30:20	**MCI DFT Ring Write data[30:20]. When dispatch is lo, then [30:20] is taken from here and [39:31] is taken from [19:11] of CFGTOMCIDFTHI** Access: R/WC _Custom_GTIReset: BUS
	19:0	**MCI DFT Ring Write data[19:0]** Access: R/WC _Custom_GTIReset: BUS

Config to MCI STATUS1

CFGTOMCIDFTSTATUS1 - Config to MCI STATUS1		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 098A4h		
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31:5	**RSVD_31_5** Access: RO _Custom_GTIReset: BUS
	4	**report fifo empty** Access: RO _Custom_GTIReset: BUS
	3	**Reserved**
	2	**Reserved**
	1	**mci fifo overflow** Access: RO _Custom_GTIReset: BUS
	0	**report fifo overflow** Access: RO _Custom_GTIReset: BUS

Configuration Register0 for RPMunit

CONFIG0 - Configuration Register0 for RPMunit

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D00h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30:7	**Placeholder Bits** Access: R/W Lock _Custom_GTIReset: BUS
	6	**Reserved**
	5:3	**Crystal Clock Freq Selector** Access: RO _Custom_GTIReset: BUS This indicates the crystal clock frequency. BIOS will read this bit and then program the shift parameters, below, appropriately

Value	Name
0b	Crystal clock is at 24 MHz **[Default]**
1b	Crystal clock is at 19.2 MHz
10b	Crystal clock is at 38.4 MHz
11b	Crystal clock is at 25 MHz
100b	Rsvd for future use

	2:1	**CTC SHIFT parameter** Default Value: 10b Access: R/W Lock _Custom_GTIReset: BUS 00 - use bit 7 as microsecond, bit 3 as lowest *CS timestamp 01 - use bit 6 as microsecond, bit 2 as lowest *CS timestamp 10 - use bit 5 as microsecond, bit 1 as lowest *CS timestamp (default) 11 - use bit 4 as microsecond, bit 0 as lowest *CS timestamp

CONFIG0 - Configuration Register0 for RPMunit

	0	**Disable TSC Synchronization** Access: R/W Lock _Custom_GTIReset: BUS 'b0 - TSC synchronization enabled in GT (default) 'b1 - TSC synchronization DISABLED in GT

Configuration Register1 for RPMunit

CONFIG1 - Configuration Register1 for RPMunit

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D04h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30:10	**Placeholder Bits** Access: R/W Lock _Custom_GTIReset: BUS
	9	**Reserved**
	8:0	**RCP L3 FREQ DETECT** Default Value: 000011110b Access: R/W Lock _Custom_GTIReset: BUS This is control signal needed from clock unit that can be set at 1 when 2X clock frequency is less than or equal to 1GHz. It needs to be at 0 when 2X clock frequency is >1GHz. Without this circuit changes, the GT L3 cache will not be functional at lower frequency due to Vcc is less than Vccmin of 0.9V for the array. default value: low2xthresh=0x01Eh corresponding to a 1x frequency of 500Mhz.

CONTEXT_SCHEDULING_ATTRIBUTES

CONTEXT_SCHEDULING_ATTRIBUTES - CONTEXT_SCHEDULING_ATTRIBUTES	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	025A8h-025ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_RCSUNIT
Address:	185A8h-185ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_POCSUNIT
Address:	225A8h-225ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_BCSUNIT
Address:	1C05A8h-1C05ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT0
Address:	1C45A8h-1C45ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT1
Address:	1C85A8h-1C85ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VECSUNIT0
Address:	1D05A8h-1D05ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT2
Address:	1D45A8h-1D45ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT3
Address:	1D85A8h-1D85ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VECSUNIT1
Address:	1E05A8h-1E05ABh

CONTEXT_SCHEDULING_ATTRIBUTES - CONTEXT_SCHEDULING_ATTRIBUTES

Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT4
Address:	1E45A8h-1E45ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT5
Address:	1E85A8h-1E85ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VECSUNIT2
Address:	1F05A8h-1F05ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT6
Address:	1F45A8h-1F45ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VCSUNIT7
Address:	1F85A8h-1F85ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_VECSUNIT3
Address:	1A5A8h-1A5ABh
Name:	CONTEXT_SCHEDULING_ATTRIBUTES
ShortName:	CONTEXT_SCHEDULING_ATTRIBUTES_CCSUNIT0

Programming Notes

This register is only functional on RenderCS and ComputeCS and must be only programmed on RenderCS and ComputeCS. This register is context save/restored on a context switch.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Mask bits act as write enables for the bits in the lower bits of this register
	15:2	**Reserved** Format: PBC
	1:0	**Reserved** Format: PBC

Context Info of Per-process GTT Space HDW

CTXT_INFO_HDW - Context Info of Per-process GTT Space HDW	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

This register matches the format required by GAM in the Element Descriptor register. HW stores the programmed values of the Per Process GTT registers across RC6 and re-sends them to the GAM on a RC6 resume, causing GAM to attempt to reload per process table pointers from memory. To avoid loading Per Process structures un-necessarily and to avoid issues with stale Per Process loads (if a application or context that used a per process table terminates), SW shall program the Per Process registers when needed and disable right after use. This register is saved in the power context.

DWord	Bit	Description
0	31:0	**Context ID** This field is available for SW to set to any value it wishes. It can be used to differentiate different instances of the same context or to serve as a lookup value in a context structure so SW does not have to search for a context by LRCA. This ID will also appear in the status writes and can be used to associate status with submitted contexts.

Context Info of Per-process GTT Space LDW

CTXT_INFO_LDW - Context Info of Per-process GTT Space LDW

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

This register matches the format required by GAM in the Element Descriptor register. HW stores the programmed values of the Per Process GTT registers across RC6 and re-sends them to the GAM on a RC6 resume, causing GAM to attempt to reload per process table pointers from memory. To avoid loading Per Process structures un-necessarily and to avoid issues with stale Per Process loads (if a application or context that used a per process table terminates), SW shall program the Per Process registers when needed and disable right after use. This register is saved in the power context.

DWord	Bit	Description
0	31:12	**Logical Ring Context Address (LRCA)** Format: GraphicsAddress[31:12] This field contains the 4 KB-aligned address of the Logical Ring Context associated with this execlist element.
	11:9	**Function Number** GFX device is considered to be on Bus0 with device number of 2. Function number is normally assigned as "0" however for gfx virtualization; there would be different function numbers which needs to be attached to context.
	8	**Privileged Context / GGTT vs PPGTT mode** Differs in legacy vs advanced context modes: **In Legacy Context**: Defines the page tables to be used. This is how page walker come to know PPGTT vs GGTT selection for the entire context. **In Advanced Context**: Defines the privilege level for the context
	7:6	**Fault Handling**
	5	**Deeper IA coherency Support** **In Advanced Context**: Defines the level of IA coherency

Value	Name	Exists If
0h	Use Global GTT	[Context Type] == 'Legacy Context'
1h	Use Per-Process GTT	[Context Type] == 'Legacy Context'
0h	User Mode Context	[Context Type] == 'Advanced Context'
1h	Supervisor Mode Context	[Context Type] == 'Advanced Context'

Value	Name
00b	Fault & Hang
01b	Fault & Halt/Wait
10b	Fault & Stream & Switch
11b	Reserved

Value	Name	Description
0h		IA coherency is provided at LLC level for all streams of GPU (i.e. gen7.5 like mode)

CTXT_INFO_LDW - Context Info of Per-process GTT Space LDW

	1h		IA coherency is provided at L3 level for EU data accesses of GPU

4 — A&D Support / 32&64b Address Support

Differs in legacy vs advanced context modes: **In Legacy Context**: Defines 32b vs 64b (48b canonical) addressing format **In Advanced Context**: Defines A&D bit support

Value	Name	Exists If
0h	32b addressing format	[Context Type] == 'Legacy Context'
1h	64b (48b canonical) addressing format	[Context Type] == 'Legacy Context'
0h	A&D bit management in page tables is NOT supported	[Context Type] == 'Advanced Context'
1h	A&D bit management in page tables is supported.	[Context Type] == 'Advanced Context'

3 — Context Type

Defines the context type. *Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.*

Value	Name	Description
0h	Advanced Context	Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU.
1h	Legacy Context	Defines the context as legacy mode which is similar to prior

2 — Force Restore

Setting this bit will force a context restore operation when switching to this context even if the LRCA in the CCID register (normally the LRCA of the last context from the prior execlist) matches this one. Note that it is legal (and likely desirable) for the **Render Context Restore Inhibit** bit (part of the CTXT_SR_CTL register) in the context image being restored to also be set. The "ring" context is being forced to be restored from a newly initialized context despite a possible LRCA match; however, the render context for such a newly initialized context will likely be uninitialized and so should not be restored

1 — Scheduling Mode

Value	Name	Description
0h		Not valid
1h	**[Default]**	Indicates Execlist mode of scheduling.

0 — Valid

Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it will continue but flag an error.

Context Restore Request To TDL

TDL_CONTEXT_RESTORE - Context Restore Request To TDL

Register Space:	MMIO: 0/2/0
Access:	WO
Size (in bits):	32
Address:	0E418h

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**Context Restore Mask** Value: 1 — Name: — Description: Bit 0 and bit 16 both need to be 1 for Context restore request
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Context Restore** Value: 1 — Name: — Description: Bit 0 and bit 16 both need to be 1 for Context restore request

Context Sizes

CXT_SIZE - Context Sizes

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	021A8h

The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.

This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27:16	**Render Engine Context Size** This field indicates the size of the render engine context data that needs to be save/restored when extended mode is not enabled for a context; this excludes URB context size. Note that this excludes the ring context image size and the engine context saved by CSFE. Value: 15Eh — Name: **[Default]**
	15:8	**SOL Context Offset** This field indicates the cacheline aligned offset of the SOL context in the render context image starting from Ring Context. Note that in execlist of scheduling Ring context itself is at 4KBoffset from LRCA. Value: 66h — Name: **[Default]**
	7:0	**Reserved** Access: RO Format: MBZ

Context Status Buffer1 Contents

CTXT_ST_BUF1 - Context Status Buffer1 Contents	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	384
_Custom_GTIReset:	DEV
Address:	023C0h-023EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_RCSUNIT
Address:	183C0h-183EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_POCSUNIT
Address:	223C0h-223EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_BCSUNIT
Address:	1C03C0h-1C03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT0
Address:	1C43C0h-1C43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT1
Address:	1C83C0h-1C83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT0
Address:	1D03C0h-1D03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT2
Address:	1D43C0h-1D43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT3
Address:	1D83C0h-1D83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT1
Address:	1E03C0h-1E03EFh
Name:	Context Status Buffer1 Contents

CTXT_ST_BUF1 - Context Status Buffer1 Contents

ShortName:	CTXT_ST_BUF1_VCSUNIT4

Address:	1E43C0h-1E43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT5

Address:	1E83C0h-1E83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT2

Address:	1F03C0h-1F03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT6

Address:	1F43C0h-1F43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT7

Address:	1F83C0h-1F83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT3

Address:	1A3C0h-1A3EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_CCSUNIT0

All "Context Status* LDW" have the format of the Bits[31:0] of the "Context Status" definition.
All "Context Status* UDW" have the format of the Bits[61:32] of the "Context Status" definition.

Programming Notes

This structure contains the Context Switch status locations Context Status 6 to Context Status 11.

DWord	Bit	Description
0	63:32	**Context Status 6 UDW** Format: U32
	31:0	**Context Status 6 LDW** Format: U32
1	63:32	**Context Status 7 UDW** Format: U32
	31:0	**Context Status 7 LDW** Format: U32
2	63:32	**Context Status 8 UDW** Format: U32

CTXT_ST_BUF1 - Context Status Buffer1 Contents		
	31:0	**Context Status 8 LDW** Format: U32
3	63:32	**Context Status 9 UDW** Format: U32
	31:0	**Context Status 9 LDW** Format: U32
4	63:32	**Context Status 10 UDW** Format: U32
	31:0	**Context Status 10 LDW** Format: U32
5	63:32	**Context Status 11 UDW** Format: U32
	31:0	**Context Status 11 LDW** Format: U32

Context Status Buffer Contents

CTXT_ST_BUF - Context Status Buffer Contents	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	384
_Custom_GTIReset:	DEV
Address:	02370h-0239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_RCSUNIT
Address:	18370h-1839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_POCSUNIT
Address:	22370h-2239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_BCSUNIT
Address:	1C0370h-1C039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT0
Address:	1C4370h-1C439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT1
Address:	1C8370h-1C839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT0
Address:	1D0370h-1D039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT2
Address:	1D4370h-1D439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT3
Address:	1D8370h-1D839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT1
Address:	1E0370h-1E039Fh
Name:	Context Status Buffer Contents

CTXT_ST_BUF - Context Status Buffer Contents

ShortName:	CTXT_ST_BUF_VCSUNIT4
Address:	1E4370h-1E439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT5
Address:	1E8370h-1E839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT2
Address:	1F0370h-1F039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT6
Address:	1F4370h-1F439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT7
Address:	1F8370h-1F839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT3
Address:	1A370h-1A39Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_CCSUNIT0

Contents of the Execlist 0 in HW.

All "Context Status* LDW" have the format of the Bits[31:0] of the "Context Status" definition.
All "Context Status* UDW" have the format of the Bits[61:32] of the "Context Status" definition.

Programming Notes

This structure contains the Context Switch status locations Context Status 0 to Context Status 5.

This register functionality is not supported and must not be programmed for Position command streamer.

DWord	Bit	Description
0	63:32	**Context Status 0 UDW** Format: U32
	31:0	**Context Status 0 LDW** Format: U32
1	63:32	**Context Status 1 UDW** Format: U32
	31:0	**Context Status 1 LDW** Format: U32

CTXT_ST_BUF - Context Status Buffer Contents		
2	63:32	**Context Status 2 UDW** Format: U32
	31:0	**Context Status 2 LDW** Format: U32
3	63:32	**Context Status 3 UDW** Format: U32
	31:0	**Context Status 3 LDW** Format: U32
4	63:32	**Context Status 4 UDW** Format: U32
	31:0	**Context Status 4 LDW** Format: U32
5	63:32	**Context Status 5 UDW** Format: U32
	31:0	**Context Status 5 LDW** Format: U32

Context Status Buffer Interrupt Mask Register

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02218h-0221Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_RCSUNIT
Address:	18218h-1821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_POCSUNIT
Address:	22218h-2221Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_BCSUNIT
Address:	1C0218h-1C021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT0
Address:	1C4218h-1C421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT1
Address:	1C8218h-1C821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT0
Address:	1D0218h-1D021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT2
Address:	1D4218h-1D421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT3
Address:	1D8218h-1D821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT1
Address:	1E0218h-1E021Bh

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register

Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT4
Address:	1E4218h-1E421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT5
Address:	1E8218h-1E821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT2
Address:	1F0218h-1F021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT6
Address:	1F4218h-1F421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT7
Address:	1F8218h-1F821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT3
Address:	1A218h-1A21Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_CCSUNIT0

Hardware generates context switch interrupt and the associated context switch status report for the context switch reasons unmasked in this register. By default the context switch interrupts for all context switch reasons are un-masked. This register is privileged and global across all contexts and power context save/restored by hardware.
Note that on a context switch status report even the status of the masked context switch reasons are reported.

Programming Notes

Software must program this register through direct MMIO when hardware is idle and not processing any contexts.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**Active to Idle** This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch leading hardware to go idle. Active-to-Idle is a special case of element switch due to ring done or un-successful semaphore wait or un-successful display wait

for event following which hardware goes idle.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch leading hardware to go idle.
1		Context switch interrupt and associated context switch status report is not generated on a context switch leading hardware to go idle.

6 **Preempt to Idle**

This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch due to Preempt-to-Idle.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to Preempt-to-Idle.
1		Context switch interrupt and associated context switch status report is not generated on a context switch due to Preempt-to-Idle.

5 **Lite Restore**

This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch due to lite restore.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to lite restore.
1		Context switch interrupt and associated context switch status report is not generated on a context switch due to lite restore.

4 **Preemption**

This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch due to preemption. Preemption of an ongoing context is triggered due to loading of submission queue to execution queue on a "Load".

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to preemption.
1		Context switch interrupt and associated context switch status report is not generated on a context switch due to preemption.

3 **Display Wait For Event**

This mask bit controls the context switch interrupt generation and the associated context switch status report on Ring-Done context switch.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to un-successful display wait for event. Context switch on un-successful display wait for even wait is a part of element switch.

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register

		1		Context switch interrupt and associated context switch status report is not generated on a context switch due to un-successful display wait for event.
	2	**Semaphore Wait** This mask bit controls the context switch interrupt generation and the associated context switch status report on Ring-Done context switch.		
		Value	**Name**	**Description**
		0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to un-successful sempahore wait. Context switch on un-successful semaphore wait is a part of element switch.
		1		Context switch interrupt and associated context switch status report is not generated on a context switch un-successful semaphore wait.
	1	**Ring Done** This mask bit controls the context switch interrupt generation and the associated context switch status report on Ring-Done context switch.		
		Value	**Name**	**Description**
		0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch reason due to Ring-Done. Context switch on ring done is a part of element switch.
		1		Context switch interrupt and associated context switch status report is not generated on a context switch due to Ring-Done.
	0	**Idle To Active** This mask bit controls the context switch interrupt generation and the associated context switch status report on Idle-to-Active context switch.		
		Value	**Name**	**Description**
		0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to Idle-to-Active. Idle2Active is a special case of submission queue acceptance by hardware.
		1		Context switch interrupt and associated context switch status report is not generated on a context switch due to Idle-to-Active.

Context Status Buffer Read Register

CSB_STATUS - Context Status Buffer Read Register	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	023A4h-023A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_RCSUNIT
Address:	183A4h-183A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_POCSUNIT
Address:	223A4h-223A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_BCSUNIT
Address:	1C03A4h-1C03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT0
Address:	1C43A4h-1C43A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT1
Address:	1C83A4h-1C83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT0
Address:	1D03A4h-1D03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT2
Address:	1D43A4h-1D43A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT3
Address:	1D83A4h-1D83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT1
Address:	1E03A4h-1E03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT4
Address:	1E43A4h-1E43A7h

CSB_STATUS - Context Status Buffer Read Register

Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT5
Address:	1E83A4h-1E83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT2
Address:	1F03A4h-1F03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT6
Address:	1F43A4h-1F43A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT7
Address:	1F83A4h-1F83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT3
Address:	1A3A4h-1A3A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_CCSUNIT0

This 32 bit address contains the value of the context status that is next to be read by scheduler.

Programming Notes

This register functionality is not supported and must not be programmed for Position command streamer.

DWord	Bit	Description
0	31:0	**Context Status** Access: RO This field contains the value of the Context Status depending on the value of **Context Status Buffer Read Pointer** in the CTXT_ST_PTR. Read Pointer value of zero will point to context status zero, read pointer value of one will pointer to context status one, and so on. The scheduler must read this register twice to get the full 64b of context status. The first read returns the lower DW of the status and the second read returns the upper DW of the status.

Context Timestamp Count

CTX_TIMESTAMP - Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	023A8h-023ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_RCSUNIT
Address:	183A8h-183ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_POCSUNIT
Address:	223A8h-223ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_BCSUNIT
Address:	1C03A8h-1C03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT0
Address:	1C43A8h-1C43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT1
Address:	1C83A8h-1C83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT0
Address:	1D03A8h-1D03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT2
Address:	1D43A8h-1D43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT3
Address:	1D83A8h-1D83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT1
Address:	1E03A8h-1E03ABh
Name:	Context Timestamp Count

CTX_TIMESTAMP - Context Timestamp Count

ShortName:	CTX_TIMESTAMP_VCSUNIT4
Address:	1E43A8h-1E43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT5
Address:	1E83A8h-1E83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT2
Address:	1F03A8h-1F03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT6
Address:	1F43A8h-1F43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT7
Address:	1F83A8h-1F83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT3
Address:	1A3A8h-1A3ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_CCSUNIT0

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch.

DWord	Bit	Description
0	31:0	**Timestamp Value** Format: U32 The granularity of this toggle is at the rate of the bit 3 in the "Reported Timestamp Count" register(0x2358).. The toggle will be 8 times slower that "Reported Timestamp Count". The granularity of the time stamp base unit for "Reported Timestamp Count" is defined in the Timestamp Bases subsection in Power Management chapter.

Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020CCh-020CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_RCSUNIT
Address:	180CCh-180CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_POCSUNIT
Address:	220CCh-220CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_BCSUNIT
Address:	1C00CCh-1C00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT0
Address:	1C40CCh-1C40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT1
Address:	1C80CCh-1C80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT0
Address:	1D00CCh-1D00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT2
Address:	1D40CCh-1D40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT3
Address:	1D80CCh-1D80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT1
Address:	1E00CCh-1E00CFh
Name:	Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management

ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT4
Address:	1E40CCh-1E40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT5
Address:	1E80CCh-1E80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT2
Address:	1F00CCh-1F00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT6
Address:	1F40CCh-1F40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT7
Address:	1F80CCh-1F80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT3
Address:	1A0CCh-1A0CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_CCSUNIT0

This register gets power context save/restored. Bit[0] contents of this register does't get save/restored.Note: Even though this register exists in BlitterCS, VideoCS, VidoeEnhancmentCS, individual bit driven functionality is not supported.

Programming Notes
This register is functional for RenderCS only and must not be programmed for other command streamers.
This register functionality is not supported and must not be programmed for Position command streamer.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Selective Read Addressing Enable** Source: RenderCS, ComputeCS This field controls the outbound read request originating from Render Command Streamer. This field enables to read the MMIO register from selected unit in a given slice and sub-slice instead of multicasting the read cycle to all slices/sub-slices.

WAIT_FOR_RC6_EXIT - Control Register for Power Management

Value	Name	Description
0h	**[Default]**	Lowest Slice and Lowest Sub-Slice Enabled. Ex: Slice-0, Sub-Slice-0 are the lowest in GT.
1h	Selective Unit Enabled	Unit selected based on **Selective Read Slice Select** and **Selective Read Sub-Slice Select**.

14 **Reserved**

Source:	RenderCS, ComputeCS
Format:	PBC

13:12 **Selective Read Slice Select**

Source:	RenderCS, ComputeCS

This field selects the slice from which the read return data value has to be considered when **Selective Read Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.

Value	Name
0h	Slice-0
1h	Slice-1
2h	Slice-2
3h	Slice-3

11:9 **Selective Read Sub-Slice Select**

Source:	RenderCS, ComputeCS

This field selects the sub-slice from which the read return data value has to be considered when **Selective Read Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.

Value	Name
000b	Sub Slice-0
001b	Sub Slice-1
010b	Sub Slice-2
011b	Sub Slice-3
100b	Sub Slice-4
101b	Sub Slice-5
110b	Sub Slice-6
111b	Sub Slice-7

8 **Selective Write Addressing Enable**

Source:	RenderCS, ComputeCS

This field controls the outbound write request on message channel originating from Render Command Streamer on executing LRI, LRR and LRM commands. Setting this field doesn't affect the execution of LRI commands from context image during context restore. This field enables to

select the unit in given slice and sub-slice instead of multicasting the write cycle to all slices/half-slices.

Value	Name	Description
0h	Multi Cast **[Default]**	
1h	Selective Unit Enabled	Unit selected based on **Selective Write Slice Select** and **Selective Write Sub-Slice Select**.

Programming Notes
This field is used to implement per-slice performance counting by limiting which slices receive Flex EU programming.

7 **Reserved**

Source:	RenderCS, ComputeCS
Format:	PBC

6:5 **Selective Write Slice Select**

Source:	RenderCS, ComputeCS

This field selects the slice to which the write has to be done when **Selective Write Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.

Value	Name
000b	Slice-0
001b	Slice-1
010b	Slice-2
011b	Slice-3

Programming Notes
This field is used to implement per-slice performance counting by limiting which slices receive Flex EU programming. Please refer to Flex EU event for more details.

4:2 **Selective Write Sub-Slice Select**

Source:	RenderCS, ComputeCS

This field selects the Sub-Slice to which the write has to be done when **Selective Write Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.

Value	Name
000b	Sub Slice-0
001b	Sub Slice-1
010b	Sub Slice-2
011b	Sub Slice-3

WAIT_FOR_RC6_EXIT - Control Register for Power Management

		100b: Sub Slice-4 101b: Sub Slice-5 110b: Sub Slice-6 111b: Sub Slice-7
	1	**Reserved** Source: RenderCS, ComputeCS Format: PBC
	0	**Reserved** Source: RenderCS, ComputeCS Format: PBC

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

Address:	02290h-02297h
Name:	Count Active Channels Dispatched
ShortName:	TS_GPGPU_THREADS_DISPATCHED_RCSUNIT_BE_COMPUTE

Address:	1A290h-1A297h
Name:	Count Active Channels Dispatched
ShortName:	TS_GPGPU_THREADS_DISPATCHED_CCSUNIT_BE_COMPUTE0

This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h

DWord	Bit	Description
0..1	63:32	**GPGPU_THREADS_DISPATCHED UDW** Format: U32 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.
	31:0	**GPGPU_THREADS_DISPATCHED LDW** Format: U32 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.

Count of C6 Latency maximum

C6_EXIT_LATENCY_MAX - Count of C6 Latency maximum		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A620h	
Name:	Count of C6 Latency maximum	
ShortName:	C6_EXIT_LATENCY_MAX	
This register keeps track of the maximum Latency taken for C6 exit i.e from Boot evt to go to DILE		
DWord	**Bit**	**Description**
0	31:0	**C6 Latency Maximum** Access: RO _Custom_GTIReset: DEV Maximum C6 Latency

Count of Media License latency

CNT_MED_LIC_LAT - Count of Media License latency	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A0ECh
Name:	Count of Media License Latency
ShortName:	CNT_MED_LIC_LAT
This register keeps track of the Latency taken for Media License	

DWord	Bit	Description
0	31:0	**Media License Latency Count** Access: RO _Custom_GTIReset: BUS Count of Media License Latency

Count of Media License latency Maximum

CNT_MED_LIC_LAT_MAX - Count of Media License latency Maximum

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A0F8h
Name:	Count of Media License Latency Maximum
ShortName:	CNT_MED_LIC_LAT_MAX

This register keeps track of the Maximum Latency taken for Media License

DWord	Bit	Description
0	31:0	**Media License Latency Maximum Count** Access: RO _Custom_GTIReset: BUS Count of Media License Latency Maximum

Count of Media License Request

CNT_MED_LIC_REQ - Count of Media License Request	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A0E0h
Name:	Count of Media License Request
ShortName:	CNT_MED_LIC_REQ

This register keeps track of the number of Media License requests that have been sent

DWord	Bit	Description
0	31:0	**Media License Request Count** Access: RO _Custom_GTIReset: BUS Count of Media License Request

Count of Media Sampler License latency

CNT_MSAMP_LIC_LAT - Count of Media Sampler License latency	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A104h
Name:	Count of Media Sampler License latency
ShortName:	CNT_MSAMP_LIC_LAT

This register keeps track of the Latency taken for Media Sampler License

DWord	Bit	Description
0	31:0	**Media Sampler License Latency** Default Value: 000000000000000b Access: RO _Custom_GTIReset: BUS

Count of Media Sampler License latency Maximum

CNT_MSAMP_LIC_LAT_MAX - Count of Media Sampler License latency Maximum

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A108h
Name:	Count of Media Sampler License latency Maximum
ShortName:	CNT_MSAMP_LIC_LAT_MAX

This register keeps track of the Maximum Latency taken for Media Sampler License

DWord	Bit	Description
0	31:0	**Maximun Latency for Media Sampler Licensing Request** Default Value: 0000000000000000b Access: RO _Custom_GTIReset: BUS

Count of Media Sampler License Request

CNT_MSAMP_LIC_REQ - Count of Media Sampler License Request	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A100h
Name:	Count of Media Sampler License Request
ShortName:	CNT_MSAMP_LIC_REQ

This register keeps track of how many license requests have been sent out for Media Sampler

DWord	Bit	Description
0	31:0	**Number of Media Sampler License Request** Default Value: 000000000000000b Access: RO _Custom_GTIReset: BUS

Count of Render License latency

CNT_REN_LIC_LAT - Count of Render License latency		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A0E8h	
Name:	Count of Render License Latency	
ShortName:	CNT_REN_LIC_LAT	
This register keeps track of the Latency taken for Render License		
DWord	**Bit**	**Description**
0	31:0	**Render License Latency Count** Access: RO _Custom_GTIReset: BUS Count of Render License Latency

Count of Render License latency Maximum

CNT_REN_LIC_LAT_MAX - Count of Render License latency Maximum	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A0F4h
Name:	Count of Render License Latency Maximum
ShortName:	CNT_REN_LIC_LAT_MAX
This register keeps track of the Maximum Latency taken for Render License	

DWord	Bit	Description
0	31:0	**Render License Latency Maximum Value** Access: RO _Custom_GTIReset: BUS Count of Render License Latency Maximum

Count of Render License Request

CNT_REN_LIC_REQ - Count of Render License Request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A0DCh	
Name:	Count of Render License Request	
ShortName:	CNT_REN_LIC_REQ	
This register keeps track of the number of Render License Count		
DWord	**Bit**	**Description**
0	31:0	**Render License Request Count** Access: RO _Custom_GTIReset: BUS Count of Render License Request

Count of spec License Request

CNT_SPEC_LIC_REQ - Count of spec License Request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A0E4h	
Name:	Count of spec License Request	
ShortName:	CNT_SPEC_LIC_REQ	
DWord	**Bit**	**Description**
0	31:0	**Spec License Request Count** Access: RO _Custom_GTIReset: BUS Count of spec License Request

Count of Speculative License latency

CNT_SPEC_LIC_LAT - Count of Speculative License latency		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A0F0h	
Name:	Count of Speculative License Latency	
ShortName:	CNT_SPEC_LIC_LAT	
DWord	**Bit**	**Description**
0	31:0	**Speculative License Latency Value** Access: RO _Custom_GTIReset: BUS Count of Speculative License Latency

Count of Speculative License latency Maximum

CNT_SPEC_LIC_LAT_MAX - Count of Speculative License latency Maximum

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A0FCh
Name:	Count of Speculative License Latency Maximum
ShortName:	CNT_SPEC_LIC_LAT_MAX

This register keeps track of the Maximum Latency taken for Speculative License

DWord	Bit	Description
0	31:0	**Speculative License Latency Maximum Value** Access: RO _Custom_GTIReset: BUS Count of Speculative License Latency Maximum

CPS Invocation Counter

CPS_INVOCATION_COUNT - CPS Invocation Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02478h
Name:	CPS Invocation Counter
ShortName:	CPS_INVOCATION_COUNT

This register stores the value of the coarse pixel count shaded. This register is part of the context save and restore.

DWord	Bit	Description
0..1	63:32	**CPS Invocation Count Report UDW** Number of coarse pixels that are dispatched as threads by the PS Stage. Updated only when **Statistics Enable** is set in **3DSTATE_CPS**.
	31:0	**CPS Invocation Count Report LDW** Number of coarse pixels that are dispatched as threads by the PS Stage. Updated only when **Statistics Enable** is set in **3DSTATE_CPS**.

CSC_COEFF

CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49010h-49027h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_A
Reset:	soft

Address:	49110h-49127h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_B
Reset:	soft

Address:	49210h-49227h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_C
Reset:	soft

Address:	49310h-49327h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_D
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT

CSC_COEFF		
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ

CSC_MODE

CSC_MODE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	49028h-4902Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_A
Reset:	soft
Address:	49128h-4912Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_B
Reset:	soft
Address:	49228h-4922Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_C
Reset:	soft
Address:	49328h-4932Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_D
Reset:	soft

Writes to this register arm CSC registers for this pipe.

DWord	Bit	Description
0	31	**Pipe CSC Enable** This bit enables the pipe color space conversion.
	30	**Pipe Output CSC Enable** This bit enables the pipe output color space conversion.
	29	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for the Color Space Conversionregisters that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled. Value: 0b — Not Allowed Value: 1b — Allowed **[Default]**

CSC_MODE		
	28	**Reserved** Access: RO Format: MBZ
	27:0	**Reserved** Access: RO Format: MBZ

CSC_POSTOFF

CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49040h-4904Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_A
Reset:	soft

Address:	49140h-4914Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_B
Reset:	soft

Address:	49240h-4924Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_C
Reset:	soft

Address:	49340h-4934Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_D
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

CSC_POSTOFF		
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_PREOFF

CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49030h-4903Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_A
Reset:	soft

Address:	49130h-4913Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_B
Reset:	soft

Address:	49230h-4923Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_C
Reset:	soft

Address:	49330h-4933Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_D
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

CSC_PREOFF		
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CS CSB

CS_CSB - CS CSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SW reads this offset to read the Context Status Buffer entry at the top of the CSB fifo. Reads must occur in pairs to obtain a single 64bit CSB entry. The second read pops the CSB entry off the FIFO.		
DWord	**Bit**	**Description**
0	31:0	**Context Status Buffer DW** Access: RO This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.

CS CSB _FSR

CS_CSB_FSR - CS CSB _FSR		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
This RO register holds status of the CSB fifo.		
DWord	**Bit**	**Description**
0	31	**Not Empty** Access: RO
	30:16	**Reserved** Access: RO Format: MBZ
	15:8	**FIFO Maximum Occupancy Count** This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.
	7:0	**FIFO Occupancy Count**

CSFE FSM2

CSFEFSM2 - CSFE FSM2	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	022A4h-022A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_RCSUNIT
Address:	182A4h-182A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_POCSUNIT
Address:	222A4h-222A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_BCSUNIT
Address:	1C02A4h-1C02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT0
Address:	1C42A4h-1C42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT1
Address:	1C82A4h-1C82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT0
Address:	1D02A4h-1D02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT2
Address:	1D42A4h-1D42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT3
Address:	1D82A4h-1D82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT1
Address:	1E02A4h-1E02A7h
Name:	CSFE FSM2

CSFEFSM2 - CSFE FSM2

ShortName:	CSFEFSM2_VCSUNIT4
Address:	1E42A4h-1E42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT5
Address:	1E82A4h-1E82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT2
Address:	1F02A4h-1F02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT6
Address:	1F42A4h-1F42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT7
Address:	1F82A4h-1F82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT3
Address:	1A2A4h-1A2A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_CCSUNIT0

DWord	Bit	Description
0	31:30	**POCSLITERST** Format: MBZ
	29:27	**POCSELSUB** Format: MBZ
	26:23	**CTXSWM** Format: MBZ
	22:20	**CSRL_PREEMPT** Format: MBZ
	19:16	**CSCTXSW_CTXSEQ** Format: MBZ
	15:13	**CSPREP4SWITCH** Format: MBZ
	12:11	**SVWR** Format: MBZ

CSFEFSM2 - CSFE FSM2		
	10:9	**RRCRD** Format: MBZ
	8:6	**RENDCTX** Format: MBZ
	5:3	**CTXSEQ** Format: MBZ
	2:0	**RCURSTSEQ**

CS Indirect Base

CS_INDIRECT_BASE - CS Indirect Base

Register Space: MMIO: 0/2/0

Size (in bits): 32

This is a general-purpose register to hold data. This register is power context save/restored across idle sequences.
Data in this register is used as a base address in below mentioned MI commands upon ADD_INDIRECT_BASE field set.

- MI_LOAD_REGISTER_IMM
- MI_STORE_REGISTER_MEM
- MI_LOAD_REGISTER_MEM
- MI_LOAD_REGISTER_REG

DWord	Bit	Description
0	31:0	**Indirect Base** Access: R/W Format: U32

CS-LTISEQ Flush Message Register

CS_LTISEQ_FLSH_MSG - CS-LTISEQ Flush Message Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B464h

This register handles flush messaging between CS and LTISEQ.
Valid values are :
1. 0x00010001 : Tile Cache Flush Request
2. 0x00020002 : RCS Fabric Flush Request
2. 0x00040004 : CCS Fabric Flush Request

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2	**CCS Fabric Flush Request Message Bit** Access: R/W Hardware Clear _Custom_GTIReset: DEV Message Bit of Fabric flush request from CCS to LTISEQ. Bit[2] must be set to "1", along with Bit[18]=1, for Valid Fabric Flush Requests from Compute CS to LTISEQ.
	1	**Fabric Flush Request Message Bit** Access: R/W Hardware Clear _Custom_GTIReset: DEV Message Bit of Fabric flush request from CS to LTISEQ. Bit[1] must be set to "1", along with Bit[17]=1, for Valid Fabric Flush Requests from Render CS to LTISEQ.
	0	**Tile Cache Flush Request Message Bit** Access: R/W Hardware Clear _Custom_GTIReset: DEV Message Bit of Tile Cache flush request from CS to LTISEQ. Bit[0] must be set to "1", along with Bit[16]=1, for Valid Tile Cache Flush Requests from CS to LTISEQ.

CSPREEMPT

CSPREEMPT - CSPREEMPT

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	024B0h
Name:	CSPREEMPT
ShortName:	CSPREEMPT

Address:	224B0h
Name:	BCSPREEMPT
ShortName:	BCSPREEMPT

Address:	124B0h
Name:	VCSPREEMPT
ShortName:	VCSPREEMPT

Address:	1A4B0h
Name:	VECSPREEMPT
ShortName:	VECSPREEMPT

Programming Notes

This is for HW internal usage and must not be written by SW.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Unnamed** Format: Disable This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.

CUR_BASE

CUR_BASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	70084h-70087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_A
Reset:	soft
Address:	71084h-71087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_B
Reset:	soft
Address:	72084h-72087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_C
Reset:	soft
Address:	73084h-73087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_D
Reset:	soft

Writes to this register arm cursor registers for this pipe.

DWord	Bit	Description
0	31:12	**Cursor Base 31 12** Format: GraphicsAddress[31:12] This field specifies bits 31:12 of the graphics address of the base of the cursor for hi-res mode. When performing 180 degree rotation, this address does not need to change, hardware will internally offset to start from the last pixel of the last line of the cursor. **Workaround** To prevent false VT-d type 6 errors, use 64KB address alignment and allocate an extra 2 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves. **Restriction** The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.

CUR_BASE		
	11	**Reserved**
	10:7	**Reserved** Access: RO Format: MBZ
	6:4	**Reserved**
	3	**Reserved** Access: RO Format: MBZ
	2	**Reserved**
	1:0	**Reserved** Access: RO Format: MBZ

CUR_COLOR_CTL

CUR_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to CUR_BASE or cursor not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed

Address:	700C0h-700C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_A
Reset:	soft

Address:	710C0h-710C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_B
Reset:	soft

Address:	720C0h-720C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_C
Reset:	soft

Address:	730C0h-730C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_D
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Tone Mapping Enable** This field enables the tone mapping of cursor pixels using the programmed tone mapping factor. 1b – Enable 0b – Disable
	14:10	**Reserved** Access: RO Format: MBZ

CUR_COLOR_CTL		
	9:0	**Tone Mapping Factor** This field specifies the tone mapping factor. Each color component gets corrected with this programmed 10 bit fractional value.

CUR_CSC_COEFF

CUR_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to CUR_CTL
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	700D0h-700E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_A
Reset:	soft

Address:	710D0h-710E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_B
Reset:	soft

Address:	720D0h-720E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_C
Reset:	soft

Address:	730D0h-730E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_D
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT

CUR_CSC_COEFF		
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ

CUR_CTL

CUR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to CUR_BASE or cursor not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed

Address:	70080h-70083h
Name:	Cursor Control
ShortName:	CUR_CTL_A
Reset:	soft

Address:	71080h-71083h
Name:	Cursor Control
ShortName:	CUR_CTL_B
Reset:	soft

Address:	72080h-72083h
Name:	Cursor Control
ShortName:	CUR_CTL_C
Reset:	soft

Address:	73080h-73083h
Name:	Cursor Control
ShortName:	CUR_CTL_D
Reset:	soft

Address:	70880h-70883h
Name:	Selective Fetch Cursor Control
ShortName:	SEL_FETCH_CUR_CTL_A
Reset:	soft

The cursor is enabled by programming a valid cursor mode in the cursor mode select fields. The cursor is disabled by programming all 0s in the cursor mode select fields.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:28	**Pipe Slice Arbitration Slots** This field specifies the number of slots allocated to cursor in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.

CUR_CTL

27 Reserved

Access:	RO
Format:	MBZ

26 Gamma Enable

This bit enables pipe gamma correction for the cursor pixel data. In VGA pop-up operation, the cursor data will always bypass gamma.

This field is deprecated.

Value	Name
0b	Disable
1b	Enable

25 Reserved

Access:	RO
Format:	MBZ

24 Pipe CSC Enable

This bit enables pipe color space conversion for the cursor pixel data.

Use CSC_MODE.Pipe CSC Enable, GAMMA_MODE.*_GAMMA_ENABLE for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Cursor CSC must be used for cursor specific color space conversion.

This field is deprecated.

Value	Name
0b	Disable
1b	Enable

23 Allow Double Buffer Update Disable

Access:	R/W

This field controls whether double buffer updates are allowed to be disabled for this cursor. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled.

Value	Name
0b	Not Allowed
1b	Allowed

22:19 Reserved

Access:	RO
Format:	MBZ

CUR_CTL

18 Pre CSC Gamma Enable

This bit enables the cursor pre-CSC gamma for the cursor pixel data. This is generally used with HDR to de-gamma the sRGB cursor pixel data before the RGB2020 conversion.

Value	Name
0b	Disable
1b	Enable

17 Reserved

Access:	RO
Format:	MBZ

16 CSC Enable

This bit enables the cursor color space conversion for the cursor pixel data. Hardware uses the coefficients programmed in the CUR_CSC_COEFF registers to perform the color space conversion.

Value	Name
0b	Disable
1b	Enable

15 180 Rotation

This mode causes the cursor image to be rotated 180 degrees. In addition to setting this bit, the cursor position must be adjusted to match the physical orientation of the display.

Value	Name
0b	No rotation
1b	180 degree rotation

Restriction
Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.

14:12 Reserved

Access:	RO
Format:	MBZ

11:10 Force Alpha Plane Select

This field selects which planes the cursor alpha value will be forced for. It is used together with the Force Alpha Value field.

Value	Name	Description
00b	Disable	Disable alpha forcing
01b	Pipe CSC Enabled	Enable alpha forcing where cursor overlaps a plane that has enabled pipe CSC
10b	Pipe CSC Disabled	Enable alpha forcing where cursor overlaps plane that has disabled pipe CSC
11b	Reserved	Reserved

CUR_CTL

9:8 Force Alpha Value

This field controls the behavior of cursor when alpha blending onto certain plane pixels. It is used together with the Force Alpha Plane Select field.

Value	Name	Description
00b	Disable	Cursor pixels alpha blend normally over any plane.
01b	50	Cursor pixels with alpha >= 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).
10b	75	Cursor pixels with alpha >= 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).
11b	100	Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).

Restriction
Force Alpha is only for use with ARGB cursor formats.

7:6 Reserved

Access:	RO
Format:	MBZ

5:0 Cursor Mode Select

This field selects the cursor mode. Cursor is disabled when the selection is 000000b and enabled when the selection is any other value. The cursor vertical size can be overriden by the size reduction mode.

Color channels should be pre-multiplied with alpha by software.

Value	Name	Description
000000b	Disable	Cursor is disabled
000010b	128x128 32bpp AND/INV	128x128 32bpp AND/INVERT
000011b	256x256 32bpp AND/INV	256x256 32bpp AND/INVERT
000100b	64x64 2bpp 3-color	64x64 2bpp Indexed 3-color and transparency
000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color
000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color
000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT
100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR
100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR
100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR
100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)

Others	Reserved	Reserved

Programming Notes
INVERT, XOR, and alpha blends may not look as expected when the plane underlying the cursor is YUV or extended range RGB. Out of range RGB values will be clamped prior to alpha blending, INVERT, or XOR with cursor. It is recommended to use Force Alpha when cursor is alpha blending onto a plane of a different color space or extended gamut.
The AND/INVERT format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: Cursor inverts the color of the surface underneath.
The AND/XOR format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: The three least significant bytes are XOR'd with the color of the surface underneath.

CUR_FBC_CTL

CUR_FBC_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to CUR_BASE or cursor not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed

Address:	700A0h-700A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_A
Reset:	soft

Address:	710A0h-710A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_B
Reset:	soft

Address:	720A0h-720A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_C
Reset:	soft

Address:	730A0h-730A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**Size Reduction Enable** This enables cursor size reduction logic. The cursor engine will fetch and display the programmed reduced number of lines, then go transparent for the rest of the frame.

Value	Name
0b	Disable
1b	Enable

Restriction
Cursor size reduction is not allowed with 2bpp cursor formats or cursor 180 degree rotation. The reduced scan lines field must be programmed with a valid value when cursor size reduction is enabled.

<table>
<tr><th colspan="3">CUR_FBC_CTL</th></tr>
<tr><td></td><td>30:8</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>7:0</td><td>Reduced Scan Lines
This specifies the number of scan lines of cursor data to fetch and display when cursor size reduction is enabled. The value programmed is the size minus one.<table><tr><th>Restriction</th></tr><tr><td>The minimum size is 8 lines, programmed as 07h.The maximum size cannot be greater than the normal size when size reduction is not enabled.</td></tr></table></td></tr>
</table>

CUR_PAL

CUR_PAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	70090h-70093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_A
Reset:	soft
Address:	70094h-70097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_A
Reset:	soft
Address:	70098h-7009Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_A
Reset:	soft
Address:	7009Ch-7009Fh
Name:	Cursor Palette
ShortName:	CUR_PAL_3_A
Reset:	soft
Address:	71090h-71093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_B
Reset:	soft
Address:	71094h-71097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_B
Reset:	soft
Address:	71098h-7109Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_B
Reset:	soft
Address:	7109Ch-7109Fh

CUR_PAL	
Name:	Cursor Palette
ShortName:	CUR_PAL_3_B
Reset:	soft
Address:	72090h-72093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_C
Reset:	soft
Address:	72094h-72097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_C
Reset:	soft
Address:	72098h-7209Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_C
Reset:	soft
Address:	7209Ch-7209Fh
Name:	Cursor Palette
ShortName:	CUR_PAL_3_C
Reset:	soft
Address:	73090h-73093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_D
Reset:	soft
Address:	73094h-73097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_D
Reset:	soft
Address:	73098h-7309Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_D
Reset:	soft
Address:	7309Ch-7309Fh
Name:	Cursor Palette
ShortName:	CUR_PAL_3_D
Reset:	soft
The cursor palette provides color information when using the indexed cursor modes. There are 4 instances of	

CUR_PAL

this register format per cursor. The table below describes how the cursor mode and index value will select between the cursor palette colors, AND/XOR, transparency, and destination invert.

Index Value	2 color mode	3 color mode	4 color mode
00	CUR_PAL 0	CUR_PAL 0	CUR_PAL 0
01	CUR_PAL 1	CUR_PAL 1	CUR_PAL 1
10	Transparent	Transparent	CUR_PAL 2
11	Invert Destination	CUR_PAL 3	CUR_PAL 3

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**Palette Red** This field is the cursor palette red value
	15:8	**Palette Green** This field is the cursor palette green value.
	7:0	**Palette Blue** This field is the cursor palette blue value.

CUR_POS

CUR_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	70088h-7008Bh
Name:	Cursor Position
ShortName:	CUR_POS_A
Reset:	soft
Address:	71088h-7108Bh
Name:	Cursor Position
ShortName:	CUR_POS_B
Reset:	soft
Address:	72088h-7208Bh
Name:	Cursor Position
ShortName:	CUR_POS_C
Reset:	soft
Address:	73088h-7308Bh
Name:	Cursor Position
ShortName:	CUR_POS_D
Reset:	soft

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the display pipe source image area. When performing 180 degree rotation, the cursor image is rotated by hardware, but the position is not, so it should be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction
The cursor must have at least a single pixel positioned over the pipe source area. The cursor must not overlap both the left and right sides of the pipe source area.

DWord	Bit	Description
0	31	**Y Position Sign** This specifies the sign of the vertical position of the cursor upper left corner.
	30:29	**Reserved** Access: RO Format: MBZ

CUR_POS		
	28:16	**Y Position Magnitude** This specifies the magnitude of the vertical position of the cursor upper left corner in lines.
	15	**X Position Sign** This specifies the sign of the horizontal position of the cursor upper left corner.
	14:13	**Reserved** Access: RO Format: MBZ
	12:0	**X Position Magnitude** This specifies the magnitude of the horizontal position of the cursor upper left corner in pixels.

CUR_PRE_CSC_GAMC_DATA

CUR_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	700B4h-700B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_A
Reset:	soft
Address:	710B4h-710B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_B
Reset:	soft
Address:	720B4h-720B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_C
Reset:	soft
Address:	730B4h-730B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_D
Reset:	soft

CUR_PRE_CSC_GAMC_INDEX and CUR_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the cursor pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion if desired.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pre CSC Enable" bit in the CUR_CTL register.

CUR_PRE_CSC_GAMC_DATA

Programming Notes
To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction
The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Gamma Value** Default Value: 00000000000000000b Format: U3.16

CUR_PRE_CSC_GAMC_INDEX

CUR_PRE_CSC_GAMC_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	700B0h-700B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_A
Reset:	soft
Address:	710B0h-710B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_B
Reset:	soft
Address:	720B0h-720B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_C
Reset:	soft
Address:	730B0h-730B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_D
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. Value 0b: No Increment — Do not automatically increment the index value. Value 1b: Auto Increment **[Default]** — Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ

CUR_PRE_CSC_GAMC_INDEX

	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of pipe pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value** / **Name** [0,34]

CUR_SURFLIVE

CUR_SURFLIVE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	700ACh-700AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_A
Reset:	soft
Address:	710ACh-710AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_B
Reset:	soft
Address:	720ACh-720AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_C
Reset:	soft
Address:	730ACh-730AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_D
Reset:	soft
There is one instance of this register for each pipe.	

DWord	Bit	Description
0	31:12	**Live Surface Base Address** This gives the live value of the surface base address as being currently used for the cursor.
	11:0	**Reserved** Access: RO Format: MBZ

Customizable Event Creation 5-0

CEC5_0 - Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02798h

Description
This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –
	18:3	**Compare Value** Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC5_0 - Customizable Event Creation 5-0

2:0 **Compare Function**

Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

DATAM

DATAM	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60030h-60033h
Name:	Transcoder Data M Value 1
ShortName:	TRANS_DATAM1_A
Reset:	soft
Address:	61030h-61033h
Name:	Transcoder Data M Value 1
ShortName:	TRANS_DATAM1_B
Reset:	soft
Address:	62030h-62033h
Name:	Transcoder Data M Value 1
ShortName:	TRANS_DATAM1_C
Reset:	soft
Address:	63030h-63033h
Name:	Transcoder Data M Value 1
ShortName:	TRANS_DATAM1_D
Reset:	soft

This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:25	**TU or VCpayload Size** In DisplayPort SST mode this field is the size of the transfer unit, minus one. Typically it is programmed with a value of 63 for TU size of 64. In DisplayPort MST mode this field is the Virtual Channel payload size, minus one. **Restriction** In DisplayPort MST mode the Virtual Channel payload size must not be programmed greater than 62 (resulting payload size of 63). In DisplayPort MST mode the Virtual Channel payload size must not be changed while the Virtual Channel is enabled, even after a transcoder has been disabled.

DATAM		
	24	**Reserved** Access: RO Format: MBZ
	23:0	**Data M value** This field is the data M value for internal use.

DATAN

DATAN	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60034h-60037h
Name:	Transcoder Data N Value 1
ShortName:	TRANS_DATAN1_A
Reset:	soft
Address:	61034h-61037h
Name:	Transcoder Data N Value 1
ShortName:	TRANS_DATAN1_B
Reset:	soft
Address:	62034h-62037h
Name:	Transcoder Data N Value 1
ShortName:	TRANS_DATAN1_C
Reset:	soft
Address:	63034h-63037h
Name:	Transcoder Data N Value 1
ShortName:	TRANS_DATAN1_D
Reset:	soft
This register is double buffered to update on the next MSA after LINKN is written.	

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Data N value** This field is the data N value for internal use.

DBUF_CTL

DBUF_CTL		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	45008h-4500Bh	
Name:	DBUF Slice 1 Control	
ShortName:	DBUF_CTL_S1	
Reset:	soft	
Address:	44FE8h-44FEBh	
Name:	DBUF Slice 2 Control	
ShortName:	DBUF_CTL_S2	
Reset:	soft	

DWord	Bit	Description
0	31	**DBUF Power Request** Access: R/W This field requests DBUF power to enable or disable. 0b – Disable 1b – Enable **Programming Notes** DBUF power must be enabled prior to using internal display engine features. Enable power by programming the power request to 1, then wait for the power state to indicate it is enabled.
	30	**DBUF Power State** Access: RO This field indicates the status of DBUF power. 0b – Disabled 1b – Enabled
	29:28	**Reserved** Access: RO Format: MBZ
	27	**Reserved**

DBUF_CTL

	26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved**
	23:19	**Tracker State Service** Default Value: 1100b This field sets the maximum number of clocks before servicing tracker state.
	18:16	**Reserved** Access: RO Format: MBZ
	15:12	**CC Block Valid State Service** Default Value: 1100b This field sets the maximum number of clocks before servicing CC block valid state.
	11:10	**Reserved** Access: RO Format: MBZ
	9:8	**Reserved** Access: RO Format: MBZ
	7	**Reserved**
	6	**Reserved** Access: RO Format: MBZ
	5:4	**Reserved**
	3:0	**Reserved** Access: RO Format: MBZ

DBUF_CTL2

DBUF_CTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44FFCh-44FFFh
Name:	DBUF Slice 1 Control 2
ShortName:	DBUF_CTL2_S1
Reset:	soft
Address:	44FE4h-44FE7h
Name:	DBUF Slice 2 Control 2
ShortName:	DBUF_CTL2_S2
Reset:	soft

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:8	**HPUT Service Count** Forces an Hput to be serviced every number of programmed clocks. Value: 01010b — Name: **[Default]** Value: [1,31] — Name:
	7:4	**APUT Service Count** The number of time slots devoted to APUTs. Value: 0001b — Name: **[Default]** Value: [1,15] — Name:
	3:0	**Bypass Service Count** The number of time slots devoted to BYPASS Puts. Value: 0001b — Name: **[Default]** Value: [1,15] — Name:

DBUF_ECC_STAT

DBUF_ECC_STAT	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	45010h-45013h
Name:	DBUF Slice 1 ECC Status
ShortName:	DBUF_ECC_STAT_S1
Reset:	soft
Address:	44FF0h-44FF3h
Name:	DBUF Slice 2 ECC Status
ShortName:	DBUF_ECC_STAT_S2
Reset:	soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit.Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31	**Double Error Bank 15**
	30	**Double Error Bank 14**
	29	**Double Error Bank 13**
	28	**Double Error Bank 12**
	27	**Double Error Bank 11**
	26	**Double Error Bank 10**
	25	**Double Error Bank 9**
	24	**Double Error Bank 8**
	23	**Double Error Bank 7**
	22	**Double Error Bank 6**
	21	**Double Error Bank 5**
	20	**Double Error Bank 4**
	19	**Double Error Bank 3**
	18	**Double Error Bank 2**
	17	**Double Error Bank 1**
	16	**Double Error Bank 0**
	15	**Single Error Bank 15**
	14	**Single Error Bank 14**
	13	**Single Error Bank 13**

DBUF_ECC_STAT		
	12	**Single Error Bank 12**
	11	**Single Error Bank 11**
	10	**Single Error Bank 10**
	9	**Single Error Bank 9**
	8	**Single Error Bank 8**
	7	**Single Error Bank 7**
	6	**Single Error Bank 6**
	5	**Single Error Bank 5**
	4	**Single Error Bank 4**
	3	**Single Error Bank 3**
	2	**Single Error Bank 2**
	1	**Single Error Bank 1**
	0	**Single Error Bank 0**

DBUF_STATUS

DBUF_STATUS		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
Address:	4500Ch-4500Fh	
Name:	DBUF Slice 1 Status	
ShortName:	DBUF_STATUS_S1	
Reset:	soft	
Address:	44FECh-44FEFh	
Name:	DBUF Slice 2 Status	
ShortName:	DBUF_STATUS_S2	
Reset:	soft	

DWord	Bit	Description
0	31	**Spare31**
	30	**Dataout FIFO overrun** Access: R/WC A '1' indicates the DBUF out FIFO overrun. Sticky bit cleared by a write of '1'.
	29	**Spare29** Access: R/WC
	28	**EAck FIFO Overrun** A '1' indicates that the EAckFIFO overflowed. Sticky bit cleared by a write of '1'.
	27	**DROB Rsvd6** Access: R/WC
	26	**DROB Rsvd5** Access: R/WC
	25	**DROB Rsvd4** Access: R/WC
	24	**DROB Rsvd3** Access: R/WC
	23	**DROB Track Num FIFO Overrun** Access: R/WC A '1' indicates that the DROB Track Num FIFO overflowed. Sticky bit cleared by a write of '1'.
	22	**Spare22** Access: R/WC

DBUF_STATUS		
	21	**Tracker Over Allocated** Access: R/WC A '1' indicates that the Arbiter allocated more than 16 trackers. Sticky bit cleared by a write of '1'.
	20	**Eput Fifo Overrun** Access: R/WC Indication that the bypass fifo in coming into dbuf has overrun.
	19	**Spare19** Access: R/WC
	18	**Spare18** Access: R/WC
	17	**Spare17** Access: R/WC
	16	**Spare16** Access: R/WC
	15:0	**Reserved**

DC_STATE_EN

DC_STATE_EN

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
CrashLogSaved:	true
CrashLogPriority:	1
CrashLogVisibility:	public
ExternalLongName:	DE DC State Enable
ExternalDescription:	Display Engine C-state enable

Address:	45504h-45507h
Name:	Display C State Enable
ShortName:	DC_STATE_EN
Reset:	soft

DWord	Bit	Description
0	31	**MODE SET in Progress** This bit indicates that Mode set is in progress and DCPR will not generate any CSR_Start to DMC when set. Software needs to program this bit when mode set is started and software should reset it when mode set is done. Value: 0b – CSR_start generation not gated **[Default]** Value: 1b – CSR_start generation is gated
	30	**Display Clock Off Enable** This bit indicates that the DC*clock off is allowed. Driver must program this bit to 1 to allow the DMC to go the DC*CO states. Value: 0b – DC*CO is disallowed **[Default]** Value: 1b – DC*CO is allowed
	29	**Display DC*CO State Status** This bit indicates that the DMC DC*CO exit has completed and driver has to write a 0 to clear this bit. Value: 0b – **[Default]** Value: 1b – DMC DC*CO exit completed
	28	**DSI PLLs turn off disallowed** This bit indicates that when set, both the DSI PLLs will not be allowed to turnoff in the DC*CO state. Driver needs to set this bit if it does not want the DSI PLL to turn off in DC*CO states. Value: 0b – DSI PLLs turn off allowed **[Default]**

	1b	DSI PLLs turn off disallowed

27:24 Reserved

Access:	RO
Format:	MBZ

23:22 Reserved

Access:	RO
Format:	MBZ

21:20 Reserved

Access:	RO
Format:	MBZ

19:17 Reserved

Access:	RO
Format:	MBZ

16 Reserved

Access:	RO
Format:	MBZ

15:11 Reserved

Access:	RO
Format:	MBZ

10 Reserved

Access:	RO
Format:	MBZ

9 In CSR Flow

Value	Name
0b	Not In CSR
1b	In CSR

Restriction
This field is used for hardware communication. Software must not change this field.

8 Block Outbound Traffic

Access is read/write, but hardware can also clear the value based on the PM Request.

Value	Name
0b	Do Not Block
1b	Block

Restriction
This field is used for hardware communication. Software must not change this field.

DC_STATE_EN

	7:6	**Reserved** Access: RO Format: MBZ
	5	**Reserved** Access: RO Format: MBZ
	4	**Mask Poke** This field masks the poke signal that would otherwise be generated by a write to the DC_STATE_SEL register. Value: 0b – Unmask; 1b – Mask Restriction: This field is used for hardware communication. Software must not change this field.
	3	**DC9 Allow** This field indicates software allows Display C9. When allowed, the PCU can save the display PCI Config context and power down display Value: 0b – Do not allow; 1b – Allow
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Dynamic DC State Enable** This field enables hardware to dynamically enter and exit Display C states. Value: 00b – Disable; 01b – Enable up to DC5; 10b – Enable up to DC6 Restriction: The Display CSR code must be loaded before this field is enabled.

DCPR_STATUS_1

DCPR_STATUS_1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	46440h-46443h
Name:	DCPR Status 1
ShortName:	DCPR_STATUS_1
Reset:	global

This register indicates whether display is demoting Isoch requests.

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28	**Reserved**
	27	**Reserved**
	26	**Reserved** Access: RO Format: MBZ
	25:0	**Reserved** Access: RO Format: MBZ

DDI_AUX_CTL

DDI_AUX_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64310h-64313h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_USBC1
Reset:	soft
Address:	64410h-64413h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_USBC2
Reset:	soft
Address:	64510h-64513h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_USBC3
Reset:	soft
Address:	64610h-64613h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_USBC4
Reset:	soft
Address:	64710h-64713h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_USBC5
Reset:	soft
Address:	64810h-64813h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_USBC6
Reset:	soft
Address:	64010h-64013h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_A
Reset:	soft
Address:	64110h-64113h
Name:	DDI AUX Channel Control

DDI_AUX_CTL

ShortName:	DDI_AUX_CTL_B
Reset:	soft
Address:	64210h-64213h
Name:	DDI AUX Channel Control
ShortName:	DDI_AUX_CTL_C
Reset:	soft

DWord	Bit	Description
0	31	**Send Busy** Access: R/W Set Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes. **Programming Notes** Aux IO power must be enabled in PWR_WELL_CTL prior to starting an Aux transaction. **Restriction** Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes.
	30	**Done** Access: R/WC A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event 0b – Not done 1b – Done
	29	**Interrupt on Done** Access: R/W Enable an interrupt when the transaction completes or times out. 0b – Disable 1b – Enable
	28	**Time out error** Access: R/WC A sticky bit that indicates the transaction has timed out. Write a 1 to this bit to clear the event. 0b – Not error 1b – Error

DDI_AUX_CTL

27:26 Time out timer value

Access:	R/W

Used to determine how long to wait for receiver response before timing out.

Value	Name
01b	600us **[Default]**
10b	800us
11b	4000us

25 Receive error

Access:	R/WC

A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. Write a 1 to this bit to clear the event.

Value	Name
0b	Not Error
1b	Error

24:20 Message Size

Access:	Write/Read Status

The value written to this field indicates the total number bytes to transmit (including the header). The value read from this field indicates the number of bytes received, including the header, in the last transaction. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted.

Restriction
Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.

19:16 Reserved

Access:	RO
Format:	MBZ

15 Reserved

14 Reserved

13 Reserved

12 Reserved

11 IO Select

Access:	R/W

This field selects which IO will be used for the Aux transaction. It must not be switched while a transaction is in progress.

Value	Name	Description
1b	TBT	Use Thunderbolt IO
0b	Legacy	Use legacy IO. Either typeC or regular DDI, depending on project and SKU

DDI_AUX_CTL

	10	**Reserved** Access: RO Format: MBZ
	9:5	**Fast Wake Sync Pulse Count** Default Value: 1 0001b 18 pulses Access: R/W This field determines the total number of SYNC pulses sent during the SYNC phase of a fast wake transaction. The value programmed is the number of pulses minus 1. When this is field is set to "n" the aux controller will send "n+1" SYNC pulses before transmitting the STOP pattern. **SW must always program this field to the value of decimal 7.**
	4:0	**Sync Pulse Count** Default Value: 1 1111b 32 pulses Access: R/W This field determines the total number of SYNC pulses sent during the SYNC phase of a standard transaction. The value programmed is the number of pulses minus 1. When this is field is set to "n" the aux controller will send "n+1" SYNC pulses before transmitting the STOP pattern. **Restriction** This field must be programmed to at least 25 decimals to send the minimum amount of pulses required for a standard transaction.

DDI_AUX_DATA

DDI_AUX_DATA	
Register Space:	MMIO: 0/2/0
Access:	Write/Read Status
Size (in bits):	32
Address:	64314h-64317h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_USBC1
Reset:	soft
Address:	64318h-6431Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_USBC1
Reset:	soft
Address:	6431Ch-6431Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_USBC1
Reset:	soft
Address:	64320h-64323h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_USBC1
Reset:	soft
Address:	64324h-64327h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_USBC1
Reset:	soft
Address:	64414h-64417h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_USBC2
Reset:	soft
Address:	64418h-6441Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_USBC2
Reset:	soft
Address:	6441Ch-6441Fh
Name:	DDI AUX Channel Data 2

DDI_AUX_DATA	
ShortName:	DDI_AUX_DATA_2_USBC2
Reset:	soft
Address:	64420h-64423h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_USBC2
Reset:	soft
Address:	64424h-64427h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_USBC2
Reset:	soft
Address:	64514h-64517h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_USBC3
Reset:	soft
Address:	64518h-6451Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_USBC3
Reset:	soft
Address:	6451Ch-6451Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_USBC3
Reset:	soft
Address:	64520h-64523h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_USBC3
Reset:	soft
Address:	64524h-64527h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_USBC3
Reset:	soft
Address:	64614h-64617h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_USBC4
Reset:	soft
Address:	64618h-6461Bh
Name:	DDI AUX Channel Data 1

DDI_AUX_DATA	
ShortName:	DDI_AUX_DATA_1_USBC4
Reset:	soft
Address:	6461Ch-6461Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_USBC4
Reset:	soft
Address:	64620h-64623h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_USBC4
Reset:	soft
Address:	64624h-64627h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_USBC4
Reset:	soft
Address:	64714h-64717h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_USBC5
Reset:	soft
Address:	64718h-6471Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_USBC5
Reset:	soft
Address:	6471Ch-6471Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_USBC5
Reset:	soft
Address:	64720h-64723h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_USBC5
Reset:	soft
Address:	64724h-64727h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_USBC5
Reset:	soft
Address:	64814h-64817h
Name:	DDI AUX Channel Data 0

DDI_AUX_DATA	
ShortName:	DDI_AUX_DATA_0_USBC6
Reset:	soft
Address:	64818h-6481Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_USBC6
Reset:	soft
Address:	6481Ch-6481Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_USBC6
Reset:	soft
Address:	64820h-64823h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_USBC6
Reset:	soft
Address:	64824h-64827h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_USBC6
Reset:	soft
Address:	64014h-64017h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_A
Reset:	soft
Address:	64018h-6401Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_A
Reset:	soft
Address:	6401Ch-6401Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_A
Reset:	soft
Address:	64020h-64023h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_A
Reset:	soft
Address:	64024h-64027h
Name:	DDI AUX Channel Data 4

DDI_AUX_DATA	
ShortName:	DDI_AUX_DATA_4_A
Reset:	soft
Address:	64114h-64117h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_B
Reset:	soft
Address:	64118h-6411Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_B
Reset:	soft
Address:	6411Ch-6411Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_B
Reset:	soft
Address:	64120h-64123h
Name:	DDI AUX Channel Data 3
ShortName:	DDI_AUX_DATA_3_B
Reset:	soft
Address:	64124h-64127h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_B
Reset:	soft
Address:	64214h-64217h
Name:	DDI AUX Channel Data 0
ShortName:	DDI_AUX_DATA_0_C
Reset:	soft
Address:	64218h-6421Bh
Name:	DDI AUX Channel Data 1
ShortName:	DDI_AUX_DATA_1_C
Reset:	soft
Address:	6421Ch-6421Fh
Name:	DDI AUX Channel Data 2
ShortName:	DDI_AUX_DATA_2_C
Reset:	soft
Address:	64220h-64223h
Name:	DDI AUX Channel Data 3

DDI_AUX_DATA

ShortName:	DDI_AUX_DATA_3_C
Reset:	soft

Address:	64224h-64227h
Name:	DDI AUX Channel Data 4
ShortName:	DDI_AUX_DATA_4_C
Reset:	soft

There are 5 DWords of this register format per instance.

DWord	Bit	Description
0	31:0	**AUX CH DATA** This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted

DDI_BUF_CTL

DDI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64300h-64303h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_USBC1
Reset:	soft
Address:	64400h-64403h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_USBC2
Reset:	soft
Address:	64500h-64503h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_USBC3
Reset:	soft
Address:	64600h-64603h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_USBC4
Reset:	soft
Address:	64700h-64703h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_USBC5
Reset:	soft
Address:	64800h-64803h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_USBC6
Reset:	soft
Address:	64000h-64003h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_A
Reset:	soft
Address:	64100h-64103h
Name:	DDI Buffer Control

DDI_BUF_CTL

ShortName:	DDI_BUF_CTL_B
Reset:	soft

Address:	64200h-64203h
Name:	DDI Buffer Control
ShortName:	DDI_BUF_CTL_C
Reset:	soft

Do not read or write the register when the associated power well is disabled.

DWord	Bit	Description
0	31	**DDI Buffer Enable** This bit enables the DDI buffer. Value: 0b = Disable; 1b = Enable
	30	**Reserved** Access: RO Format: MBZ
	29	**Override Training Enable** This field enables the override on the training enable signal that tells the DDI I/O to pick up any DDI voltage swing and pre-emphasis changes. Value: 1b = Enable Override; 0b = Disable Override
	28	**Phy Param Adjust** Enables adjustment of Phy parameters such as voltage swing and pre emphasis outside Inik training process. This field is conditioned on "override training enable" (DDI_BUF_CTL[29]). Value: 1b = Enable; 0b = Disable
	27:24	**Reserved** Access: RO Format: MBZ
	23:18	**Reserved** Access: RO Format: MBZ

DDI_BUF_CTL

17 Reserved

Access:	RO
Format:	MBZ

16 Port Reversal

This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port.

Value	Name
0b	Not reversed
1b	Reversed

Programming Notes

Type-C/TBT dynamic connections:
The DDIs going to thunderbolt or USB-C DP alternate mode should not be reversed here. The reversal is taken care of in the FIA.
Static/fixed connections (DP/HDMI) through FIA:
In the case of static connections such as "No pin assignment (Non Type-C DP)", DDIs will use this lane reversal bit.
All other connections:
DDIs will use this lane reversal bit.

Restriction

This field must not be changed while the DDI is enabled.

15:8 USB Type-C DP Lane Staggering Delay

Specifies the number of symbol clocks delay used to stagger assertion/deassertion of the port lane enables. The target time recommended by circuit team is 100ns or greater. The delay should be programmed based on link clock frequency. This staggering delay is ONLY required when the port is used in USB Type C mode. Otherwise the default delay is zero which means no staggering. Example: 270MHz link clock = 1/270MHz = 3.7ns. (100ns/3.7ns)=27.02 symbols. Round up to 28.

7 DDI Idle Status

Access:	RO

This bit indicates when the DDI buffer is idle.

Value	Name
0b	Buffer Not Idle
1b	Buffer Idle

6 Reserved

Access:	RO
Format:	MBZ

5:4 Reserved

Access:	RO
Format:	MBZ

DDI_BUF_CTL

	3:1	**DP Port Width Selection** This bit selects the number of lanes to be enabled on the DDI link for DisplayPort.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode
Others	Reserved	Reserved

Restriction
When in DisplayPort mode the value selected here must match the value selected in TRANS_DDI_FUNC_CTL attached to this DDI.
This field must not be changed while the DDI is enabled.

	0	**Init Display Detected**

Access:	RO

Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection.

Value	Name	Description
0b	Not Detected	Digital display not detected during initialization
1b	Detected	Digital display detected during initialization

DDI_CLK_SEL

DDI_CLK_SEL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4610Ch-4610Fh
Name:	DDI USBC1 Clock Select
ShortName:	DDI_CLK_SEL_USBC1
Reset:	soft
Address:	46110h-46113h
Name:	DDI USBC2 Clock Select
ShortName:	DDI_CLK_SEL_USBC2
Reset:	soft
Address:	46114h-46117h
Name:	DDI USBC3 Clock Select
ShortName:	DDI_CLK_SEL_USBC3
Reset:	soft
Address:	46118h-4611Bh
Name:	DDI USBC4 Clock Select
ShortName:	DDI_CLK_SEL_USBC4
Reset:	soft
Address:	4611Ch-4611Fh
Name:	DDI USBC5 Clock Select
ShortName:	DDI_CLK_SEL_USBC5
Reset:	soft
Address:	46120h-46123h
Name:	DDI USBC6 Clock Select
ShortName:	DDI_CLK_SEL_USBC6
Reset:	soft

DWord	Bit	Description
0	31:28	**Clock Select** Select which clock to use for this DDI.

Value	Name	Description
0000b	None	Nothing selected. Clock is disabled for this DDI.
1000b	MG	Type-C PHY PLL output
1100b	TBT 162	Thunderbolt 162 MHz

		1101b	TBT 270	Thunderbolt 270 MHz
		1110b	TBT 540	Thunderbolt 540 MHz
		1111b	TBT 810	Thunderbolt 810 MHz

Restriction

This must not be changed while the DDI is enabled or any transcoder directed to the DDI is enabled.

27:0 **Reserved**

Access:	RO
Format:	MBZ

DE_FUSA_IOSF_PARITY_CNTRL

DE_FUSA_IOSF_PARITY_CNTRL - DE_FUSA_IOSF_PARITY_CNTRL

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100140h

This register controls the parity generation, checking, and error insertion logic in the DE IOSF end points : PSF 0 and PSF DIP

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**PSF DIP Cmd Parity Gen Dis** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 command parity generation is disabled
	28	**Reserved** Access: RO Format: MBZ
	27:26	**Reserved** Access: RO Format: MBZ
	25	**PSF DIP Cmd Parity Chk En** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 checking of command parity is enabled
	24	**PSF DIP Data Parity Chk En** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 checking of data parity is enabled

DE_FUSA_IOSF_PARITY_CNTRL - DE_FUSA_IOSF_PARITY_CNTRL

23	**Reserved** Access: RO Format: MBZ
22	**PSF DIP Cmd Parity Err Inj** Default Value: 0h Access: R/W _Custom_GTIReset: BUS 0: No error injection 1: Invert mcparity Once set the next command mcparity is corrupted and then the bit is cleared by HW.
21:20	**Reserved** Access: RO Format: MBZ
19:14	**Reserved** Access: RO Format: MBZ
13	**PSF 0 Cmd Parity Gen Dis** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 command parity generation is disabled
12	**PSF 0 Data Parity Gen Dis** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 data parity generation is disabled
11:10	**Reserved** Access: RO Format: MBZ
9	**PSF 0 Cmd Parity Chk En** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 checking of command parity is enabled

DE_FUSA_IOSF_PARITY_CNTRL - DE_FUSA_IOSF_PARITY_CNTRL

8	**PSF 0 Data Parity Chk En** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 checking of data parity is enabled
7	**Reserved** Access: RO Format: MBZ
6	**PSF 0 Cmd Parity Err Inj** Default Value: 0h Access: R/W _Custom_GTIReset: BUS 0: No error injection 1: Invert mcparity Once set the next command mcparityis corrupted and then the bit is cleared by HW.
5:4	**PSF 0 Data Parity Error Inj** Default Value: 0h Access: R/W _Custom_GTIReset: BUS 00: No error injected 01:Invert mdparity[0] 10:Invert mdparity[1] 11: Invert mdparity[1:0] Once set the next command with data is corrupted and then the bit is cleared by HW. Note: mdparity[1] is only present forIOSF data widths of 512
3:1	**Reserved** Access: RO Format: MBZ
0	**DE_FUSA_IOSF_PARITY_CNTRL_LOCK** Default Value: 000b _Custom_GTIReset: BUS Writing 1 to this bit will lock the register from further updates

DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	44400h-4440Fh
Name:	Display Engine Pipe A Interrupts
ShortName:	DE_PIPE_INTERRUPT_A
Reset:	soft
Address:	44410h-4441Fh
Name:	Display Engine Pipe B Interrupts
ShortName:	DE_PIPE_INTERRUPT_B
Reset:	soft
Address:	44420h-4442Fh
Name:	Display Engine Pipe C Interrupts
ShortName:	DE_PIPE_INTERRUPT_C
Reset:	soft
Address:	44430h-4443Fh
Name:	Display Engine Pipe D Interrupts
ShortName:	DE_PIPE_INTERRUPT_D
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers. The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the next level up interrupt registers. There is one full set of Display Engine Pipe interrupts per display pipe. The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.

0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C, 0x44430 = ISR D
0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C, 0x44434 = IMR D
0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C, 0x44438 = IIR D
0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C, 0x4443C = IER D

DWord	Bit	Description
0	31	**Underrun** Description: The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.
	30	**VRR Double Buffer Update** The ISR is an active high pulse on the eDP/DP Variable Refresh Rate double buffer update event on this pipe.
	29	**Reserved**

DE_PIPE_INTERRUPT

	28	**Reserved**
	27	**Isoch Ack** The ISR is an active high pulse when the IsocReq for this pipe receives an Ack.
	26	**PIPEDMC_Interrupt** The ISR is an active high pulse when the PIPE DMC has an interrupt.
	25	**PIPEDMC_gtt_fault_status** The ISR is an active high pulse when the PIPE DMC gtt fault occurs.
	24	**Unused_Int_24** These interrupts are currently unused.
	23	**LACE Fast Access Interrupt** The ISR is an active high level indicating an interrupt is set in DPLC_FA_STATUS.
	22	**Plane7_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 7 on this pipe.
	21	**Plane6_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 6 on this pipe.
	20	**Plane5_GTT_Fault_Status** Description The ISR is an active high pulse when a GTT fault is detected for plane 5 on this pipe.
	19	**Vblank unmodified** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe, the unmodified vertical blank, as opposed to the modified vertical blank that the pipe units use. The transcoder vertical blank always begins at the end of transcoder vertical active (unmodified). When the transcoder vertical blank start is programmed later than transcoder vertical active, the pipe vertical blank will start later than the transcoder vertical blank (modified).
	18	**Plane7_Flip_Done** The ISR is an active high pulse when the flip is done for plane 7 on this pipe.
	17	**Plane6_Flip_Done** The ISR is an active high pulse when the flip is done for plane 6 on this pipe.
	16	**Plane5_Flip_Done** The ISR is an active high pulse when the flip is done for plane 5 on this pipe.

DE_PIPE_INTERRUPT

	15	**DSB_2_Interrupt** The ISR is an active high pulse when there is interrupt from DSB 2. SW must read the DSB interrupt registers to check what is caused interrupt in DSB.
	14	**DSB_1_Interrupt** The ISR is an active high pulse when there is interrupt from DSB 1. SW must read the DSB interrupt registers to check what is caused interrupt in DSB..
	13	**DSB_0_Interrupt** The ISR is an active high pulse when there is interrupt from DSB 0. SW must read the DSB interrupt registers to check what is caused interrupt in DSB..
	12	**DPST_Histogram_event** The ISR is an active high pulse on the DPST Histogram event on this pipe.
	11	**Cursor_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.
	10	**Plane4_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe.
	9	**Plane3_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe.
	8	**Plane2_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 2 on this pipe.
	7	**Plane1_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 1 on this pipe.
	6	**Plane4_Flip_Done** The ISR is an active high pulse when the flip is done for plane 4 on this pipe.
	5	**Plane3_Flip_Done** The ISR is an active high pulse when the flip is done for plane 3 on this pipe.
	4	**Plane2_Flip_Done** The ISR is an active high pulse when the flip is done for plane 2 on this pipe.
	3	**Plane1_Flip_Done** The ISR is an active high pulse when the flip is done for plane 1 on this pipe.
	2	**Scan_Line_Event** The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe.

DE_PIPE_INTERRUPT		
	1	**Vsync** The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe.
	0	**Vblank** **Description** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe. This represents the vertical blank observed by units within the pipe and used for updating double-buffered registers in the pipe. The transcoder vertical blank always begins at the end of transcoder vertical active (unmodified). When the transcoder vertical blank start is programmed later than transcoder vertical active, the pipe vertical blank will start later than the transcoder vertical blank (modified).

DE_POWER1

DE_POWER1	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	42400h-42403h
Name:	Display Engine Power 1
ShortName:	DE_POWER1
Reset:	global

DWord	Bit	Description
0	31	**Power Well 2 State** This field indicates the status of display power well 2. Value: 0b = Off; 1b = On
	30	**Display Pipes Enabled** This field indicates if any display pipes are enabled. Value: 0b = Disabled (All display pipes disabled); 1b = Enabled (One or more display pipes enabled)
	29	**Reserved** Access: RO Format: MBZ
	28	**Power Well 1 State** This field indicates the status of display power well 1. Value: 0b = Off; 1b = On
	27:26	**SRD Status** This field indicates the live status of the SRD link on transcoder A. Value: 00b = Full Off (Link is fully off. DDI lanes are disabled and most memory reads are disabled.); 01b = Full On (Link is fully on. Normal operation.); 11b = Reserved (Reserved)
	25	**KVM Session Status** This field indicates the status of KVM session.

DE_POWER1

Value	Name	Description
0b	Disabled	KVM session disabled
1b	Enabled	KVM session enabled

24:20	**Transmit Lanes Enabled** The total number of DDI lanes enabled.
19:14	**Reserved** Access: RO Format: MBZ
13:10	**Enabled Pipe Scalers** Indicates total usage of the Scaler EBBs.
9:8	**Enabled DEPLLs** The total number of display CCU PLLs enabled.
7	**Reserved** Access: RO Format: MBZ
6:4	**Reserved** Access: RO Format: MBZ
3	**Enabled CDPLLs** Indicates if CD PLL is enabled.
2:0	**Enabled MGPLLs** The total number of type-C PLLs enabled by display.

DE_POWER2

DE_POWER2	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	42404h-42407h
Name:	Display Engine Power 2
ShortName:	DE_POWER2
Reset:	global

DWord	Bit	Description
0	31:0	**DE bandwidth counter** This counter increments on every cache line put arriving at the DE. The bandwidth is estimated by taking the difference between two reads at a known interval. Access is actually a read/write variant. Writes to this register will load the write data into the counter. **Restriction** This register will measure the memory Bandwidth of the Low Priority channel to memory. It is associated with ABOX. It does not measure BW associated with ABOX1 or ABOX2.

DE_RR_DEST

DE_RR_DEST

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44058h-4405Bh
Name:	Render Response Destination
ShortName:	DE_RR_DEST
Reset:	soft

This register selects the destination of certain render responses that may go to CS, BCS, or both. In order for a response to be sent to a particular destination, the event most occur, the event must be unmasked, and that destination must be selected.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:6	**Pipe D Vertical Blank Destination** This field selects the destination for the render response sent on pipe D start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS
	5:4	**Pipe C Vertical Blank Destination** This field selects the destination for the render response sent on pipe C start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS
	3:2	**Pipe B Vertical Blank Destination** This field selects the destination for the render response sent on pipe B start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS

<table>
<tr><th colspan="3">DE_RR_DEST</th></tr>
<tr><td></td><td>1:0</td><td>Pipe A Vertical Blank Destination
This field selects the destination for the render response sent on pipe A start of vertical blank.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>CS</td></tr><tr><td>01b</td><td>BCS</td></tr><tr><td>10b,11b</td><td>Both CS and BCS</td></tr></table></td></tr>
</table>

DE_RRMR

DE_RRMR	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44050h-44053h
Name:	Render Response Mask
ShortName:	DE_RRMR
Reset:	soft

This register contains a bit mask which selects which events cause and are reported in the render response message.
See the render response message definition table to find the source event for each bit.
The render response message is sent from the display engine to the render command streamer (CS) or blitter command streamer (BCS). The message is used to inform CS and BCS of certain display events.
This register is used to control which render response message bits are masked or unmasked.
Unmasked bits will cause a render response message to be sent and will be reported in that message.
Masked bits will not be reported and will not cause a render response message to be sent.
Vertical blank events occur periodically while the associated display pipe timing generator is running and will be reported in a render response to CS or BCS (depending on DE_RR_DEST destination selection) if un-masked here.
Scanline events occur after they have been initiated through MMIO writes or LRI to the Display Load Scan Lines register. A scanline done event will be reported in a render response to CS if un-masked here and the Display Load Scanline source is CS. A scanline done event will be reported in a render response to BCS if un-masked here and the Display Load Scanline source is BCS.
Flip done events occur after they have been initiated through MI_DISPLAY_FLIP or MMIO write to plane surface address registers. A flip event will be reported in a render response to CS if un-masked here and the flip source is CS. A flip event will be reported in a render response to BCS if un-masked here and the flip source is BCS.

This register defines the DWord 0 of the render response bit mask. DWord 1and DWord 2 are defined inDE_RRMR_DW1 and DE_RRMR_DW2 registers.

Programming Notes

Programming this register can be done through MMIO or a command streamer LOAD_REGISTER_IMMEDIATE (LRI) command.
When using LRI, care must be taken to follow all the programming rules for LRI targeting the display engine.
Unmasked events will wake GT as they occur, so for improved power savings it is recommended to only unmask events while they are required.

Restriction

Events must be unmasked prior to waiting for them with a MI_WAIT_FOR_EVENT ring command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline.

DWord	Bit	Description
0	31	**Mask 31**

DE_RRMR

		Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	30	**Mask 30** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	29	**Mask 29** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	28	**Mask 28** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	27	**Mask 27** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	26	**Mask 26** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	25	**Mask 25** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	24	**Mask 24** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	23	**Mask 23** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR

	22	**Mask 22** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	21	**Mask 21** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	20	**Mask 20** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	19	**Mask 19** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	18	**Mask 18** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	17	**Mask 17** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	16	**Mask 16** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	15	**Mask 15** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	14	**Mask 14** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**

DE_RRMR

	13	**Mask 13** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	12	**Mask 12** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	11	**Mask 11** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	10	**Mask 10** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	9	**Mask 9** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	8	**Mask 8** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	7	**Mask 7** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	6	**Mask 6** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	5	**Mask 5** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**

DE_RRMR

	4	**Mask 4** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	3	**Mask 3** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	2	**Mask 2** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	1	**Mask 1** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	0	**Mask 0** Value: 0b — Not Masked Value: 1b — Masked **[Default]**

DE_RRMR_DW1

DE_RRMR_DW1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44048h-4404Bh
Name:	Render Response Mask DW 1
ShortName:	DE_RRMR_DW1
Reset:	soft

This register contains the Dword 1 of the CS/BCS render response bit mask. For more details refer to DE_RRMR.

DWord	Bit	Description
0	31	**Mask 31** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	30	**Mask 30** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	29	**Mask 29** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	28	**Mask 28** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	27	**Mask 27** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	26	**Mask 26** Value: 0b – Not Masked Value: 1b – Masked **[Default]**

DE_RRMR_DW1

	25	**Mask 25** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	24	**Mask 24** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	23	**Mask 23** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	22	**Mask 22** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	21	**Mask 21** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	20	**Mask 20** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	19	**Mask 19** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	18	**Mask 18** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	17	**Mask 17** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR_DW1

	16	**Mask 16** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	15	**Mask 15** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	14	**Mask 14** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	13	**Mask 13** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	12	**Mask 12** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	11	**Mask 11** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	10	**Mask 10** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	9	**Mask 9** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	8	**Mask 8** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR_DW1

	7	**Mask 7** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	6	**Mask 6** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	5	**Mask 5** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	4	**Mask 4** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	3	**Mask 3** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	2	**Mask 2** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	1	**Mask 1** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	0	**Mask 0** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR_DW2

DE_RRMR_DW2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4404Ch-4404Fh
Name:	Render Response Mask DW 2
ShortName:	DE_RRMR_DW2
Reset:	soft

This register contains the DWord 2 of the CS/BCS render response bit mask. For more details refer to DE_RRMR.

DWord	Bit	Description
0	31	**Mask 31** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	30	**Mask 30** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	29	**Mask 29** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	28	**Mask 28** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	27	**Mask 27** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	26	**Mask 26** Value: 0b – Not Masked Value: 1b – Masked **[Default]**

DE_RRMR_DW2

	25	**Mask 25** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	24	**Mask 24** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	23	**Mask 23** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	22	**Mask 22** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	21	**Mask 21** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	20	**Mask 20** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	19	**Mask 19** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	18	**Mask 18** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	17	**Mask 17** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR_DW2

	16	**Mask 16** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	15	**Mask 15** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	14	**Mask 14** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	13	**Mask 13** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	12	**Mask 12** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	11	**Mask 11** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	10	**Mask 10** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	9	**Mask 9** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	8	**Mask 8** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR_DW2

	7	**Mask 7** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	6	**Mask 6** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	5	**Mask 5** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	4	**Mask 4** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	3	**Mask 3** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	2	**Mask 2** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	1	**Mask 1** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	0	**Mask 0** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

Decouple Register 0 DW0

DECOUPREG0DW0 - Decouple Register 0 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F00h-00F03h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg0DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 0 DW0 Data.

Decouple Register 0 DW1

DECOUPREG0DW1 - Decouple Register 0 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F04h-00F07h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 1 DW0

DECOUPREG1DW0 - Decouple Register 1 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F08h-00F0Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg1DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 1 DW0 Data.

Decouple Register 1 DW1

DECOUPREG1DW1 - Decouple Register 1 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F0Ch-00F0Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 2 DW0

DECOUPREG2DW0 - Decouple Register 2 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F10h-00F13h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg2DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 2 DW0 Data.

Decouple Register 2 DW1

DECOUPREG2DW1 - Decouple Register 2 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F14h-00F17h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 3 DW0

DECOUPREG3DW0 - Decouple Register 3 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F18h-00F1Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg3DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 3 DW0 Data.

Decouple Register 3 DW1

DECOUPREG3DW1 - Decouple Register 3 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F1Ch-00F1Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 4 DW0

DECOUPREG4DW0 - Decouple Register 4 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F20h-00F23h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg4DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 4 DW0 Data. DCR requests on the NP path will be blocked during CPD

Decouple Register 4 DW1

DECOUPREG4DW1 - Decouple Register 4 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F24h-00F27h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 5 DW0

DECOUPREG5DW0 - Decouple Register 5 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F28h-00F2Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg5DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 5 DW0 Data.

Decouple Register 5 DW1

DECOUPREG5DW1 - Decouple Register 5 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F2Ch-00F2Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 6 DW0

DECOUPREG6DW0 - Decouple Register 6 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F30h-00F33h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg6DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 6 DW0 Data.

Decouple Register 6 DW1

DECOUPREG6DW1 - Decouple Register 6 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F34h-00F37h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 7 DW0

DECOUPREG7DW0 - Decouple Register 7 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F38h-00F3Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg7DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 7 DW0 Data.

Decouple Register 7 DW1

DECOUPREG7DW1 - Decouple Register 7 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F3Ch-00F3Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 8 DW0

DECOUPREG8DW0 - Decouple Register 8 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F40h-00F43h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg8DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 8 DW0 Data.

Decouple Register 8 DW1

DECOUPREG8DW1 - Decouple Register 8 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F44h-00F47h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 9 DW0

DECOUPREG9DW0 - Decouple Register 9 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F48h-00F4Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg9DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 9 DW0 Data.

Decouple Register 9 DW1

DECOUPREG9DW1 - Decouple Register 9 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F4Ch-00F4Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 10 DW0

DECOUPREG10DW0 - Decouple Register 10 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F50h-00F53h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg10DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 10 DW0 Data.

Decouple Register 10 DW1

DECOUPREG10DW1 - Decouple Register 10 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F54h-00F57h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 11 DW0

DECOUPREG11DW0 - Decouple Register 11 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F58h-00F5Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg11DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 11 DW0 Data.

Decouple Register 11 DW1

DECOUPREG11DW1 - Decouple Register 11 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F5Ch-00F5Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 12 DW0

DECOUPREG12DW0 - Decouple Register 12 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F60h-00F63h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg12DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 12 DW0 Data.

Decouple Register 12 DW1

DECOUPREG12DW1 - Decouple Register 12 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F64h-00F67h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 13 DW0

DECOUPREG13DW0 - Decouple Register 13 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F68h-00F6Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg13DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 13 DW0 Data.

Decouple Register 13 DW1

DECOUPREG13DW1 - Decouple Register 13 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F6Ch-00F6Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 14 DW0

DECOUPREG14DW0 - Decouple Register 14 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F70h-00F73h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg14DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 14 DW0 Data.

Decouple Register 14 DW1

DECOUPREG14DW1 - Decouple Register 14 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F74h-00F77h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 15 DW0

DECOUPREG15DW0 - Decouple Register 15 DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00F78h-00F7Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg15DW0Data** Access: R/W _Custom_GTIReset: BUS Decouple Register 15 DW0 Data.

Decouple Register 15 DW1

DECOUPREG15DW1 - Decouple Register 15 DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00F7Ch-00F7Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Dedicated Path Arbiter Credits

DEDICATED_PATH_ARB_CREDITS - Dedicated Path Arbiter Credits

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100180h

This register holds the credits for arbitrating between different ABOXs for streaming HP traffic to the dedicated memory path

DWord	Bit	Description
0	31:15	**Spare_0** Default Value: 0000h Access: R/W _Custom_GTIReset: BUS Spare bits
	14:8	**ABOX1 Credits** Default Value: 00h Access: R/W _Custom_GTIReset: BUS Number of Credits for ABOX1
	7	**Spare_1** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Spare bit
	6:0	**ABOX0 Credits** Default Value: 00h Access: R/W _Custom_GTIReset: BUS Number of Credits for ABOX0

DE HPD Interrupt Definition

DE HPD Interrupt Definition	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	44470h-4447Fh
Name:	Display Engine HPD Interrupts
ShortName:	DE_HPD_INTERRUPT
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine HPD Interrupt registers.
0x44470 = ISR
0x44474 = IMR
0x44478 = IIR
0x4447C = IER
The HPD bits use a modified interrupt structure where the live value goes to the ISR and a processed event goes to the IMR and IIR path.

DWord	Bit	Description
0	31	**Unused 31**
	30	**Unused 30**
	29	**Unused 29**
	28	**Unused 28**
	27	**Unused 27**
	26	**Unused 26**
	25	**Unused 25**
	24	**Unused 24**
	23	**TC8 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	22	**TC7 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	21	**TC6 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	20	**TC5 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	19	**TC4 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.

DE HPD Interrupt Definition		
	18	**TC3 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	17	**TC2 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	16	**TC1 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	15	**Unused 15**
	14	**Unused 14**
	13	**Unused 13**
	12	**Unused 12**
	11	**Unused 11**
	10	**Unused 10**
	9	**Unused 9**
	8	**Unused 8**
	7	**TBT8 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	6	**TBT7 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	5	**TBT6 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	4	**TBT5 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	3	**TBT4 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	2	**TBT3 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.

DE HPD Interrupt Definition		
	1	**TBT2 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	0	**TBT1 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.

DE Misc Interrupt Definition

DE Misc Interrupt Definition

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	44460h-4446Fh
Name:	Display Engine Miscellaneous Interrupts
ShortName:	DE_MISC_INTERRUPT
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Miscellaneous Interrupt registers.
0x44460 = ISR
0x44464 = IMR
0x44468 = IIR
0x4446C = IER

DWord	Bit	Description
0	31	**Poison** The ISR is an active high pulse on receiving the poison response to a memory transaction.
	30	**ECC_Double_Error** The ISR is an active high level while any of the ECC Double Error status bits are set.
	29	**Reserved** Access: RO Format: MBZ
	28	**Isoch_msg_error** The ISR is an active high pulse on the Isoch messages error.
	27	**Isoch_rsptimeout_error** The ISR is an active high pulse on the Isoch response timeout error.
	26	**Reserved** Access: RO Format: MBZ
	25	**Reserved**
	24	**Reserved**
	23	**WD0_Interrupts_Combined** The ISR is an active high level while any of the WD0_IIR bits are set.
	22:20	**Reserved** Access: RO Format: MBZ

DE Misc Interrupt Definition

	19	**SRD_Interrupts_Combined** The ISR is an active high level while any of the SRD_IIR bits are set.
	18	**WD1_Interrupts_Combined** The ISR is an active high level while any of the WD1_IIR bits are set.
	17:16	**Reserved** Access: RO Format: MBZ
	15	**GTC_Interrupts_Combined** The ISR is an active high level while any of the GTC_IIR bits are set.
	14:8	**Reserved** Access: RO Format: MBZ
	7	**Reserved**
	6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3	**NonPipe Isoch Ack** The ISR is an active high pulse when the Non-Pipe IsocReq receives an Ack.
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Reserved** Access: RO Format: MBZ

DE Port Interrupt Definition

DE Port Interrupt Definition

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	44440h-4444Fh
Name:	Display Engine Port Interrupts
ShortName:	DE_PORT_INTERRUPT
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers.
0x44440 = ISR
0x44444 = IMR
0x44448 = IIR
0x4444C = IER

DWord	Bit	Description
0	31	**DSI1** The ISR is an active high level indicating a non-TE interrupt is set in DSI_INTER_IDENT_REG_1.
	30	**DSI0** The ISR is an active high level indicating a non-TE interrupt is set in DSI_INTER_IDENT_REG_0.
	29:25	**Reserved** Access: RO Format: MBZ
	24	**DSI1 TE** The ISR is an active high level indicating a TE interrupt is set in DSI_INTER_IDENT_REG_1.
	23	**DSI0 TE** The ISR is an active high level indicating a TE interrupt is set in DSI_INTER_IDENT_REG_0.
	22:21	**Reserved** Access: RO Format: MBZ
	20:14	**Reserved** Access: RO Format: MBZ
	13	**AUX USBC6** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.

DE Port Interrupt Definition

	12	**AUX USBC5** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	11	**AUX USBC4** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	10	**AUX USBC3** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	9	**AUX USBC2** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	8	**AUX USBC1** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	7:3	**Reserved** Access: RO Format: MBZ
	2	**AUX DDIC** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	1	**AUX DDIB** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.
	0	**AUX DDIA** The ISR is an active high pulse on the AUX done event. This event will not occur for HW triggered AUX transactions.

Device 2 Control

DEV2CTL_0_2_0_PCI - Device 2 Control			
Register Space:	PCI: 0/2/0		
Size (in bits):	8		
Address:	00058h		
This register implements a control bit to disable and hide the IOBAR register in systems that do not require legacy IOBAR access to Gfx MMIO registers.			
DWord	**Bit**	**Description**	
0	7:1	**Reserved**	
		Access:	RO
		Format:	MBZ
	0	**Reserved**	

Device Capabilities

DEVICECAP_0_2_0_PCI - Device Capabilities

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00074h

PCI Express Device Capabilities

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**Functional Level Reset Capability** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
	27:26	**Captured Slot Power Limit Scale** Default Value: 00b Access: RO _Custom_GTIReset: BUS Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b
	25:18	**Captured Slot Power Limit Value** Default Value: 00000000h Access: RO _Custom_GTIReset: BUS Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h
	17:16	**Reserved** Access: RO Format: MBZ
	15	**Role-Based Error Reporting** Default Value: 1b Access: RO _Custom_GTIReset: BUS When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated

DEVICECAP_0_2_0_PCI - Device Capabilities

		into PCI Express Base Specification, Revision 1.1.Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
	14:12	**Reserved** Access: RO Format: MBZ
	11:9	**Endpoint L1 Acceptable Latency** Default Value: 000b Access: RO _Custom_GTIReset: BUS This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state. This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 1 us).
	8:6	**Endpoint L0s Acceptable Latency** Default Value: 000b Access: RO _Custom_GTIReset: BUS This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state. This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 64 ns).
	5	**Extended Tag Field Supported** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit indicates the maximum supported size of the Tag field as a Requester.This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).
	4:3	**Phantom Functions Supported** Default Value: 00b Access: RO _Custom_GTIReset: BUS This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices.This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.

DEVICECAP_0_2_0_PCI - Device Capabilities

	2:0	**Max Payload Size Supported** Default Value: 000b Access: RO _Custom_GTIReset: BUS This field indicates the maximum payload size that the Function can support for TLPs. Hardwired to 000b to represents 128 bytes, the minimum allowed value.

Device Enable

DEVEN_0_0_0_PCI - Device Enable

Register Space: PCI: 0/0/0
Size (in bits): 32

Address: 00054h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package.

DWord	Bit	Description
0	31:15	**Reserved** Access: RO Format: MBZ
	14	**Chap Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	13	**Device 6 Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	12:11	**Reserved** Access: RO Format: MBZ
	10	**Device 5 Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	9:8	**Reserved** Access: RO Format: MBZ

DEVEN_0_0_0_PCI - Device Enable

	7	**Device 4 Enable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	6	**Reserved** Access: RO Format: MBZ
	5	**Device 3 enable for Display HD Audio** Default Value: 1b Access: R/W _Custom_GTIReset: BUS
	4	**Internal Graphics Engine** Default Value: 1b Access: R/W _Custom_GTIReset: BUS 0: Bus 0 Device 2 is disabled and hidden1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
	3	**PEG10 Enable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	2	**PEG11 Enable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	1	**PEG12 Enable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS

DEVEN_0_0_0_PCI - Device Enable		
	0	**Host Bridge** Default Value: 1b Access: RO _Custom_GTIReset: BUS

Device Identification

DID2_0_2_0_PCI - Device Identification

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00002h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

DWord	Bit	Description
0	15:7	**Device Identification Number MSB** Default Value: 100110100b Access: R/W Variant _Custom_GTIReset: BUS All 16 bits of Device ID is acquired through fuse pull as per Chassis 2.1 updates.
	6:0	**Device Identification Number SKU** Default Value: 1000000b Access: RO Variant _Custom_GTIReset: BUS All 16 bits of Device ID is acquired through fuse pull as per Chassis 2.1 updates.

DFSDONE

DFSDONE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	51080h-51083h
Name:	Display Fuse Done
ShortName:	DFSDONE
Reset:	global

This register is not reset by FLR.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Download Done** This field indicates when fuse download is complete. 0b – Note Done 1b – Done

DFSM

DFSM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	51000h-51003h
Name:	Display Fuse
ShortName:	DFSM
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31	**Reserved**
	30	**Display PipeA Disable** This bit indicates whether the display pipe A (first pipe) capability is disabled. Value / Name / Description: 0b / Enable / Pipe A Capability Enabled 1b / Disable / Pipe A Capability Disabled
	29	**Reserved**
	28	**Display PipeC Disable** This bit indicates whether the display pipe C (third pipe) capability is disabled. Value / Name / Description: 0b / Enable / Pipe C Capability Enabled 1b / Disable / Pipe C Capability Disabled
	27	**Display PM Disable** This bit indicates whether the display power management FBC and DPST capabilities are disabled. Value / Name / Description: 0b / Enable / PM Capability Enabled 1b / Disable / PM Capability Disabled
	26	**Display eDP Disable** Description: This fuse indicates that all combo PHY ports are disabled by the SoC and cannot be used. Value / Name / Description: 0b / Enable / eDP Capability Enabled 1b / Disable / eDP Capability Disabled
	25	**Reserved**
	24	**Reserved**

23	**Reserved**
22	**Display PipeD Disable** This bit indicates whether the display pipe D (fourth pipe) capability is disabled. **Value** / **Name** 0b – Enable 1b – Disable
21	**Display PipeB Disable** This bit indicates whether the display pipe B (second pipe) capability is disabled. **Value** / **Name** 0b – Pipe B Capability Enabled 1b – Pipe B Capability Disabled
20	**Display WD Disable** This bit indicates whether the display WD capability is disabled. **Value** / **Name** / **Description** 0b – Enable – WD Capability Enabled 1b – Disable – WD Capability Disabled
19	**Reserved**
18	**Reserved**
17	**Reserved**
16	**Isolated Decode Disable** This field indicates whether the Isolated Decode feature is disabled. **Value** / **Name** 0b – Isolated Decode Capability Enabled 1b – Isolated Decode Capability Disabled
15:8	**Audio Codec ID** This field indicates the lower 8 bits of the audio codec device ID. See the root node F00 verb for the device IDs on each project. **Value** / **Name** / **Description** 0Bh – Audio Codec ID 280Bh **[Default]** – Default value is N/A. Fuse download will override with correct value for this project.
7	**Display DSC Disable** This field indicates whether the DSC (port Display Stream Compression) feature is disabled. **Value** / **Name** 0b – DSC Capability Enabled 1b – DSC Capability Disabled
6	**Display RSB Enable** This bit indicates whether the remote screen blanking feature is enabled in the display engine.

DFSM

		Value / **Name** / **Description** 0b / Disable / RSB Capability Disabled 1b / Enable / RSB Capability Enabled
	5	**Reserved**
	4	**Reserved**
	3	**Reserved**
	2	**Reserved**
	1	**Reserved**
	0	**Display Audio Codec Disable** This bit indicates whether the display audio codec capability is disabled. **Value** / **Name** / **Description** 0b / Enable / Audio Codec Capability Enabled 1b / Disable / Audio Codec Capability Disabled

DG_CLKREQ_POLICY

DG_CLKREQ_POLICY - DG_CLKREQ_POLICY

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	101038h

Various bits that control clock req functionality in DG. This register should be programmed as part of graphics initialization.

DWord	Bit	Description
0	31:24	**SPARE2** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS Reserved
	23:16	**CLKREQ_HYST_CNTR** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS Register to store the parameter used to counting IDLE cycles during Hysteris state. Deassert clkreq when DG is idle for the number of cycles this register is programmed to.
	15:2	**SPARE1** Default Value: 00000000000000b Access: R/W _Custom_GTIReset: BUS Reserved
	1	**Reserved**
	0	**Reserved**

Discard counter status register

L3DISCARDCNTR - Discard counter status register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B130h	
DWord	**Bit**	**Description**
0	31:16	**Discard Counter** Counter indicating Total evictions (in multiple of 64 events) dropped due to discard mechanism
	15:0	**C/Z Active Tile Eviction Counter** Counter indicating total number of eviction (in multiple of 64 events) from C/Z (or unified tile cache) ways when the tile it belongs to is active

Discard Enables for Z streams

Z_DISCARD_EN - Discard Enables for Z streams

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	07040h
ShortName:	Z_DISCARD_EN

Under Posh Based Tiled Rendering (aka PTBR), at the end of tile, certain streams can be discarded from the on-chip caches i.e. without evicting to memory. SW programs LOAD_REG_MEMORY command in the RCS command buffer to program this register. HW uses this value live from the register
This register defines the discard bits for Z streams.
Setting the discard enable bit for a stream, allows HW to drop writing back dirty cachelines from on-chip caches to memory.

Programming Notes

This register value must not change during the render pass (aka tile pass).

DWord	Bit	Description
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**STC Discard Enable** When this bit is set, Stencil (STC) stream can be discarded at the end of tile in the PTBR mode. 0 – Disable **[Default]** 1 – Enable
	0	**Z Discard Enable** Access: R/W **Description** When this bit is set, all Z streams i.e. HiZ and Z can be discarded at the end of tile in the PTBR mode. 0 – Disable **[Default]** 1 – Enable

DISMBASE_LSB

DISMBASE_LSB - DISMBASE_LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	108410h	
32 bit register that defines LSB of Display Stolen Memory base.		
DWord	**Bit**	**Description**
0	31:24	**DISM_BASE_LSB** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS
	23:0	**Reserved** Access: RO Format: MBZ

DISMBASE_MSB

DISMBASE_MSB - DISMBASE_MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	108414h	
32 bit register that defines MSB of Display Stolen memory base.		
DWord	**Bit**	**Description**
0	31:0	**DISM_BASE_MSB** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS

DISMLIMIT_LSB

DISMLIMIT_LSB - DISMLIMIT_LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	108418h	
32 bit register that defines LSB of Display Stolen Memory limit.		
DWord	**Bit**	**Description**
0	31:24	**DISM_LIMIT_LSB** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS
	23:0	**Reserved** Access: RO Format: MBZ

DISMLIMIT_MSB

DISMLIMIT_MSB - DISMLIMIT_MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	10841Ch	
32 bit register that defines MSB of Display Stolen Memory limit.		
DWord	**Bit**	**Description**
0	31:0	**DISM_LIMIT_MSB** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS

DISPLAY_INT_CTL

DISPLAY_INT_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	44200h-44203h
Name:	Display Interrupt Control
ShortName:	DISPLAY_INT_CTL
Reset:	soft

This register has the primary enable for display interrupts and gives an overview of what interrupts are pending. An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER). All Pending Interrupts are ORed together to generate the combined interrupt.
The combined interrupt is ANDed with the Display Interrupt enable to create the display enabled interrupt.
The display enabled interrupt goes to graphics interrupt processing.

DWord	Bit	Description
0	31	**Display Interrupt Enable** Access: R/W This is the ultimate control for display interrupts. This must be enabled for any of these interrupts to propagate to graphics interrupt processing. 0b: Disable 1b: Enable
	30:26	**Reserved** Access: RO Format: MBZ
	25	**Direct PICA Interrupts Pending** Access: RO This field indicates if PICA interrupts are pending. This is use on SoCs that connect the PICA interrupt to North DE. Other SoCs connect the PICA interrupt to south DE because of partitioning and power domains. The PICA interrupt is configured through the PICA interrupt registers.
	24	**Audio Codec Interrupts Pending** Access: RO This field indicates if audio codec interrupts are pending.
	23	**DE PCH Interrupts Pending** Access: RO This field indicates if South (PCH) display interrupts are pending. The South Display interrupt is configured through the SDE interrupt registers.

DISPLAY_INT_CTL		
	22	**DE Misc Interrupts Pending** Access: RO This field indicates if DE Misc interrupts are pending.
	21	**DE HPD Interrupts Pending** Access: RO This field indicates if North DE HPD interrupts are pending.
	20	**DE Port Interrupts Pending** Access: RO This field indicates if Port interrupts are pending.
	19	**DE Pipe D Interrupts Pending** Access: RO This field indicates if Pipe D interrupts are pending.
	18	**DE Pipe C Interrupts Pending** Access: RO This field indicates if Pipe C interrupts are pending.
	17	**DE Pipe B Interrupts Pending** Access: RO This field indicates if Pipe B interrupts are pending.
	16	**DE Pipe A Interrupts Pending** Access: RO This field indicates if Pipe A interrupts are pending.
	15:0	**Reserved** Access: RO Format: MBZ

DKL_BIAS

DKL_BIAS	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B3Ch-168B3Fh
Name:	DKL_BIAS_NULL
ShortName:	DKL_BIAS_NULL
Reset:	global

This register is not reset by the device 2 FLR.
This register is associated with the display PLL instance (PLL1).

DWord	Bit	Description
0	31	**i_tdc_fine_res** Default Value: 1b TDC fine resolution select 0: Coarse resolution / 8 1: Coarse resolution / 4
	30	**i_fracnen_h** Default Value: 1b Enables fractional modulator. For SSC, this bit needs to be set to '1', even though it starts with integer division ratio.
	29:24	**i_fbdiv_frac_21_16** Default Value: 1Eh Fractional modulator settings.
	23:16	**i_fbdiv_frac_15_8** Default Value: 00h Fractional modulator settings.
	15:8	**i_fbdiv_frac_7_0** Default Value: 00h Fractional modulator settings.
	7:0	**i_sscinj_stepsize_7_0** Default Value: 00h SSC injection step size.

DKL_CLKTOP2_CORECLKCTL1

DKL_CLKTOP2_CORECLKCTL1 - DKL_CLKTOP2_CORECLKCTL1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B34h-168B37h
Name:	DKL_CLKTOP2_CORECLKCTL1_NULL
ShortName:	DKL_CLKTOP2_CORECLKCTL1_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**od_clktop2_coreclkd_bypass** bypass enable of coreclkd to take input refclk.
	28	**od_clktop2_coreclkd_divretimeren_h** Default Value: 1b retimer enable: 0 for odd division ratio, 1 for even division ratio
	27	**Reserved** Access: RO Format: MBZ
	26	**od_clktop2_coreclkc_bypass** bypass enable of coreclkc to take input refclk
	25	**od_clktop2_coreclkc_divretimeren_h** retimer enable: 0 for odd division ratio, 1 for even division ratio
	24	**Reserved** Access: RO Format: MBZ
	23:16	**od_clktop2_coreclkb_divratio** Default Value: 8h divider ratio for coreclkb divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255 8'h08: PCIe4/PCIE3
	15:8	**od_clktop2_coreclka_divratio** Default Value: 5h divider ratio for coreclka divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255 8'h05: HBR3/HBR2 8'h0A: HBR/RBR

DKL_CLKTOP2_CORECLKCTL1 - DKL_CLKTOP2_CORECLKCTL1		
	7:6	**Reserved** Access: RO Format: MBZ
	5	**od_clktop2_coreclkb_bypass** bypass enable of coreclkb to take input refclk
	4	**od_clktop2_coreclkb_divretimeren_h** Default Value: 1b retimer enable: 0 for odd division ratio, 1 for even division ratio
	3	**Reserved** Access: RO Format: MBZ
	2	**od_clktop2_coreclka_bypass** bypass enable of coreclka to take input refclk
	1	**od_clktop2_coreclka_divretimeren_h** retimer enable: 0 for odd division ratio, 1 for even division ratio
	0	**Reserved** Access: RO Format: MBZ

DKL_CLKTOP2_HSCLKCTL

DKL_CLKTOP2_HSCLKCTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B30h-168B33h
Name:	DKL_CLKTOP2_HSCLKCTL_NULL
ShortName:	DKL_CLKTOP2_HSCLKCTL_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26:25	**od_clktop2_clkobs_inputsel** mux select for oc_dfx_ck_clk2obs[0] digobs output 00b: hsdiv output clock 01b: iclk_bypass input from other clktop 10b: dsdiv output clock 11b: non-divided pll clock
	24	**od_clktop2_clk2obs_en_h** enable of oc_dfx_ck_clk2obs[0] digobs output 0b: Disable 1b: Enable
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Reserved**
	19	**Reserved** Access: RO Format: MBZ
	18	**od_clktop2_outclk_bypassen_h** enable of bypass clock output to the other clktop

DKL_CLKTOP2_HSCLKCTL

Value	Name
0b	Disable
1b	Enable

17 **Reserved**

Access:	RO
Format:	MBZ

16 **od_clktop2_coreclk_inputsel**

mux select for input clock to coreclk divhub

Value	Name
0b	hsdiv output
1b	dsdiv output

15:14 **od_clktop2_tlinedrv_clksel**

mux select for non-dedicated tlinedrv clock

Value	Name
00b	hsclkdiv output
01b	iclk_bypass input from other clktop
10b	dsdiv output clock
11b	non-divided pll clock

13:12 **od_clktop2_hsdiv_divratio**

Divider ratio for high speed divider. Div1

Value	Name
00b	Divide by 2
01b	Divide by 3
10b	Divide by 5
11b	Divide by 7

11:8 **od_clktop2_dsdiv_divratio**

Divider ratio settings for programmable divider. Div2

Value	Name
0000b	No Division
0001b	No Div **[Default]**
0010b	Divide by 2
0011b	Divide by 3
0100b	Divide by 4
0101b	Divide by 5
0110b	Divide by 6
0111b	Divide by 7
1000b	Divide by 8

DKL_CLKTOP2_HSCLKCTL

	1001b	Divide by 9
	1010b	Divide by 10

7 — od_clktop2_tlinedrv_overrideen

override enable for following 4 tlinedrv enables

Value	Name
0b	Disable
1b	Enable

6 — od_clktop2_tlinedrv_enleft_ded_h_ovrd

enable of left side dedicated tlinedrv to output full-rate clock to left lanes

Value	Name
0b	Disable
1b	Enable

5 — od_clktop2_tlinedrv_enright_ded_h_ovrd

enable of right side dedicated tlinedrv to output full-rate clock to right lanes

Value	Name
0b	Disable
1b	Enable

4 — od_clktop2_tlinedrv_enleft_h_ovrd

enable of left side tlinedrv to output divided clock to left lanes

Value	Name
0b	Disable
1b	Enable **[Default]**

3 — od_clktop2_tlinedrv_enright_h_ovrd

enable of right side tlinedrv to output divided clock to right lanes

Value	Name
0b	Disable
1b	Enable **[Default]**

2 — od_clktop2_dsdiv_en_h

Enable dsdiv clock divider. Div2.

Value	Name
0b	Disable
1b	Enable **[Default]**

1 — Reserved

Access:	RO
Format:	MBZ

DKL_CLKTOP2_HSCLKCTL		
	0	**od_clktop2_hsdiv_en_h** Enable high speed clock divider. Div1 **Value** / **Name** 0b – Disable 1b – Enable **[Default]**

DKL_CMN_ANA_DWORD28

DKL_CMN_ANA_DWORD28	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B98h-168B9Bh
Name:	DKL_CMN_ANA_DWORD28_NULL
ShortName:	DKL_CMN_ANA_DWORD28_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**clktop2_id_vga_chpmp_div_en_h** Default Value: 1
	27:25	**clktop2_id_vga_chpmp_ck_divratio** Default Value: 0100b
	24:21	**Reserved** Access: RO Format: MBZ
	20	**clktop1_id_vga_chpmp_div_en_h** Default Value: 1
	19:16	**clktop1_id_vga_chpmp_ck_divratio** Default Value: 0101b
	15	**refclkin2_refclk_dlane_en** Default Value: 1
	14	**refclkin2_refclk_sel**
	13:12	**refclkin2_refclk_dlane_sel**
	11	**refclkin1_refclk_dlane_en** Default Value: 1
	10	**refclkin1_refclk_sel**
	9:8	**refclkin1_refclk_dlane_sel**
	7	**clktop2_vga_clk2dl_en** Default Value: 1

DKL_CMN_ANA_DWORD28		
	6	**clktop2_vga_clk_sel**
	5	**clktop2_divby2clk_bypass_en**
	4	**clktop2_plldivby2_2dmon_en_h**
	3	**clktop1_vga_clk2dl_en** Default Value: 1
	2	**clktop1_vga_clk_sel**
	1	**clktop1_divby2clk_bypass_en**
	0	**clktop1_plldivby2_2dmon_en_h**

DKL_CMN_DIG_PLL_MISC

DKL_CMN_DIG_PLL_MISC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B94h-168B97h
Name:	DKL_CMN_DIG_PLL_MISC_NULL
ShortName:	DKL_CMN_DIG_PLL_MISC_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:18	**Reserved**
	17	**od_cri_cascaded_pll2_enable**
	16	**od_cri_cascaded_pll1_enable**
	15:1	**Reserved**
	0	**od_cri_pll2_pcie_enable**

DKL_CMN_UC_DW27

DKL_CMN_UC_DW27 - DKL_CMN_UC_DW27

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168B50h
Name:	DKL_CMN_UC_DW27
ShortName:	DKL_CMN_UC_DW27

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**Spare28** Default Value: 0b Access: RO
	27	**Spare27** Default Value: 0b Access: RO
	26	**Spare26** Default Value: 0b Access: RO
	25	**Spare25** Default Value: 0b Access: RO
	24	**Spare24** Default Value: 0b Access: RO
	23	**Spare23** Default Value: 0b Access: RO
	22	**Spare22** Default Value: 0b Access: RO

DKL_CMN_UC_DW27 - DKL_CMN_UC_DW27

21 Spare21

Default Value:	0b
Access:	RO

20 Spare20

Default Value:	0b
Access:	RO

19 Spare19

Default Value:	0b
Access:	RO

18 Spare18

Default Value:	0b
Access:	RO

17 Spare17

Default Value:	0b
Access:	RO

16 Spare16

Default Value:	0b
Access:	RO

15 uC health

Access:	R/W

- PHY uC health bit default
  - FW not ready.
- uC mode
  - PHY will set this bit to 1 after FW download is complete. Display polls this bit to '1'.
- In uC mode, direct IOSF transactions are supported.

Value	Name	Description
0b	**[Default]**	uC mode: FW not ready. uC bypass mode: Display can force this bit to '1' to select uC bypass (direct IOSF) mode.
1b		uC mode: FW ready. uC bypass mode: direct IOSF mode is set.

14:13 Reserved

Access:	RO
Format:	MBZ

DKL_CMN_UC_DW27 - DKL_CMN_UC_DW27

12	**Spare12**	
	Default Value:	0b
	Access:	R/W
11	**Spare11**	
	Default Value:	0b
	Access:	R/W
10	**Spare10**	
	Default Value:	0b
	Access:	R/W
9	**Spare9**	
	Default Value:	1b
	Access:	R/W
8	**Spare8**	
	Default Value:	0b
	Access:	R/W
7	**Spare7**	
	Default Value:	0b
	Access:	R/W
6	**Spare6**	
	Default Value:	0b
	Access:	R/W
5	**Spare5**	
	Default Value:	1b
	Access:	R/W
4	**Spare4**	
	Default Value:	0b
	Access:	R/W
3	**Spare3**	
	Default Value:	0b
	Access:	R/W
2	**Spare2**	
	Default Value:	1b
	Access:	R/W
1	**Spare1**	
	Default Value:	0b
	Access:	R/W

DKL_CMN_UC_DW27 - DKL_CMN_UC_DW27		
	0	**Spare0** Default Value: 0b Access: R/W

DKL_DP_MODE

DKL_DP_MODE - DKL_DP_MODE		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	168B0Ch-168B0Fh	
Name:	DKL_DP_MODE_LN0_ACU_NULL	
ShortName:	DKL_DP_MODE_LN0_ACU_NULL	
Reset:	global	
This register is not reset by device 2 FLR.		

DWord	Bit	Description
0	31:24	**ldo_powerup_timer** Default Value: 02h Timer to decide when LDO would be up. In case pwr_gate is used instead of LDO, it's configured to wait 20us, i.e 9'd500 by default using 25 MHz susclk.
	23	**cfg_tr2_pwrgate_timer_bypass**
	22	**cfg_tr_pwrgate_timer_bypass**
	21	**cfg_cl_pwrgate_timer_bypass**
	20	**cfg_dig_pwrgate_timer_bypass**
	19	**cfg_crireg_cold_boot_done**
	18	**cfg_vr_pulldwn2gnd_tr2**
	17	**cfg_vr_pulldwn2gnd_tr**
	16	**cfg_ldo_powerup_timer_8**
	15	**cfg_corepwr_ack_with_pcs_pwrreq**
	14	**cfg_cri_digpwr_req**
	13	**cfg_laneclkreq_force** Default Value: 1b When cfg_laneclkreq_gating_ctrl is low, this value will be used for the lane sus_clk request
	12	**cfg_laneclkreq_gating_ctrl** 1'b1 - lanesusclk req gating enabled
	11	**cfg_susclk_gating_ctrl** 1'b1 - susclk gating enabled
	10	**cfg_rawpwr_req_override** Keep rawpwr on when this bit is 1
	9	**cfg_digpwr_req_override** Keep digpwr on when this bit is 1

DKL_DP_MODE - DKL_DP_MODE		
	8	**cfg_rawpwr_gating_ctrl** Power gating enable reg for raw power
	7	**cfg_dp_x2_mode** Indicates x2 mode for DP
	6	**cfg_dp_x1_mode** Indicates x1 mode for DP
	5	**cfg_tr2pwr_gating_ctrl** Power gating enable reg for tr2
	4	**cfg_trpwr_gating_ctrl** Power gating enable reg for tr
	3	**cfg_clnpwr_gating_ctrl** Power gating enable reg for cln
	2	**cfg_digpwr_gating_ctrl** Power gating enable reg for dig
	1	**cfg_gaonpwr_gating_ctrl** Power gating enable reg for gaon
	0	**cfg_suspwr_gating_ctrl** Power gating enable reg for sus

DKL_PLL_DIV0

DKL_PLL_DIV0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B00h-168B03h
Name:	DKL_PLL1_DIV0_NULL
ShortName:	DKL_PLL1_DIV0_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:30	**i_truelock_criteria_1_0** Default Value: 01b True lock indicator criteria. After early lock generation, external PLL lock indicator asserted high when phase error is less than threshold value 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	29:28	**i_earlylock_criteria_1_0** Default Value: 11b Early lock indicator criteria. Early PLL lock indicator asserted high when phase error is less than threshold value. 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	27:25	**i_afc_startup_2_0** Default Value: 000b This is for AFC start point. 000: fine = 511 001: fine = 639 (+128) 010: fine = 767 (+256) 011: fine = 895 (+384) 100: NA 101: fine = 127 (-384) 110: fine = 255 (-256) 111: fine = 383 (-128).

DKL_PLL_DIV0		
	24	**i_divretimeren** Retiming of feedback clock
	23:21	**i_gainctrl_2_0** Default Value: 001b Adjustable gain for loop filter. Both coefficients shifted right by gainctrl before lock.
	20:16	**i_int_coeff_4_0** Default Value: 07h integral coeff. = 2^(-int_coeff), tageting up to 2^-11.
	15:12	**i_prop_coeff_3_0** Default Value: 0010b proportional coeff. = 2^(-prop_coeff+1).
	11:8	**i_fbprediv_3_0** Default Value: 10b predivider ratio 0000,0001 : reserved 0010: /2 0100: /4 0011: reserved Rest: reserved
	7:0	**i_fbdiv_intgr** Default Value: 69h Feedback divider post division (M2 integer)

DKL_PLL_DIV1

DKL_PLL_DIV1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B40h-168B43h
Name:	DKL_PLL1_DIV1_NULL
ShortName:	DKL_PLL1_DIV1_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**i_bw_ampmeas_window** Default Value: 0b 0: 10 modulation cycles of averaging for mplitude measurement 1: 20 modulation cycles of averaging for mplitude measurement
	30:29	**i_bias_calib_stepsize_1_0** Default Value: 00b Bias Calibration Step Size during linear search 00: 1 01: 2 10: 3 11: 4
	28:24	**i_ctrim_4_0** Default Value: 0Ch Cap trimming for irefout. This also has refclock dependency. Current default is for 24MHz.
	23	**i_fastlock_internal_reset** Default Value: 1b Clears internal fastlock memory so that next cold start will do both TDC and AFC calibration instead of fast lock. NOTE: this does not clear the i_fastlock_en_h register bit, clears functional register and self-clears[br]Formerly, i_bbthresh[3] (no longer strap).
	22:21	**i_bias_r_programmability** Default Value: 10b Bias Filter R programmability - note mapped to bias_bonus[1:0].

DKL_PLL_DIV1

	20:16	**i_ireftrim_4_0** Default Value: 1Ch Output current trim . Mirror ratio is changed based on constant current requirement. SInce it is refclock dependent, needs to be reconfigurable i_ireftrim[4:0] - 38.4/19.2 MHz= 5'h1C i_ireftrim[4:0] - 25.0/100.0 MHz = 5'h18 Step size: 20 uA.
	15	**i_biasfilter_en_delay** Default Value: 1b 0: Filter enabled even before pll enabled 1: Filter enable is delay until lock acquisition This bit is sensitive only when i_bias_filter_en is set (bit3)
	14	**i_bias_filter_en** Value: 0b — Name: Disable Value: 1b — Name: Enable **[Default]**
	13	**i_biascal_en_h** Bias Calibration Signal. Bias cal should be disable when override DCO coarse code.
	12	**i_dcodither_config** Whenever we have binary weighted MFC cap, this should be set to 1'b0. Ex: i_dcofine_resolution = 1'b0. For this case, this should be set to 1'b0. 0: No floating dither 1: Floating dither (511+Nobinary - Floating dither).
	11:8	**i_lockthresh_3_0** Default Value: 4h Digital lock detect threshold, the PLL will generate plllockout when the phase error detected by TDC is within lockthresh number of TDC counts for 64 consecutive cycles 5*16 (TDC Code) = 80 (16 is internally hard coded scalar value) - This setting isin middle of coarse range.
	7:0	**i_tdctargetcnt_7_0** Default Value: 22h TDC tristate buffer calibration counter value. Delay line loop oscillation is counted over two refclk cycles. This is used for TDC coarse code calibration.

DKL_PLL_FRAC_LOCK

DKL_PLL_FRAC_LOCK

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B08h-168B0Bh
Name:	DKL_PLL1_FRAC_LOCK_NULL
ShortName:	DKL_PLL1_FRAC_LOCK_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:30	**i_cml2cmosbonus_1_0** Default Value: 10b NOTE: These bits are ported to anatop bit [0] mapped to cml2cmosbonus[1] port - o_plllc_ck_dcocmosclkp_ana disable '1' = o_plllc_ck_dcocmosclkp_ana is disabled (ie for MG B0) '0' = both phases of the cmos clock toggle at the interface bit[1] mapped to cml2cmosbonus[2] port - available.
	29:27	**i_bb_gain2_2_0** Default Value: 000b BB gain for second BB range.
	26:24	**i_bb_gain1_2_0** Default Value: 000b BB gain for first BB range.
	23	**i_fastlock_en_h** Enable FLL based AFC; this replaces binary search based AFC. FLL based AFC faster than binary search. Value: 0b – Disable Value: 1b – Enable
	22:19	**i_fllafc_gain_3_0** Default Value: 1000b Initial FLL gain that decrements down to 1 every refclk cycle in the beginning of FLL based AFC.
	18:16	**i_fllafc_lockcnt_2_0** Default Value: 100b Number of refclk cycles for FLL lock after gain is reduced to 1.

DKL_PLL_FRAC_LOCK		
	15:8	**i_max_cselafc_7_0** Default Value: B5h Max. AFC code for a given DCO.
	7:0	**i_init_cselafc_7_0** Default Value: 6Ah Initial AFC code for FLL AFC; apply approximate AFC, and starting at closer frequency helps fast/accurate calibration.

DKL_PLL_LF

DKL_PLL_LF	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B04h-168B07h
Name:	DKL_PLL_LF_NULL
ShortName:	DKL_PLL_LF_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**i_afc_divratio** 0: DCO/4 (prediv: 2, Mdithdiv: 2) 1: DCO/8 (prediv: 4 Mdithdiv: 2)
	30:29	**i_plllock_sel_1_0** Default Value: 00b select between lockdetect-based plllock or counter based plllock 11: Sticky lock 10: Counter-based 01: Lock Detection + Counter 00: Lock Detection.
	28:24	**i_bwphase_4_0** Default Value: 00h Phase amplitude for bandwidth measurement
	23:21	**i_ft_mode_sel_2_0** Default Value: 010b ftmodesel[2:0] : 9b vs 10b finetune selection, lsb0 tuning 3'b000 : 10b Nom -> Dither = LSB0, LSB0 = LSB0 3'b001 : 10b+ -> Dither = LSB+, LSB0 = LSB0+ 3'b010 : 10b- -> Dither = LSB-, LSB0 = LSB0- 3'b011 : 10b DNL -> Dither = LSB01, LSB0 = LSB0+ 3'h1xx: 9b -> Dither = LSB1, LSB0 = N/A
	20:19	**i_bw_mode_1_0** Default Value: 00b 00: No measurement 01: BW measurement 10: BW calibration up to +1 direction 11: BW calibration up to +2 direction

DKL_PLL_LF		
	18:16	**i_bw_upperbound_2_0** Default Value: 000b Upper bound setting for BW 000: 0.1MHz 001: 1 MHz 010: 2 MHz 011: 5 MHz 100: 6 MHz 101: 8 MHz 110: 16 MHz]111: 25MHz
	15:13	**i_bw_lowerbound_2_0** Default Value: 000b Lower bound setting for BW 000: 0.1MHz 001: 1 MHz 010: 2 MHz 011: 5 MHz 100: 6 MHz 101: 8 MHz 110: 16 MHz 111: 25MHz
	12:9	**i_dcoamp_3_0** Default Value: 1001b Amplitude override value for DCO, 0000 is min amplitude, 1111 is max amplitude, applied when i_dcoampovrden_h is high. 4bit is left shifted to generate 6bit code (x4).
	8	**i_dcoampovrrden_h** Default Value: 1b DCO amplitude override enable: 0 DCO amplitude set internally (default) 1 DCO amplitude is set by i_dcoamp[3:0]
	7:5	**i_bbthresh2_2_0** Default Value: 0b threshold for second (inner) bang-bang (BB) range.
	4:2	**i_bbthresh1_2_0** Default Value: 0b threshold for first (inner) bang-bang (BB) range.
	1:0	**i_tdc_offset_1_0** Default Value: 0b TDC Offset during lock for integer mode.

DKL_PLL1_CNTR_XXXX_SETTINGS

DKL_PLL1_CNTR_XXXX_SETTINGS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B9Ch-168B9Fh
Name:	DKL_PLL1_CNTR_BIST_SETTINGS_NULL
ShortName:	DKL_PLL1_CNTR_BIST_SETTINGS_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:28	**RESERVED205** Access: RO
	27:24	**RESERVED204** Access: RO
	23	**RESERVED203** Access: RO
	22:21	**I_DFX_DIV_CKLO_1_0** Access: R/W
	20	**I_M1_LONGLOOP_SEL** Access: R/W
	19:18	**I_DITHER_DIV_1_0** Default Value: 01b Access: R/W
	17	**I_PLLLC_REG_LONGLOOPCLK_SEL** Access: R/W
	16	**AI_PLLLC_REG_FBCLKEXT_SEL** Access: R/W
	15	**RESERVED197** Access: RO
	14:10	**RESERVED196** Access: RO
	9:8	**I_IREFGEN_SETTLING_TIME_RO_STANDBY_1_0** Access: R/W

DKL_PLL1_CNTR_XXXX_SETTINGS		
	7:0	**I_IREFGEN_SETTLING_TIME_CNTR_7_0** Default Value: 0x30 Access: R/W

DKL_PMD_FORCE_PCS_IF_TX1

DKL_PMD_FORCE_PCS_IF_TX1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168BA4h-168BA7h
Name:	DKL_PMD_FORCE_PCS_IF_TX1_NULL
ShortName:	DKL_PMD_FORCE_PCS_IF_TX1_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**reserved1**
	30	**ecsr_force_val_pmd_pwdn_n_rx** Access: R/W
	29	**ecsr_force_en_pmd_pwdn_n_rx** Access: R/W
	28	**ecsr_force_val_pmd_pwdn_n_tx1** Access: R/W
	27	**ecsr_force_en_pmd_pwdn_n_tx1** Access: R/W
	26	**ecsr_eidle_en_by_tx_pmd_pwdn_n_tx1** Default Value: 1b Access: R/W
	25:22	**force_req_valid_pmd_rx_pwr_mode** Default Value: 0001b Access: R/W
	21:18	**force_val_pmd_rx_pwr_mode** Access: R/W
	17	**force_en_pmd_rx_pwr_mode** Access: R/W
	16:13	**force_req_valid_pmd_tx_pwr_mode_tx1** Default Value: 0001b Access: R/W
	12:9	**force_val_pmd_tx_pwr_mode_tx1** Access: R/W

DKL_PMD_FORCE_PCS_IF_TX1		
	8	**force_en_pmd_tx_pwr_mode_tx1** Access: R/W
	7	**ecsr_force_val_pmd_hard_rst_b_tx1** Access: R/W
	6	**ecsr_force_en_pmd_hard_rst_b_tx1** Access: R/W
	5	**ecsr_force_val_pmd_hard_rst_b_rx** Access: R/W
	4	**ecsr_force_en_pmd_hard_rst_b_rx** Access: R/W
	3	**force_val_pmd_txeidle_tx1** Access: R/W
	2	**force_en_pmd_txeidle_tx1** Access: R/W
	1	**force_val_pmd_pwdn_n_tx1** Access: R/W
	0	**force_en_pmd_pwdn_n_tx1** Access: R/W

DKL_REFCLKIN_CTL

DKL_REFCLKIN_CTL - DKL_REFCLKIN_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B2Ch-168B2Fh
Name:	DKL_REFCLKIN_CTL_NULL
ShortName:	DKL_REFCLKIN_CTL_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:12	**Reserved** Access: RO Format: MBZ
	11	**od_refclkin2_refclkinjmux** mux select of external injection refclk inputs: 0 to select amonrefclkinj 1 to select rcomprefclkinj
	10:8	**od_refclkin2_refclkmux** mux select for refclk output 3'b000: external injection refclk 3'b001: xtalinrefclk 3'b010:mgrefclkin 3'b011: socrefclk1 3'b100:socrefclk2 3'b101:socrefclk3 3'b110:socrefclk4 3'b111:socrefclk5
	7:4	**Reserved** Access: RO Format: MBZ
	3	**od_refclkin1_refclkinjmux** mux select of external injection refclk inputs: 0 to select amonrefclkinj 1 to select rcomprefclkinj
	2:0	**od_refclkin1_refclkmux** mux select for refclk output. 3'b000: external injection refclk3'b001: xtalinrefclk 3'b010: mgrefclkin 3'b011: socrefclk13'b100: socrefclk2 3'b101: socrefclk33'b110: socrefclk4 3'b111: socrefclk5

DKL_SSC

DKL_SSC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B38h-168B3Bh
Name:	DKL_SSC_NULL
ShortName:	DKL_SSC_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:29	**i_iref_ndivratio_2_0** Default Value: 10b SSC injection Adaptive Gain Change Enable
	28:26	**ssc_stepnum_offset_2_0** Default Value: 000b SSC spread step is calculated with two registers, i_sscstepnum and i_sscstepnum_offset. SSC steps = 2^(i_sscstepnum + 1) + 4*i_sscstepnum_offset.
	25	**i_sscinj_adapt_en_h** SSC injection Adaptive Gain Change Enable. Value: 0b – Disable Value: 1b – Enable
	24	**i_sscinj_en_h** SSC inject enable. Value: 0b – Disable Value: 1b – Enable
	23:16	**i_sscsteplength_7_0** Default Value: 13h Number of ref clock cycles in one SSC step.
	15:14	**i_sscfll_update_sel_1_0** Default Value: 0b Select frequency update rate for FLL SSC.

DKL_SSC

	13:11	**i_sscstepnum_2_0** Default Value: 100b Number of SSC steps (=2^sscstepnum).
	10	**i_ssc_openloop_en_h** Default Value: 0b Open loop SSC enable.
	9	**i_sscen_h** Default Value: 1b Dynamic control of SSC modulator.
	8	**i_sscfllen_h** Default Value: 0b Frequency adjustment for FLL SSC.
	7:6	**i_bias_gb_sel_1_0** Default Value: 11b Select guardband after bias calibration.
	5:0	**i_init_dcoamp_5_0** Default Value: 3Fh initial DCOAMP value.

DKL_TDC_COLDST_BIAS

DKL_TDC_COLDST_BIAS	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B44h-168B47h
Name:	DKL_TDC_COLDST_BIAS_NULL
ShortName:	DKL_TDC_COLDST_BIAS_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:29	**i_cloadctrlext_4_2** Default Value: 00h cload control override for H Vernier line. This is applied when i_tdccalexten_h = 1.
	28:24	**i_tribufctrlext_4_0** Default Value: 00h Tribufctrl control override. This is applied when i_tdccalexten_h = 1.
	23:16	**i_dcocoarse_7_0** Default Value: 00h DCO coarse tune frequency value, when dcocoarse_ovrd_h is '1', this input is used to override the value calculated from the Automatic Frequency Calibration (AFC) block.
	15:8	**i_sscstepsize_7_0** Default Value: 0Fh Fractional value for one SSC frequency step.
	7:0	**i_feedfwdgain_7_0** Default Value: 23h Feed forwad gain for fractional mode/SSC mode PLL [br]This setting is needed whenever PLL is configured in fractional mode or configured for SSC clock generation.

DKL_TX_DPCNTL0

DKL_TX_DPCNTL0 - DKL_TX_DPCNTL0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B14h-168B17h
Name:	DKL_TX_DPCTRL0_TX1LN0_NULL
ShortName:	DKL_TX_DPCTRL0_TX1LN0_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**Trainingen_tx1** Enable set for programming in compliance mode.
	29	**Pipe_select_tx1** Override this bit to 0 to take the BIOS programmed Values and not pipe
	28	**Slow_trim_enable_tx1** Default Value: 1b Enable or Disable the slow trim.
	27:23	**shunt_cm_tx1** Back mode select for the Shunt CM
	22:18	**shunt_cp_tx1** Preshoot Co-efficients
	17:13	**Preshoot Control l0** Pre-shoot coefficients
	12:8	**de_emphasis_control_l0_tx1** De-emphasis co-efficient
	7:3	**Cursor_Control_tx1** Backup mode for shunt on C0
	2:0	**Vswing Control_tx1** Default Value: 111b 3'b000 = 1V + 0dB (Full Swing) 3'b001 = 800 mV + 0dB 3'b100 = 600 mV + 0dB 3'b111 = 400 mV + 0dB

DKL_TX_DPCNTL1

DKL_TX_DPCNTL1 - DKL_TX_DPCNTL1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B1Ch-168B1Fh
Name:	DKL_TX_DPCNTL1_TX2LN0_NULL
ShortName:	DKL_TX_DPCNTL1_TX2LN0_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**Trainingen_tx2** Enable set for programming in compliance mode.
	29	**Pipe_select_tx2** Override this bit to 0 to take the BIOS programmed Values and not pipe
	28	**Slow_trim_enable_tx2** Default Value: 1b Enable or Disable the slow trim.
	27:23	**shunt_cm_tx2** Back mode select for the Shunt CM
	22:18	**shunt_cp_tx2** Preshoot Co-efficients
	17:13	**Preshoot Control l0** Pre-shoot coefficients
	12:8	**de_emphasis_control_l0_tx2** De-emphasis co-efficient
	7:3	**Cursor_Control_tx2** Backup mode for shunt on C0
	2:0	**Vswing Control_tx2** Default Value: 111b 3'b000 = 1V + 0dB (Full Swing) 3'b001 = 800 mV + 0dB 3'b100 = 600 mV + 0dB 3'b111 = 400 mV + 0dB

DKL_TX_DPCNTL2

DKL_TX_DPCNTL2 - DKL_TX_DPCNTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B24h-168B27h
Name:	DKL_TX_DPCNTL2_TX2LN0_NULL
ShortName:	DKL_TX_DPCNTL2_TX2LN0_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:23	**Reserved** Access: RO Format: MBZ
	22:10	**reserved_dp3**
	9	**dp_fifo_depth_tx1**
	8	**dp_fifo_depth_tx2**
	7	**dp_2ui_4ui_mode_en** Value: 0 — Name: 4UI Value: 1 — Name: 2UI
	6:5	**loadgenselect_tx2** loadgen select for datapath2ui - Look at the sheet for CFG per Tx
	4:3	**loadgenselect_tx1** loadgen select for datapath2ui - Look at the sheet for CFG per Tx
	2	**dp20bitmode** 20 bit mode support. This will need to be set to 1 if Pipe width does not reflect the 20bit mode.
	1	**rate8boverrideen** 8bit override enable. The pisorate_8b signal is normally decoded from PHYMODE and RATE. When 1, the pisorate_8b signal will take with pisorate8bit_ovrd value.
	0	**rate8boverride** value used for pisorate_8b when pisorate8bit_overden = 1.

DKL_TX_DW17

DKL_TX_DW17 - DKL_TX_DW17	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B48h-168B4Bh
Name:	DKL_TX_DW17_NULL
ShortName:	DKL_TX_DW17_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**cri_txdeemph_override11_6** cursor deemph override value when enable bit is set, or cri_txdeemph_override[11:6]
	23	**Reserved** Access: RO Format: MBZ
	22	**cri_txdeemph_override_en** txdeemph override enable bit
	21:16	**cri_txdeemph_override5_0** precursor deemph override value when enable bit is set, or cri_txdeemph_override[5:0]
	15:0	**Reserved** Access: RO Format: MBZ

DKL_TX_DW18

DKL_TX_DW18 - DKL_TX_DW18

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B4Ch-168B4Fh
Name:	DKL_TX_DW18_NULL
ShortName:	DKL_TX_DW18_NULL
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	5:0	**cri_txdeemph_override17_12** cursor deemph override value when enable bit is set, or cri_txdeemph_override[17:12]

DKL_TX_FW_CALIB

DKL_TX_FW_CALIB		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	168B58h-168B5Bh	
Name:	DKL_TX_FW_CALIB_NULL	
ShortName:	DKL_TX_FW_CALIB_NULL	
Reset:	global	
This register is not reset by the device 2 FLR.		

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**cfg_disable_wait_init_periodic** This bit has to be set everytime TypeC connection switches from USB to DP ALT mode. Recommendation is to set this bit after PLL programming is completed.
	6	**tx1_dcc_cmp**
	5	**cfg_fw_oneshotcal_req_ctrl_val**
	4	**cfg_tx_fw_oneshotcal_req_ctrl_en**
	3	**cfg_tx_pwr_cal_en_ovrd_val**
	2	**cfg_tx_pwr_cal_en_ovrd_en**
	1	**cfg_rate_cal_en_ovrd_val**
	0	**odkl_tx_rate_ana_cal_en**

DKL_TX_PMD_LANE_SUS_LN0

DKL_TX_PMD_LANE_SUS_LN0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B88h-168B8Bh
Name:	DKL_TX_PMD_LANE_SUS_LN0_NULL
ShortName:	DKL_TX_PMD_LANE_SUS_LN0_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:0	**dummy** Flush all register bits to '0' at the time Display takes control of this PHY lane.

DKL_TX_PMD_LANE_SUS_LN1

DKL_TX_PMD_LANE_SUS_LN1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168B8Ch-168B8Fh
Name:	DKL_TX_PMD_LANE_SUS_LN1_NULL
ShortName:	DKL_TX_PMD_LANE_SUS_LN1_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:0	**dummy** Flush all register bits to '0' at the time Display takes control of this PHY lane.

DKL_XXX_TDC_CRO

DKL_XXX_TDC_CRO	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	168BA0h-168BA3h
Name:	DKL_XXX_TDC_CRO_NULL
ShortName:	DKL_XXX_TDC_CRO_NULL
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**I_PLLLC_REG_FULLCALRESETB** Default Value: 1 Access: R/W
	30	**I_DFX_POSTDIV_DISABLE** Access: R/W
	29	**I_DFX_MDFX_ENABLE** Access: R/W
	28	**I_DFX_MDITH_DISABLE** Access: R/W
	27	**I_DFX_TDC_DISABLE** Access: R/W
	26:25	**I_PLLLC_IREF_CLOCK_SEL_1_0** Access: R/W
	24	**I_PLLLC_IREF_CLOCK_OVRD** Access: R/W
	23	**I_PLLLC_REG_REFCLK_ACK_MODE_CTRL** Access: R/W
	22	**I_PLLLC_REG_REFCLK_ACK** Access: R/W
	21	**I_PLLLC_REG_ACTIVE_STANDBY_MODE_CTRL** Access: R/W
	20	**I_PLLLC_REG_ACTIVE_STANDBY** Access: R/W

DKL_XXX_TDC_CRO			
	19	**I_PLLLC_REG_RESETB_ANA_MODE_CTRL**	
		Access:	R/W
	18	**I_PLLLC_RO_MODE_CTRL**	
		Access:	R/W
	17	**I_PLLLC_RO_REGDISABLE**	
		Access:	R/W
	16	**I_PLLLC_RO_REGEN_H**	
		Access:	R/W
	15:14	**I_PLLLC_EN_MODE_CTRL_1_0**	
		Default Value:	10b
		Access:	R/W
	13	**I_PLLLC_REGEN_H**	
		Access:	R/W
	12	**I_IREF_REFCLK_INV_EN**	
		Access:	R/W
	11	**Reserved**	
	10	**Reserved**	
	9	**I_VGSBUFEN**	
		Access:	R/W
	8	**I_IREFINT_EN**	
		Default Value:	1b
		Access:	R/W
	7	**I_IREFBIAS_STARTUP_PULSE_BYPASS**	
		Access:	R/W
	6:5	**I_IREFBIAS_STARTUP_PULSE_WIDTH_1_0**	
		Default Value:	01b
		Access:	R/W
	4	**I_COLDSTART**	
		Default Value:	1b
		Access:	R/W
	3	**I_BBINLOCK_H**	
		Access:	R/W
	2:1	**I_SWCAP_IREFGEN_CLKMODE_1_0**	
		Access:	R/W
	0	**I_TDCDC_EN_H**	
		Access:	R/W

DKLP_ACU_ACU_DWORD4

DKLP_ACU_ACU_DWORD4		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
RESERVED		
DWord	**Bit**	**Description**
0	31:29	**cfg_reserved513** Default Value: 000b cfg_reserved513_defaultreset Access: RO reserved
	28:24	**cfg_clkhub2_monana1selectb_4_0** Default Value: 1Fh cfg_clkhub2_monana1selectb_4_0_defaultreset Access: R/W DFX control of CLOCK_DIST
	23:21	**cfg_reserved512** Default Value: 000b cfg_reserved512_defaultreset Access: RO reserved
	20:16	**cfg_clkhub2_monana1select_4_0** Default Value: 00h cfg_clkhub2_monana1select_4_0_defaultreset Access: R/W DFX control of CLOCK_DIST
	15:13	**cfg_reserved511** Default Value: 000b cfg_reserved511_defaultreset Access: RO reserved
	12:8	**cfg_clkhub2_monana0selectb_4_0** Default Value: 1Fh cfg_clkhub2_monana0selectb_4_0_defaultreset Access: R/W DFX control of CLOCK_DIST
	7	**cfg_reserved510** Default Value: 0b cfg_reserved510_defaultreset Access: RO reserved

DKLP_ACU_ACU_DWORD4		
	6	**cfg_cfg_reset_phymode_change** Default Value: 0b cfg_cfg_reset_phymode_change_defaultreset Access: R/W cfg bit to reset phymode change feature bit in acu suswell pwrctrl
	5	**cfg_o_cri_cfg_phymode_switch** Default Value: 0b cfg_o_cri_cfg_phymode_switch_defaultreset Access: R/W phymode_switch for pwr_ctrl
	4:0	**cfg_clkhub2_monana0select_4_0** Default Value: 00h cfg_clkhub2_monana0select_4_0_defaultreset Access: R/W DFX control of CLOCK_DIST

DKLP_ACU_ACU_DWORD8

DKLP_ACU_ACU_DWORD8

Register Space: MMIO: 0/2/0
Size (in bits): 32

DP MODE

DWord	Bit	Description
0	31:24	**cfg_ldo_powerup_timer** Default Value: 02h cfg_ldo_powerup_timer_defaultreset Access: R/W ip74pppxdkltypecfamilyew_Timer to decide when LDO would be up, in case pwr_gate is used instead of LDO, it's configured to wait 20us, i.e 9'd500 by default using 25 MHz susclk
	23	**cfg_cfg_tr2_pwrgate_timer_bypass** Default Value: 0b cfg_cfg_tr2_pwrgate_timer_bypass_defaultreset Access: R/W When this bit is 1, bypass the pwrgate ip74pppxdkltypecfamilyew_timer, which is configurable with cfg_ldo_powerup_timer
	22	**cfg_cfg_tr_pwrgate_timer_bypass** Default Value: 0b cfg_cfg_tr_pwrgate_timer_bypass_defaultreset Access: R/W When this bit is 1, bypass the pwrgate ip74pppxdkltypecfamilyew_timer, which is configurable with cfg_ldo_powerup_timer
	21	**cfg_cfg_cl_pwrgate_timer_bypass** Default Value: 0b cfg_cfg_cl_pwrgate_timer_bypass_defaultreset Access: R/W When this bit is 1, bypass the pwrgate ip74pppxdkltypecfamilyew_timer, which is configurable with cfg_ldo_powerup_timer
	20	**cfg_cfg_dig_pwrgate_timer_bypass** Default Value: 0b cfg_cfg_dig_pwrgate_timer_bypass_defaultreset Access: R/W When this bit is 1, bypass the pwrgate ip74pppxdkltypecfamilyew_timer, which is configurable with cfg_ldo_powerup_timer
	19	**cfg_cfg_crireg_cold_boot_done** Default Value: 0b cfg_cfg_crireg_cold_boot_done_defaultreset Access: R/W set cold boot done

DKLP_ACU_ACU_DWORD8

18	**cfg_cfg_vr_pulldwn2gnd_tr2** Default Value: 0b cfg_cfg_vr_pulldwn2gnd_tr2_defaultreset Access: R/W if there is a chance of high voltage from hotplug through diodes. Needed for tr/tr2 LDO
17	**cfg_cfg_vr_pulldwn2gnd_tr** Default Value: 0b cfg_cfg_vr_pulldwn2gnd_tr_defaultreset Access: R/W if there is a chance of high voltage from hotplug through diodes. Needed for tr/tr2 LDO
16	**cfg_cfg_ldo_powerup_timer_8** Default Value: 0b cfg_cfg_ldo_powerup_timer_8_defaultreset Access: R/W ip74pppxdkltypecfamilyew_Timer to decide when LDO would be up, in case pwr_gate is used instead of LDO, it's configured to wait 20us, i.e 9'd500 by default using 25 MHz susclk
15	**cfg_cfg_corepwr_ack_with_pcs_pwrreq** Default Value: 0b cfg_cfg_corepwr_ack_with_pcs_pwrreq_defaultreset Access: R/W if this bit is 1, send corepwr_ack to pcs only when pcs_pwrreq is 1
14	**cfg_cfg_cri_digpwr_req** Default Value: 0b cfg_cfg_cri_digpwr_req_defaultreset Access: R/W Keep dig up during burst CRI transactions, this also bypasses handshake with the susclk domain, greatly reducing the latency.
13	**cfg_cfg_laneclkreq_force** Default Value: 1b cfg_cfg_laneclkreq_force_defaultreset Access: R/W When cfg_laneclkreq_gating_ctrl is low, this value will be used for the lane sus_clk request
12	**cfg_cfg_laneclkreq_gating_ctrl** Default Value: 0b cfg_cfg_laneclkreq_gating_ctrl_defaultreset Access: R/W 1'b1 - lanesusclk req gating enabled
11	**cfg_cfg_susclk_gating_ctrl** Default Value: 0b cfg_cfg_susclk_gating_ctrl_defaultreset Access: R/W 1'b1 - susclk gating enabled

DKLP_ACU_ACU_DWORD8

10	**cfg_cfg_rawpwr_req_override** Default Value: 0b cfg_cfg_rawpwr_req_override_defaultreset Access: R/W Keep rawpwr on when this bit is 1
9	**cfg_cfg_digpwr_req_override** Default Value: 0b cfg_cfg_digpwr_req_override_defaultreset Access: R/W Keep digpwr on when this bit is 1
8	**cfg_cfg_rawpwr_gating_ctrl** Default Value: 0b cfg_cfg_rawpwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for raw power
7	**cfg_cfg_dp_x2_mode** Default Value: 0b cfg_cfg_dp_x2_mode_defaultreset Access: R/W {cfg_dp_x2_mode,cfg_dp_x1_mode}: 00 -) Only main tx on {cfg_dp_x2_mode,cfg_dp_x1_mode}: 01 -) Only secondary tx on {cfg_dp_x2_mode,cfg_dp_x1_mode}: 1x -) Both tx on
6	**cfg_cfg_dp_x1_mode** Default Value: 0b cfg_cfg_dp_x1_mode_defaultreset Access: R/W {cfg_dp_x2_mode,cfg_dp_x1_mode}: 00 -) Only main tx on {cfg_dp_x2_mode,cfg_dp_x1_mode}: 01 -) Only secondary tx on {cfg_dp_x2_mode,cfg_dp_x1_mode}: 1x -) Both tx on
5	**cfg_cfg_tr2pwr_gating_ctrl** Default Value: 0b cfg_cfg_tr2pwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for tr2
4	**cfg_cfg_trpwr_gating_ctrl** Default Value: 0b cfg_cfg_trpwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for tr
3	**cfg_cfg_clnpwr_gating_ctrl** Default Value: 0b cfg_cfg_clnpwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for cln

DKLP_ACU_ACU_DWORD8		
	2	**cfg_cfg_digpwr_gating_ctrl** Default Value: 0b cfg_cfg_digpwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for dig
	1	**cfg_cfg_gaonpwr_gating_ctrl** Default Value: 0b cfg_cfg_gaonpwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for gaon
	0	**cfg_cfg_suspwr_gating_ctrl** Default Value: 0b cfg_cfg_suspwr_gating_ctrl_defaultreset Access: R/W Power gating enable reg for sus

DKLP_ACU_ICL_INDEXED_ACU_INDEXED_DWORD46

DKLP_ACU_ICL_INDEXED_ACU_INDEXED_DWORD46		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Reserved		
DWord	**Bit**	**Description**
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**cfg_reserved580** Default Value: 00h cfg_reserved580_defaultreset Access: RO reserved
	7:0	**cfg_reserved579** Default Value: 00h cfg_reserved579_defaultreset Access: RO reserved

DKLP_CMN_ANA_CMN_ANA_DWORD0

DKLP_CMN_ANA_CMN_ANA_DWORD0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
CLKTOP1_HSCLKCTL		
DWord	**Bit**	**Description**
0	31:27	**cfg_reserved504** Default Value: 00h cfg_reserved504_defaultreset Access: RO Power well:DIG
	26:25	**cfg_od_clktop1_clkobs_muxsel_1_0** Default Value: 00b cfg_od_clktop1_clkobs_muxsel_1_0_defaultreset Access: R/W mux select for oc_dfx_ck_clk2obs[0] digobs output 2'b00: hsdiv output clock 2'b01: iclk_bypass input from the other clktop 2'b10: dsdiv output clock 2'b11: non-dvided pll clock (test mode)
	24	**cfg_od_clktop1_clk2obs_en_h** Default Value: 0b cfg_od_clktop1_clk2obs_en_h_defaultreset Access: R/W enable of oc_dfx_ck_clk2obs[0] digobs output
	23:22	**cfg_reserved501** Default Value: 00b cfg_reserved501_defaultreset Access: RO Power well:DIG
	21:20	**cfg_od_clktop1_clktop1_vhfclk_testen_h_1_0** Default Value: 00b cfg_od_clktop1_clktop1_vhfclk_testen_h_1_0_defaultreset Access: R/W test mode enable of pll clock bit[0]: enable of pll clock to non-dedicated tlinedrv bit[1]: enable of pll clock to dfx ouput
	19	**cfg_reserved502** Default Value: 0b cfg_reserved502_defaultreset Access: RO Power well:DIG
	18	**cfg_od_clktop1_outclk_bypassen_h** Default Value: 0b cfg_od_clktop1_outclk_bypassen_h_defaultreset Access: R/W enable of bypass clock output to the other clktop

DKLP_CMN_ANA_CMN_ANA_DWORD0

	17	**cfg_reserved503** Default Value: 0b cfg_reserved503_defaultreset Access: RO Power well:DIG
	16	**cfg_od_clktop1_coreclk_inputsel** Default Value: 0b cfg_od_clktop1_coreclk_inputsel_defaultreset Access: R/W mux select for input clock to coreclk divhub 1'b0: select hsdiv output;1'b1: select dsdiv output
	15:14	**cfg_od_clktop1_tlinedrv_clksel_1_0** Default Value: 00b cfg_od_clktop1_tlinedrv_clksel_1_0_defaultreset Access: R/W mux select for non-dedicated tlinedrv clocks 2'b00: hsclkdiv output 2'b01: dsdiv output clktop 2'b10: iqdiv2 clock 2'b11: iqdiv2 clock
	13:12	**cfg_od_clktop1_hsdiv_divratio_1_0** Default Value: 00b cfg_od_clktop1_hsdiv_divratio_1_0_defaultreset Access: R/W divider ratio for high speed divider. 2'b00: div/2 2'b01: div/3 2'b10: div/5 2'b11: div/7
	11:8	**cfg_od_clktop1_dsdiv_divratio_3_0** Default Value: Ah cfg_od_clktop1_dsdiv_divratio_3_0_defaultreset Access: R/W divider ratio settings for programmable divider: 4'b0000: no division 4'b0001: no division 4'b0010 - 4'b1010: div/2 - div/10 4'b1011 - 4'b1111: not used (div/10)
	7	**cfg_od_clktop1_tlinedrv_overrideen** Default Value: 0b cfg_od_clktop1_tlinedrv_overrideen_defaultreset Access: R/W override enable for follwing 4 tlinedrv enables
	6	**cfg_od_clktop1_tlinedrv_enleft_ded_h_ovrd** Default Value: 1b cfg_od_clktop1_tlinedrv_enleft_ded_h_ovrd_defaultreset Access: R/W enable of left side dedicated tlinedrv to output full-rate clock to left lanes

DKLP_CMN_ANA_CMN_ANA_DWORD0

	5	**cfg_od_clktop1_tlinedrv_enright_ded_h_ovrd** Default Value: 1b cfg_od_clktop1_tlinedrv_enright_ded_h_ovrd_defaultreset Access: R/W enable of right side dedicated tlinedrv to output full-rate clock to right lanes
	4	**cfg_od_clktop1_tlinedrv_enleft_h_ovrd** Default Value: 0b cfg_od_clktop1_tlinedrv_enleft_h_ovrd_defaultreset Access: R/W enable of left side tlinedrv to output divided clock to left lanes
	3	**cfg_od_clktop1_tlinedrv_enright_h_ovrd** Default Value: 0b cfg_od_clktop1_tlinedrv_enright_h_ovrd_defaultreset Access: R/W enable of right side tlinedrv to output divided clock to right lanes
	2	**cfg_od_clktop1_dsdiv_en_h** Default Value: 1b cfg_od_clktop1_dsdiv_en_h_defaultreset Access: R/W enable of dsdiv clock divider
	1	**cfg_reserved500** Default Value: 0b cfg_reserved500_defaultreset Access: RO Power well:DIG
	0	**cfg_od_clktop1_hsdiv_en_h** Default Value: 1b cfg_od_clktop1_hsdiv_en_h_defaultreset Access: R/W enable of high speed clock divider

DKLP_CMN_ANA_CMN_ANA_DWORD1

DKLP_CMN_ANA_CMN_ANA_DWORD1

Register Space: MMIO: 0/2/0
Size (in bits): 32

CLKTOP1_CORECLKCTL1

DWord	Bit	Description
0	31:30	**cfg_reserved508** Default Value: 00b cfg_reserved508_defaultreset Access: RO Power well:DIG
	29	**cfg_od_clktop1_coreclkd_bypass** Default Value: 0b cfg_od_clktop1_coreclkd_bypass_defaultreset Access: R/W bypass enable of coreclkd to take input refclk
	28	**cfg_od_clktop1_coreclkd_divretimeren_h** Default Value: 1b cfg_od_clktop1_coreclkd_divretimeren_h_defaultreset Access: R/W retimer enable: 0 for odd division ratio, 1 for even division ratio
	27	**cfg_reserved509** Default Value: 0b cfg_reserved509_defaultreset Access: RO Power well:DIG
	26	**cfg_od_clktop1_coreclkc_bypass** Default Value: 0b cfg_od_clktop1_coreclkc_bypass_defaultreset Access: R/W bypass enable of coreclkc to take input refclk
	25	**cfg_od_clktop1_coreclkc_divretimeren_h** Default Value: 1b cfg_od_clktop1_coreclkc_divretimeren_h_defaultreset Access: R/W retimer enable: 0 for odd division ratio, 1 for even division ratio
	24	**cfg_reserved510** Default Value: 0b cfg_reserved510_defaultreset Access: RO Power well:DIG
	23:16	**cfg_od_clktop1_coreclkb_divratio_7_0** Default Value: 08h cfg_od_clktop1_coreclkb_divratio_7_0_defaultreset Access: R/W divider ratio for coreclkb divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255

DKLP_CMN_ANA_CMN_ANA_DWORD1

		8'h10: USB3.1 gen2 312.5MHz
	15:8	**cfg_od_clktop1_coreclka_divratio_7_0** Default Value: 14h cfg_od_clktop1_coreclka_divratio_7_0_defaultreset Access: R/W divider ratio for coreclka divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255 8'h28: USB3.1 gen1 125MHz
	7	**cfg_on_pll12coreclkd_select** Default Value: 0b cfg_on_pll12coreclkd_select_defaultreset Access: R/W this bit is used to select from pll1_coreclkd and pll2_coreclkd for pll12coreclkd.
	6	**cfg_on_pll12coreclka_select** Default Value: 0b cfg_on_pll12coreclka_select_defaultreset Access: R/W this bit is used to select from pll1_coreclkc and pll2_coreclka for pll12coreclka.
	5	**cfg_od_clktop1_coreclkb_bypass** Default Value: 0b cfg_od_clktop1_coreclkb_bypass_defaultreset Access: R/W bypass enable of coreclkb to take input refclk
	4	**cfg_od_clktop1_coreclkb_divretimeren_h** Default Value: 1b cfg_od_clktop1_coreclkb_divretimeren_h_defaultreset Access: R/W retimer enable: 0 for odd division ratio, 1 for even division ratio
	3	**cfg_reserved506** Default Value: 0b cfg_reserved506_defaultreset Access: RO Power well:DIG
	2	**cfg_od_clktop1_coreclka_bypass** Default Value: 0b cfg_od_clktop1_coreclka_bypass_defaultreset Access: R/W bypass enable of coreclka to take input refclk
	1	**cfg_od_clktop1_coreclka_divretimeren_h** Default Value: 1b cfg_od_clktop1_coreclka_divretimeren_h_defaultreset Access: R/W retimer enable: 0 for odd division ratio, 1 for even division ratio
	0	**cfg_reserved507** Default Value: 0b cfg_reserved507_defaultreset Access: RO Power well:DIG

DKLP_CMN_ANA_CMN_ANA_DWORD5

DKLP_CMN_ANA_CMN_ANA_DWORD5

Register Space: MMIO: 0/2/0

Size (in bits): 32

CLKTOP2_HSCLKCTL

DWord	Bit	Description
0	31:27	**cfg_reserved524** Default Value: 00h cfg_reserved524_defaultreset Access: RO Power well:DIG
	26:25	**cfg_od_clktop2_clkobs_inputsel_1_0** Default Value: 00b cfg_od_clktop2_clkobs_inputsel_1_0_defaultreset Access: R/W mux select for oc_dfx_ck_clk2obs[0] digobs output 2'b00: hsdiv output clock 2'b01: iclk_bypass input from the other clktop 2'b10: dsdiv output clock 2'b11: non-divided pll clock
	24	**cfg_od_clktop2_clk2obs_en_h** Default Value: 0b cfg_od_clktop2_clk2obs_en_h_defaultreset Access: R/W enable of oc_dfx_ck_clk2obs[0] digobs output
	23:22	**cfg_reserved521** Default Value: 00b cfg_reserved521_defaultreset Access: RO Power well:DIG
	21:20	**Reserved**
	19	**cfg_reserved522** Default Value: 0b cfg_reserved522_defaultreset Access: RO Power well:DIG
	18	**cfg_od_clktop2_outclk_bypassen_h** Default Value: 0b cfg_od_clktop2_outclk_bypassen_h_defaultreset Access: R/W enable of div/2 bypass clock output to the other clktop
	17	**cfg_reserved523** Default Value: 0b cfg_reserved523_defaultreset Access: RO Power well:DIG

DKLP_CMN_ANA_CMN_ANA_DWORD5

16	**cfg_od_clktop2_coreclk_inputsel** Default Value: 0b cfg_od_clktop2_coreclk_inputsel_defaultreset Access: R/W mux select for input clock to coreclk divhub. 1'b0: select hsdiv output; 1'b1: select dsdiv output
15:14	**cfg_od_clktop2_tlinedrv_clksel_1_0** Default Value: 00b cfg_od_clktop2_tlinedrv_clksel_1_0_defaultreset Access: R/W mux select for non-dedicated tlinedrv clocks 2'b00: hsclkdiv output 2'b01: dsdiv output clktop 2'b10: iqdiv2 clock 2'b11: iqdiv2clock
13:12	**cfg_od_clktop2_hsdiv_divratio_1_0** Default Value: 00b cfg_od_clktop2_hsdiv_divratio_1_0_defaultreset Access: R/W divider ratio for high speed divider. 2'b00: div/2 HBR3 2'b01: div/3 HBR2/HBR 2'b10: div/5 RBR 2'b11: div/7
11:8	**cfg_od_clktop2_dsdiv_divratio_3_0** Default Value: 1h cfg_od_clktop2_dsdiv_divratio_3_0_defaultreset Access: R/W divider ratio settings for programmable divider: 4'b0000: no division 4'b0001: no division 4'b0010 - 4'b1010: div/2 - div/10 4'b1011 - 4'b1111: not used (div/10)
7	**cfg_od_clktop2_tlinedrv_overrideen** Default Value: 0b cfg_od_clktop2_tlinedrv_overrideen_defaultreset Access: R/W override enable for following 4 tlinedrv enables
6	**cfg_od_clktop2_tlinedrv_enleft_ded_h_ovrd** Default Value: 0b cfg_od_clktop2_tlinedrv_enleft_ded_h_ovrd_defaultreset Access: R/W enable of left side dedicated tlinedrv to output full-rate clock to left lanes
5	**cfg_od_clktop2_tlinedrv_enright_ded_h_ovrd** Default Value: 0b cfg_od_clktop2_tlinedrv_enright_ded_h_ovrd_defaultreset Access: R/W enable of right side dedicated tlinedrv to output full-rate clock to right lanes
4	**cfg_od_clktop2_tlinedrv_enleft_h_ovrd** Default Value: 1b cfg_od_clktop2_tlinedrv_enleft_h_ovrd_defaultreset Access: R/W enable of left side tlinedrv to output divided clock to left lanes
3	**cfg_od_clktop2_tlinedrv_enright_h_ovrd** Default Value: 1b cfg_od_clktop2_tlinedrv_enright_h_ovrd_defaultreset Access: R/W enable of right side tlinedrv to output divided clock to right lanes

DKLP_CMN_ANA_CMN_ANA_DWORD5

	2	**cfg_od_clktop2_dsdiv_en_h** Default Value: 1b cfg_od_clktop2_dsdiv_en_h_defaultreset Access: R/W enable of programmable divider to generate up to div/40 clock working with two iqdivs
	1	**cfg_reserved520** Default Value: 0b cfg_reserved520_defaultreset Access: RO Power well:DIG
	0	**cfg_od_clktop2_hsdiv_en_h** Default Value: 1b cfg_od_clktop2_hsdiv_en_h_defaultreset Access: R/W enable of high speed clock divider

DKLP_CMN_ANA_CMN_ANA_DWORD6

DKLP_CMN_ANA_CMN_ANA_DWORD6

Register Space: MMIO: 0/2/0

Size (in bits): 32

CLKTOP2_CORECLKCTL1

DWord	Bit	Description
0	31:30	**cfg_reserved528** Default Value: 00b cfg_reserved528_defaultreset Access: RO Power well:DIG
	29	**cfg_od_clktop2_coreclkd_bypass** Default Value: 0b cfg_od_clktop2_coreclkd_bypass_defaultreset Access: R/W bypass enable of coreclkd mux to take input as refclk instead of respective coreclk. When bypass_enable is high, refclk becomes the coreclk.
	28	**cfg_od_clktop2_coreclkd_divretimeren_h** Default Value: 1b cfg_od_clktop2_coreclkd_divretimeren_h_defaultreset Access: R/W used to enable or bypass the retimer path for coreclk. 1: enable the retimer path 0: bypass the retimer path (POR)
	27	**cfg_reserved529** Default Value: 0b cfg_reserved529_defaultreset Access: RO Power well:DIG
	26	**cfg_od_clktop2_coreclkc_bypass** Default Value: 0b cfg_od_clktop2_coreclkc_bypass_defaultreset Access: R/W bypass enable of coreclkc mux to take input as refclk instead of respective coreclk. When bypass_enable is high, refclk becomes the coreclk.
	25	**cfg_od_clktop2_coreclkc_divretimeren_h** Default Value: 0b cfg_od_clktop2_coreclkc_divretimeren_h_defaultreset Access: R/W used to enable or bypass the retimer path for coreclk. 1: enable the retimer path 0: bypass the retimer path (POR)

DKLP_CMN_ANA_CMN_ANA_DWORD6

24	**cfg_reserved530** Default Value: 0b cfg_reserved530_defaultreset Access: RO Power well:DIG
23:16	**cfg_od_clktop2_coreclkb_divratio_7_0** Default Value: 08h cfg_od_clktop2_coreclkb_divratio_7_0_defaultreset Access: R/W used to set the divider ratio for coreclkb divider . divider ratio is the decimal equivalent of hex number. 8'h00, 8'h01: div by 1; 8'h02: div by 2; 8'h03: div by3; and so on...
15:8	**cfg_od_clktop2_coreclka_divratio_7_0** Default Value: 05h cfg_od_clktop2_coreclka_divratio_7_0_defaultreset Access: R/W used to set the divider ratio for coreclka divider . divider ratio is the decimal equivalent of hex number. 8'h00, 8'h01: div by 1; 8'h02: div by 2; 8'h03: div by3; and so on...
7:6	**cfg_reserved525** Default Value: 00b cfg_reserved525_defaultreset Access: RO Power well:DIG
5	**cfg_od_clktop2_coreclkb_bypass** Access: R/W bypass enable of coreclkb mux to take input as refclk instead of respective coreclk. When bypass_enable is high, refclk becomes the coreclk.
4	**cfg_od_clktop2_coreclkb_divretimeren_h** Default Value: 0b bypass the retimer path Access: R/W used to enable or bypass the retimer path for coreclk. 1: enable the retimer path 0: bypass the retimer path (POR)

DKLP_CMN_ANA_CMN_ANA_DWORD6

	3	**cfg_reserved526** Default Value: 0b cfg_reserved526_defaultreset Access: RO Power well:DIG
	2	**cfg_od_clktop2_coreclka_bypass** Access: R/W bypass enable of coreclka mux to take input as refclk instead of respective coreclk. When bypass_enable is high, refclk becomes the coreclk.
	1	**cfg_od_clktop2_coreclka_divretimeren_h** Access: R/W used to enable or bypass the retimer path for coreclk. 1: enable the retimer path 0: bypass the retimer path (POR)

Value	Name	Description
0b	bypass the retimer path **[Default]**	This is POR.
1b	enable the retimer path	

	0	**cfg_reserved527** Default Value: 0b cfg_reserved527_defaultreset Access: RO Power well:DIG

DKLP_CMN_ANA_CMN_ANA_DWORD7

DKLP_CMN_ANA_CMN_ANA_DWORD7

Register Space: MMIO: 0/2/0

Size (in bits): 32

CLKTOP2_CORECLKCTL2

DWord	Bit	Description
0	31:24	**cfg_od_clktop2_coreclke_divratio_7_0** Default Value: 32h cfg_od_clktop2_coreclke_divratio_7_0_defaultreset Access: R/W divider ratio for coreclke divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255
	23:22	**cfg_reserved531** Default Value: 00b cfg_reserved531_defaultreset Access: RO Power well:DIG
	21	**cfg_od_clktop2_coreclkf_bypass** Default Value: 0b cfg_od_clktop2_coreclkf_bypass_defaultreset Access: R/W bypass enable of coreclkf to take input refclk
	20	**cfg_od_clktop2_coreclkf_divretimeren_h** Default Value: 1b cfg_od_clktop2_coreclkf_divretimeren_h_defaultreset Access: R/W retimer enable: 0 for odd division ratio, 1 for even division ratio
	19	**cfg_reserved532** Default Value: 0b cfg_reserved532_defaultreset Access: RO Power well:DIG
	18	**cfg_od_clktop2_coreclke_bypass** Default Value: 0b cfg_od_clktop2_coreclke_bypass_defaultreset Access: R/W bypass enable of coreclke to take input refclk

DKLP_CMN_ANA_CMN_ANA_DWORD7

	17	**cfg_od_clktop2_coreclke_divretimeren_h** Default Value: 1b cfg_od_clktop2_coreclke_divretimeren_h_defaultreset Access: R/W retimer enable: 0 for odd division ratio, 1 for even division ratio
	16	**cfg_reserved533** Default Value: 0b cfg_reserved533_defaultreset Access: RO Power well:DIG
	15:8	**cfg_od_clktop2_coreclkd_divratio_7_0** Default Value: 32h cfg_od_clktop2_coreclkd_divratio_7_0_defaultreset Access: R/W divider ratio for coreclkd divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255
	7:0	**cfg_od_clktop2_coreclkc_divratio_7_0** Default Value: 05h cfg_od_clktop2_coreclkc_divratio_7_0_defaultreset Access: R/W divider ratio for coreclkc divider 8'h00: div/256 8'h01: div/257 8'h02 - 8'hff: div/2 - div/255 8'h05: HD port

DKLP_CMN_ANA_CMN_ANA_DWORD27

DKLP_CMN_ANA_CMN_ANA_DWORD27

Register Space: MMIO: 0/2/0

Size (in bits): 32

REFCLKIN_CTL

DWord	Bit	Description
0	31:24	**cfg_reserved589** Default Value: 00h cfg_reserved589_defaultreset Access: RO Power well:DIG
	23:16	**cfg_reserved588** Default Value: 00h cfg_reserved588_defaultreset Access: RO Power well:DIG
	15:12	**cfg_reserved587** Default Value: 0h cfg_reserved587_defaultreset Access: RO Power well:DIG
	11	**cfg_od_refclkin2_refclkinjmux** Default Value: 0b cfg_od_refclkin2_refclkinjmux_defaultreset Access: R/W mux select of external injection refclk inputs: 0 to select amonrefclkinj, 1 to select rcomprefclkinj
	10:8	**cfg_od_refclkin2_refclkmux_2_0** Default Value: 011b cfg_od_refclkin2_refclkmux_2_0_defaultreset Access: R/W mux select for refclk output. 3'b000: external injection refclk; 3'b001: xtalinrefclk; 3'b010:mgrefclkin; 3'b011: socrefclk1; 3'100:socrefclk2; 3'b101:socrefclk3; 3'b110:socrefclk4; 3'b111:socrefclk5
	7:6	**cfg_reserved586** Default Value: 00b cfg_reserved586_defaultreset Access: RO Power well:DIG

DKLP_CMN_ANA_CMN_ANA_DWORD27

	5	**cfg_od_pll10p3g_refclkin_genlock_refclksel** Default Value: 0b cfg_od_pll10p3g_refclkin_genlock_refclksel_defaultreset Access: R/W pll10p3g select for refclk for genlock feature.
	4	**cfg_od_pll10g_refclkin_genlock_refclksel** Default Value: 0b cfg_od_pll10g_refclkin_genlock_refclksel_defaultreset Access: R/W pll10g select for refclk for genlock feature.
	3	**cfg_od_refclkin1_refclkinjmux** Default Value: 0b cfg_od_refclkin1_refclkinjmux_defaultreset Access: R/W mux select of external injection refclk inputs: 0 to select amonrefclkinj, 1 to select rcomprefclkinj
	2:0	**cfg_od_refclkin1_refclkmux_2_0** Default Value: 001b cfg_od_refclkin1_refclkmux_2_0_defaultreset Access: R/W mux select for refclk output. 3'b000: external injection refclk; 3'b001: xtalinrefclk; 3'b010:mgrefclkin; 3'b011: socrefclk1; 3'100:socrefclk2; 3'b101:socrefclk3; 3'b110:socrefclk4; 3'b111:socrefclk5

DKLP_CMN_DIG_CMN_DIG_DWORD6

DKLP_CMN_DIG_CMN_DIG_DWORD6

Register Space: MMIO: 0/2/0

Size (in bits): 32

MISC_SUS0

DWord	Bit	Description
0	31:29	**cfg_reserved** Default Value: 000b cfg_reserved_defaultreset Access: R/W Power well:SUS
	28:26	**cfg_os_cfg_imb750select** Default Value: 010b cfg_os_cfg_imb750select_defaultreset Access: R/W Power well:SUS
	25:24	**cfg_os_cfg_imbcompsel_2** Default Value: 00b cfg_os_cfg_imbcompsel_2_defaultreset Access: R/W CMN_DIG::cmn_dig_dword6::os_cfg_imbcompsel_2
	23	**cfg_os_cfg_imbcompsel** Default Value: 1b cfg_os_cfg_imbcompsel_defaultreset Access: R/W Power well:SUS
	22	**cfg_os_cfg_ircomp_ovrd_value** Default Value: 0b cfg_os_cfg_ircomp_ovrd_value_defaultreset Access: R/W Power well:SUS
	21	**cfg_os_cfg_ircomp_ovrd_en** Default Value: 0b cfg_os_cfg_ircomp_ovrd_en_defaultreset Access: R/W Power well:SUS

DKLP_CMN_DIG_CMN_DIG_DWORD6

	20	**cfg_os_cfg_invert_ptrim_ircomp_h** Default Value: 0b cfg_os_cfg_invert_ptrim_ircomp_h_defaultreset Access: R/W Power well:SUS
	19	**cfg_os_cfg_invert_ntrim_ircomp_h** Default Value: 0b cfg_os_cfg_invert_ntrim_ircomp_h_defaultreset Access: R/W Power well:SUS
	18	**cfg_os_cfg_invert_ptrim_h** Default Value: 0b cfg_os_cfg_invert_ptrim_h_defaultreset Access: R/W Power Well:SUS
	17	**cfg_os_cfg_invert_ntrim_h** Default Value: 0b cfg_os_cfg_invert_ntrim_h_defaultreset Access: R/W Power well:SUS
	16	**cfg_os_cfg_invert_ircomp_h** Default Value: 0b cfg_os_cfg_invert_ircomp_h_defaultreset Access: R/W Power well:SUS
	15:14	**cfg_os_susclk_dynclkgate_mode_1_0** Default Value: 00b cfg_os_susclk_dynclkgate_mode_1_0_defaultreset Access: R/W Dynamic Susclk Gating Model Select 00: Susclk gating and CLKREQ Forced High. In this mode the susclk will not be gated under any circumstances and the CLKREQ sent to the ip74pppxdkltypecfamilyew_SOC will be statically forced high. (default) 01: Susclk gating disabled, CLKREQ enabled. In this mode the susclk will not be gated under any circumstances. The CLKREQ sent to the ip74pppxdkltypecfamilyew_SOC will ip74pppxdkltypecfamilyew_toggle based on whether the susclk is needed by the MPHY 10: Susclk gating enabled, CLKREQ disabled (Forced High). In this mode the susclk will be gated during PS3-PS7 when no functions are requesting the susclk. The CLRKEQ sent to the ip74pppxdkltypecfamilyew_SOC will be statically forced high. 11: Susclk gating and CLKREQ enabled (POR Mode). In this mode the susclk will be gated during PS3-PS7 when no functions are requesting the susclk. The CLKREQ sent to the ip74pppxdkltypecfamilyew_SOC will ip74pppxdkltypecfamilyew_toggle based on whether the susclk is needed by the MPHY

DKLP_CMN_DIG_CMN_DIG_DWORD6

13	**cfg_cfg_calclk_srcsel** Default Value: 0b cfg_cfg_calclk_srcsel_defaultreset Access: R/W oa_ck_rxcalclk (Hardcoded to zero always)
12	**cfg_os_cfg_tr2pwr_gating_ctrl** Default Value: 0b cfg_os_cfg_tr2pwr_gating_ctrl_defaultreset Access: R/W Dynamic TR2 Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating.
11	**cfg_os_cfg_cl2pwr_gating_ctrl** Default Value: 0b cfg_os_cfg_cl2pwr_gating_ctrl_defaultreset Access: R/W Dynamic CL2 Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating.
10	**cfg_os_cfg_gaonpwr_gating_ctrl** Default Value: 0b cfg_os_cfg_gaonpwr_gating_ctrl_defaultreset Access: R/W Dynamic gatedAON Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating.
9	**cfg_os_cfg_cl2pwr_pll1en_gating_ctrl** Default Value: 1b cfg_os_cfg_cl2pwr_pll1en_gating_ctrl_defaultreset Access: R/W When enabled CL2 pwr will not turn off if pll1 is enabled. When disabled CL2 will ignore pll1 enable.
8	**cfg_cfg_calclkgate_dis** Default Value: 0b cfg_cfg_calclkgate_dis_defaultreset Access: R/W 0 - enable cal clock gating 1 - disable cal clock gating
7	**cfg_os_cfg_trpwr_gating_ctrl** Default Value: 0b cfg_os_cfg_trpwr_gating_ctrl_defaultreset Access: R/W Dynamic TR Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating.

DKLP_CMN_DIG_CMN_DIG_DWORD6

	6	**cfg_os_cfg_cl1pwr_gating_ctrl** Default Value: 0b cfg_os_cfg_cl1pwr_gating_ctrl_defaultreset Access: R/W Dynamic CL1 Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating.
	5	**cfg_os_cfg_dgpwr_gating_ctrl** Default Value: 0b cfg_os_cfg_dgpwr_gating_ctrl_defaultreset Access: R/W Dynamic DG Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating.
	4:0	**cfg_os_cfg_susclk_delay_5_1** Default Value: 10h cfg_os_cfg_susclk_delay_5_1_defaultreset Access: R/W Susclk Gating Cycle Delay ip74pppxdkltypecfamilyew_Timer When dynamic susclk gating is enabled. When all susclk requests are deasserted, this is the number of susclk cycles that the susclk will remain active before gating.

DKLP_CMN_DIG_CMN_DIG_DWORD29

DKLP_CMN_DIG_CMN_DIG_DWORD29

Register Space: MMIO: 0/2/0

Size (in bits): 32

LDO_VREF_ANA

DWord	Bit	Description
0	31:24	**cfg_reserved551** Default Value: 00h cfg_reserved551_defaultreset Access: RO Power well:SUS
	23:16	**cfg_os_cri_vref_rsrv_7_0** Default Value: 00h cfg_os_cri_vref_rsrv_7_0_defaultreset Access: R/W VREF CBB bonus bits
	15:13	**cfg_os_cri_vref_ref_sel_2_0** Default Value: 000b cfg_os_cri_vref_ref_sel_2_0_defaultreset Access: R/W Select between bg and resistor divider reference voltage
	12	**cfg_reserved549** Default Value: 0b cfg_reserved549_defaultreset Access: RO Power well:SUS
	11:10	**cfg_os_cri_vref_amon_sel_1_0** Default Value: 00b cfg_os_cri_vref_amon_sel_1_0_defaultreset Access: R/W Select voltage for monitor
	9	**cfg_reserved550** Default Value: 0b cfg_reserved550_defaultreset Access: RO Power well:SUS

DKLP_CMN_DIG_CMN_DIG_DWORD29

	8	**cfg_os_cfg_uc_handshake_enabled** Default Value: 0b cfg_os_cfg_uc_handshake_enabled_defaultreset Access: R/W Enables the handshake for the uC to disable the common lane DIG well (see bit0) 0: CMN DIG will power gate without intervention from uC 1: CMN DIG will wait for uC before power gating
	7:4	**cfg_os_cri_vref_nsel_3_0** Default Value: 0h cfg_os_cri_vref_nsel_3_0_defaultreset Access: R/W N select for current turning
	3:1	**cfg_os_cri_vref_rsel_2_0** Default Value: 000b cfg_os_cri_vref_rsel_2_0_defaultreset Access: R/W R select for current turning
	0	**cfg_os_cfg_uc_cmndig_pg_ok** Default Value: 0b cfg_os_cfg_uc_cmndig_pg_ok_defaultreset Access: R/W Indication from the uC that is acceptable to power gate the Common Lane DIG well.

DKLP_CMN_DIG_CMN_DIG_DWORD33

DKLP_CMN_DIG_CMN_DIG_DWORD33

Register Space: MMIO: 0/2/0

Size (in bits): 32

CFG_PWRGATE_LDO_MODE

DWord	Bit	Description
0	31:24	**cfg_reserved558** Default Value: 00h cfg_reserved558_defaultreset Access: RO Power well:DIG
	23:16	**cfg_reserved557** Default Value: 00h cfg_reserved557_defaultreset Access: RO Power well:DIG
	15:13	**cfg_reserved556** Default Value: 000b cfg_reserved556_defaultreset Access: RO Power well:SUS
	12	**cfg_os_cfg_tr_powergate_ldo_mode** Default Value: 0b cfg_os_cfg_tr_powergate_ldo_mode_defaultreset Access: R/W cfg powergate ldo mode for tr
	11	**cfg_os_cfg_tr2_powergate_ldo_mode** Default Value: 0b cfg_os_cfg_tr2_powergate_ldo_mode_defaultreset Access: R/W cfg powergate ldo mode for tr2
	10	**cfg_os_cfg_cl1_powergate_ldo_mode** Default Value: 0b cfg_os_cfg_cl1_powergate_ldo_mode_defaultreset Access: R/W cfg powergate ldo mode for cl1

DKLP_CMN_DIG_CMN_DIG_DWORD33		
	9	**cfg_os_cfg_cl2_powergate_ldo_mode** Default Value: 0b cfg_os_cfg_cl2_powergate_ldo_mode_defaultreset Access: R/W cfg powergate ldo mode for cl2
	8	**cfg_os_cfg_dig_powergate_ldo_mode** Default Value: 0b cfg_os_cfg_dig_powergate_ldo_mode_defaultreset Access: R/W cfg powergate ldo mode for dig
	7:0	**cfg_os_cfg_ldo_powerup_timer_7_0** Default Value: 7Dh cfg_os_cfg_ldo_powerup_timer_7_0_defaultreset Access: R/W cfg ldo powerup ip74pppxdkltypecfamilyew_timer

DKLP_CMN_UC_CMN_UC_DWORD27

DKLP_CMN_UC_CMN_UC_DWORD27

Register Space: MMIO: 0/2/0

Size (in bits): 32

CMN_UC::cmn_uc_dword27

DWord	Bit	Description
0	31:29	**cfg_reserved_dw27_2** Default Value: 000b cfg_reserved_dw27_2_defaultreset Access: RO CMN_UC::cmn_uc_dword27::reserved_dw27_2
	28	**cfg_forcepwrpok_req** Default Value: 0b cfg_forcepwrpok_req_defaultreset Access: RO CMN_UC::cmn_uc_dword27::forcepwrpok_req
	27	**cfg_phy_xtensa_ana_restore_done** Default Value: 0b cfg_phy_xtensa_ana_restore_done_defaultreset Access: RO CMN_UC::cmn_uc_dword27::phy_xtensa_ana_restore_done
	26	**cfg_phy_xtensa_unblock_ack** Default Value: 0b cfg_phy_xtensa_unblock_ack_defaultreset Access: RO Reserved
	25	**cfg_phy_xtensa_unblock_req** Default Value: 0b cfg_phy_xtensa_unblock_req_defaultreset Access: RO phy_xtensa_unblock_ack from firmware downloader block.
	24	**cfg_uc_xclkgatedstat** Default Value: 0b cfg_uc_xclkgatedstat_defaultreset Access: RO Phy_xtensa_unblock_request from firmware_downloader block. Can be used by firmware to determine the abort scenario. Cleared on reading this register.

DKLP_CMN_UC_CMN_UC_DWORD27

23	**cfg_phy_xtensa_ana_save_done** Default Value: 0b cfg_phy_xtensa_ana_save_done_defaultreset Access: RO Status register for xclk gated state. Cleared when xclk_gatedstat_clr bit is set.
22:21	**cfg_phy_xtensa_pllclk_change_req** Default Value: 00b cfg_phy_xtensa_pllclk_change_req_defaultreset Access: RO Consolidated version of all DLs ana save done status. CL should also have all the ana save done bits in RO status.
20	**cfg_phy_xtensa_block_req** Default Value: 0b cfg_phy_xtensa_block_req_defaultreset Access: RO PHY to set this register bit based on internal conditions and Xtensa to poll thru TIE. 0: PLL1 1: PLL2 ConfigID value MSB indicate original or shadow register write. Cleared when pllclk_change_ack is high.
19	**cfg_phy_xtensa_cl_corewell_wake** Default Value: 0b cfg_phy_xtensa_cl_corewell_wake_defaultreset Access: RO Set: When PM_block message is decoded for DEKEL10. Reset: When xtensa_phy_block_ack is 1
18	**cfg_phy_xtensa_sb_trigger_ack** Default Value: 0b cfg_phy_xtensa_sb_trigger_ack_defaultreset Access: RO This is set by CL-corewell wake logic (if it was dynamically power gated before). Cleared when Xtensa read this register.
17	**cfg_phy_xtensa_clk_switch_req** Default Value: 0b cfg_phy_xtensa_clk_switch_req_defaultreset Access: RO PHY to set this register If the request from Xtensa is read, then completion will be loaded in to 32-bit CRI-RO register and this bit is set. If request from Xtensa is write, then as soon as CL-hw sends the request to iosf-sb this bit is set. This bit is cleared when trigger_req is 1 -> 0.
16	**cfg_trigger_xtensa_to_start_restore** Default Value: 1b cfg_trigger_xtensa_to_start_restore_defaultreset Access: RO PHY has a need to switch clock source to Xtensa due to external conditions. 1: Indication to uC about its own clock switch. uC to move to idle and respond with ack. Cleared when the clk switching is complete.

DKLP_CMN_UC_CMN_UC_DWORD27

15	**cfg_uc_health** Default Value: 0b cfg_uc_health_defaultreset Access: R/W Set by CL hw after IP_READY is done and restore_b == 0 and internal restore is needed. This acts as trigger for uC to start internal restore process. Set during restore phase. Cleared on PM unblock ack msg.
14:13	**cfg_reseverd_dw27_1** Default Value: 00b cfg_reseverd_dw27_1_defaultreset Access: RO uc_health bit, indicating the firmware is up
12	**cfg_forcepwrpok_ack** Default Value: 0b cfg_forcepwrpok_ack_defaultreset Access: R/W Reserved
11	**cfg_xclkgatedstat_clr** Default Value: 0b cfg_xclkgatedstat_clr_defaultreset Access: R/W xclk gated status bit, used after coming back from clock gating. cleared on falling edge of xclk_gatedstat.
10	**cfg_xtensa_phy_send_block_nak** Default Value: 0b cfg_xtensa_phy_send_block_nak_defaultreset Access: R/W 0: No action 1: CL fsm can send NAK response to PM-REQ block message without delay. This bit can be set by Xtensa in ip74pppxdkltypecfamilyew_SOC where block message requires either ACK or NAK response without delay. ip74pppxdkltypecfamilyew_soc mode this bit is never set thus allowing CL logic/Xtensa to do DRAM save. This can be set by Xtensa if PM-REQ response delay is not tolerated by Punit. Cleared on falling edge of phy_block_req.
9	**cfg_xtensa_phy_block_ack** Default Value: 1b cfg_xtensa_phy_block_ack_defaultreset Access: R/W Once Xtensa takes control, it can SET the bit to ensure all housekeeping is done before PM-REQ is allowed to be responded 1: CL fsm can send block ack based on other internal conditions (like firmware download in progress) 0: CL fsm should look for Xtensa_phy_send_block_NAK to take further action for PM_REQ message in processing. this is cleared after DRAM save is done and phy_xtensa_block_req is TRUE. This is cleared by Xtensa after internal housekeeping is done. Cleared on falling edge of phy_block_req.

DKLP_CMN_UC_CMN_UC_DWORD27

	8	**cfg_xtensa_phy_sb_trigger_req** Default Value: 0b cfg_xtensa_phy_sb_trigger_req_defaultreset Access: R/W
	7:6	**cfg_xtensa_phy_pllclk_change_ack** Default Value: 00b cfg_xtensa_phy_pllclk_change_ack_defaultreset Access: R/W Xtensa has done PLL configuration writes in to main bank or shadow bank (depending on configID value). This bit is cleared after Phy_xtensa_pllclk_change_req is 0. 0: PLL1 1: PLL2
	5	**cfg_xtensa_phy_cl_corewell_pg_ok** Default Value: 1b cfg_xtensa_phy_cl_corewell_pg_ok_defaultreset Access: R/W Xtensa allows CL-sus-fsm to power gate CL-corewell. Other PG-entry conditions are decided by CL-logic. Default is CL-corewell power gating allowed. This bit gets cleared if any interrupt comes. Firmware needs to set it when it is ok to power gate. This bit is regular CRI domain flop and not saved.
	4	**cfg_xtensa_phy_clk_switch_ack** Default Value: 0b cfg_xtensa_phy_clk_switch_ack_defaultreset Access: R/W Xtensa has reduced pending external dependencies and ok for clock source switch. Cleared on falling edge of clk_switch_req.
	3	**cfg_xtensa_int_restore_done** Default Value: 0b cfg_xtensa_int_restore_done_defaultreset Access: R/W This is used in CL-fsm to notify ACU/DL to start internal ANA-restore if needed. Applicable for phy mode and used along with restore_b of 0. 1: Internal restore done for both CL/DL 0: Internal restore not done. This bit is cleared after unblock PM-ACK is sent out to PMC.
	2	**cfg_anasave_at_pm_req** Default Value: 1b cfg_anasave_at_pm_req_defaultreset Access: R/W Abutted to all DLs. Used along with PM_REQ block message. Once Xtensa takes control, it can clear/set this bit to either bypass ANA snapshot trigger or allow. Default is bypass as power gating of DL by ip74pppxdkltypecfamilyew_soc would erase the ANA register contents. 1: DL ACU fsm will trigger ANA-snap shot during save op. 0: DL ACU fsm should bypass ANA-snap shot during external or internal save. Set/Cleared by firmware

DKLP_CMN_UC_CMN_UC_DWORD27

	1	**cfg_xtensa_ok4_pll_disable** Default Value: 0b cfg_xtensa_ok4_pll_disable_defaultreset Access: R/W Set by Xtensa: If PLL is enabled forcefully and ok to be disabled to save power. cleared when the clock is gated.
	0	**cfg_xtensa_ok4_cg** Default Value: 0b cfg_xtensa_ok4_cg_defaultreset Access: R/W If xtensa is idle for X clocks and ok to gate its clock. RUNSTALL is applied prior to clock gate properly followed by explicit clock gating at source. cleared when the clock is gated.

DKLP_CMN_UC_CMN_UC_DWORD30

DKLP_CMN_UC_CMN_UC_DWORD30		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
CMN_UC::cmn_uc_dword30		
DWord	**Bit**	**Description**
0	31:0	**cfg_scratch_reg** Default Value: 00000080h cfg_scratch_reg_defaultreset Access: R/W Used by firmware as a scratch register

DKLP_CMN2_DIG_CMN_DIG_DWORD0

DKLP_CMN2_DIG_CMN_DIG_DWORD0

Register Space: MMIO: 0/2/0

Size (in bits): 32

UC_INTR

DWord	Bit	Description
0	31:18	**cfg_reserved** Default Value: 0000h cfg_reserved_defaultreset Access: RO CMN2_DIG::cmn_dig_dword0::reserved
	17:16	**cfg_i_csr_cmn_pll_mux_select_ovrd_val** Default Value: 00b cfg_i_csr_cmn_pll_mux_select_ovrd_val_defaultreset Access: R/W Power Well:SUS
	15	**cfg_i_csr_cmn_dl_corepwr_ack_mask** Default Value: 1b cfg_i_csr_cmn_dl_corepwr_ack_mask_defaultreset Access: R/W Power Well:SUS
	14	**cfg_i_csr_cmn_pll_mux_select_ovrd_en** Default Value: 0b cfg_i_csr_cmn_pll_mux_select_ovrd_en_defaultreset Access: R/W Power Well:SUS
	13	**cfg_i_csr_cmn_clk_policy_ovrd_en** Default Value: 0b cfg_i_csr_cmn_clk_policy_ovrd_en_defaultreset Access: R/W Power well:SUS
	12:9	**cfg_i_csr_cmn_clk_policy_mask** Default Value: 0h cfg_i_csr_cmn_clk_policy_mask_defaultreset Access: R/W Power well:SUS

DKLP_CMN2_DIG_CMN_DIG_DWORD0

	8	**cfg_id_csr_cmn_uc_sideclk_div_select** Default Value: 0b cfg_id_csr_cmn_uc_sideclk_div_select_defaultreset Access: R/W Power well:SUS
	7	**cfg_os__cmn_cri_intr_trigger** Default Value: 0b cfg_os__cmn_cri_intr_trigger_defaultreset Access: R/W trigger interrupt status
	6	**cfg_os_cmn_cri_intr_rcomp_done** Default Value: 0b cfg_os_cmn_cri_intr_rcomp_done_defaultreset Access: R/W uc interrupt. 1: clear rcomp done. 0: update rcomp done
	5	**cfg_os_cmn_cri_intr_cmn_rst_l** Default Value: 0b cfg_os_cmn_cri_intr_cmn_rst_l_defaultreset Access: R/W uc interrupt. 1: clear cmnrst. 0: update cmnrst
	4	**cfg_os_cmn_cri_intr_procmon_done** Default Value: 0b cfg_os_cmn_cri_intr_procmon_done_defaultreset Access: R/W uc interrupt. 1: clear procmon. 0: update procmon
	3	**cfg_os_cmn_cri_intr_pll1_en** Default Value: 0b cfg_os_cmn_cri_intr_pll1_en_defaultreset Access: R/W uc interrupt, 1: clear pll1 enable. 0: update pll1 enable
	2	**cfg_os_cmn_cri_intr_pll2_en** Default Value: 0b cfg_os_cmn_cri_intr_pll2_en_defaultreset Access: R/W uc interrupt. 1: clear pll2 enable. 0: update pll2 enable
	1	**cfg_os_cmn_cri_intr_pll1_lock** Default Value: 0b cfg_os_cmn_cri_intr_pll1_lock_defaultreset Access: R/W uc interrupt. 1. clear pll1 lock. 0: update pll1 lock

DKLP_CMN2_DIG_CMN_DIG_DWORD0		
	0	**cfg_os_cmn_cri_intr_pll2_lock** Default Value: 0b cfg_os_cmn_cri_intr_pll2_lock_defaultreset Access: R/W uc interrupt. 1: clear pll2 lock. 0: update pll2 lock

DKLP_PCS_GLUE_PMD_IRQ_VEC_EN

DKLP_PCS_GLUE_PMD_IRQ_VEC_EN		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Enable irq functions within lane		
DWord	**Bit**	**Description**
0	31:0	**cfg_cfg_ecsr_irq_en** Default Value: 00080000h cfg_cfg_ecsr_irq_en_defaultreset Access: R/W PCS_Glue::PMD_IRQ_VEC_EN::cfg_ecsr_irq_en

DKLP_PCS_GLUE_RTT_CR_SPARE

DKLP_PCS_GLUE_RTT_CR_SPARE		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Spare registers for RTTLane		
DWord	**Bit**	**Description**
0	31:0	**cfg_rtt_cr_spare** Default Value: 8048000h cfg_rtt_cr_spare_defaultreset Access: R/W PCS_Glue::RTT_CR_SPARE::rtt_cr_spare

DKLP_PCS_GLUE_TX_DPCNTL0

DKLP_PCS_GLUE_TX_DPCNTL0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Dp control 0 register		
DWord	**Bit**	**Description**
0	31	**cfg_reserved_tx1** Default Value: 0b cfg_reserved_tx1_defaultreset Access: RO reserved fields
	30	**cfg_trainingen_tx1** Default Value: 0b cfg_trainingen_tx1_defaultreset Access: R/W Enable set for programming in Compliance mode
	29	**cfg_pipe_select_tx1** Default Value: 0b cfg_pipe_select_tx1_defaultreset Access: R/W Override this bit to 0 to take the BIOS programmed Values and not pipe
	28	**cfg_slow_trim_enable_tx1** Default Value: 1b cfg_slow_trim_enable_tx1_defaultreset Access: R/W Enable or Disable the slow trim
	27:23	**cfg_shunt_cm_tx1** Default Value: 00h cfg_shunt_cm_tx1_defaultreset Access: R/W Back mode select for the Shunt CM
	22:18	**cfg_shunt_cp_tx1** Default Value: 00h cfg_shunt_cp_tx1_defaultreset Access: R/W Back mode select for the Shunt CP

DKLP_PCS_GLUE_TX_DPCNTL0

	17:13	**cfg_preshoot_control_l0_tx1** Default Value: 00h cfg_preshoot_control_l0_tx1_defaultreset Access: R/W Preshoot Co-efficients
	12:8	**cfg_de_emphasis_control_l0_tx1** Default Value: 00h cfg_de_emphasis_control_l0_tx1_defaultreset Access: R/W De-emphasis co-efficient
	7:3	**cfg_cursor_control_tx1** Default Value: 00h cfg_cursor_control_tx1_defaultreset Access: R/W Back Up mode for Shunt on C0
	2:0	**cfg_vswing_control_tx1** Default Value: 111b cfg_vswing_control_tx1_defaultreset Access: R/W 1. 1V + 0dB (Full Swing) - 3b000 2. 800 mV + 0dB - 3b001 3. 600 mV + 0 dB - 3b100 4. 400 mV + 0dB -3b111

DKLP_PCS_GLUE_TX_DPCNTL1

DKLP_PCS_GLUE_TX_DPCNTL1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Dp control 1 register		
DWord	**Bit**	**Description**
0	31	**cfg_reserved_tx2** Default Value: 0b cfg_reserved_tx2_defaultreset Access: RO reserved fields
	30	**cfg_trainingen_tx2** Default Value: 0b cfg_trainingen_tx2_defaultreset Access: R/W Enable set for programming in Compliance mode
	29	**cfg_pipe_select_tx2** Default Value: 0b cfg_pipe_select_tx2_defaultreset Access: R/W Override this bit to 0 to take the BIOS programmed Values and not pipe
	28	**cfg_slow_trim_enable_tx2** Default Value: 1b cfg_slow_trim_enable_tx2_defaultreset Access: R/W Enable or Disable the slow trim
	27:23	**cfg_shunt_cm_tx2** Default Value: 00h cfg_shunt_cm_tx2_defaultreset Access: R/W Back mode select for the Shunt CM
	22:18	**cfg_shunt_cp_tx2** Default Value: 00h cfg_shunt_cp_tx2_defaultreset Access: R/W Back mode select for the Shunt CP

DKLP_PCS_GLUE_TX_DPCNTL1

	17:13	**cfg_preshoot_control_l0_tx2** Default Value: 00h cfg_preshoot_control_l0_tx2_defaultreset Access: R/W Preshoot Co-efficients
	12:8	**cfg_de_emphasis_control_l0_tx2** Default Value: 00h cfg_de_emphasis_control_l0_tx2_defaultreset Access: R/W De-emphasis co-efficient
	7:3	**cfg_cursor_control_tx2** Default Value: 00h cfg_cursor_control_tx2_defaultreset Access: R/W Back Up mode for Shunt on C0
	2:0	**cfg_vswing_control_tx2** Default Value: 111b cfg_vswing_control_tx2_defaultreset Access: R/W 1. 1V + 0dB (Full Swing) - 3b000 2. 800 mV + 0dB - 3b001 3. 600 mV + 0 dB - 3b100 4. 400 mV + 0dB -3b111

DKLP_PCS_GLUE_TX_DPCNTL2

DKLP_PCS_GLUE_TX_DPCNTL2

Register Space: MMIO: 0/2/0

Size (in bits): 32

Dp control 2 register

DWord	Bit	Description
0	31:13	**cfg_reserved_dp3** Default Value: 000000h cfg_reserved_dp3_defaultreset Access: RO PCS_Glue::TX_DPCNTL2::reserved_dp3
	12	**loadgen_sharing_pmd_disable** Access: R/W For DP1p62, HDMI5p94: This bit is used if we want to fall-back to older logic where no loadgen sharing will be there inside PMD logic by setting this bit to 1. For other modes: This bit can be set to 1 for enabling loadgen sharing feature if needed. Internally its used as inversion for these modes. Value: 0b – Disable **[Default]**; 1b – Enable
	11	**cfg_dp_mode_cg_enable** Access: R/W This bit enables the feature of power saving in non-dp modes by clock gating few clocks in Tx2. To disable this feature we need to program this bit to 0. Value: 1b – Enable **[Default]**; 0b – Disable
	10	**usb3_gen1_2ui_mode_en** Access: R/W This bit is to enable 2UI path to counter the lane2lane skew in USB3.2 Gen1 mode. Value: 1b – Enable **[Default]**; 0b – Disable
	9	**cfg_dp_fifo_depth_tx1** Default Value: 0b cfg_dp_fifo_depth_tx1_defaultreset Access: R/W PCS_Glue::TX_DPCNTL2::dp_fifo_depth_tx1

DKLP_PCS_GLUE_TX_DPCNTL2

8	**cfg_dp_fifo_depth_tx2** Default Value: 0b cfg_dp_fifo_depth_tx2_defaultreset Access: R/W PCS_Glue::TX_DPCNTL2::dp_fifo_depth_tx2
7	**cfg_dp_2ui_4ui_mode_en** Default Value: 0b cfg_dp_2ui_4ui_mode_en_defaultreset Access: R/W 1 - 2ui 0- 4ui
6:5	**cfg_loadgenselect_tx2** Default Value: 00b cfg_loadgenselect_tx2_defaultreset Access: R/W loadgen select for datapath2ui - Look at the sheet for CFG per Tx
4:3	**cfg_loadgenselect_tx1** Default Value: 00b cfg_loadgenselect_tx1_defaultreset Access: R/W loadgen select for datapath2ui - Look at the sheet for CFG per Tx
2	**cfg_dp20bitmode** Default Value: 0b cfg_dp20bitmode_defaultreset Access: R/W 20 bit mode supprot. This will need to be set to 1 if Pipe width does not reflect the 20bit mode
1	**cfg_rate8boverride_enable** Default Value: 0b cfg_rate8boverride_enable_defaultreset Access: R/W 8bit override enable. The pisorate_8b signal is normally decoded from PHYMODE and RATE. When 1, the pisorate_8b signal will take with pisorate8bit_ovrd value.
0	**cfg_rate8boverride** Default Value: 0b cfg_rate8boverride_defaultreset Access: R/W value used for pisorate_8b when pisorate8bit_overden = 1

DKLP_PCS_GLUE_TX1_FW_CALIB

DKLP_PCS_GLUE_TX1_FW_CALIB

Register Space: MMIO: 0/2/0

Size (in bits): 32

Tx2 Fw calib support

DWord	Bit	Description
0	31:8	**cfg_reserved_tx1** Default Value: 000000h cfg_reserved_tx1_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::reserved_tx1
	7	**cfg_cfg_disable_wait_init_periodic** Default Value: 0b cfg_cfg_disable_wait_init_periodic_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::cfg_disable_wait_init_periodic
	6	**cfg_tx1_dcc_cmp** Default Value: 0b cfg_tx1_dcc_cmp_defaultreset Access: RO PCS_Glue::TX1_FW_CALIB::tx1_dcc_cmp
	5	**cfg_cfg_fw_oneshotcal_req_ctrl_val** Default Value: 0b cfg_cfg_fw_oneshotcal_req_ctrl_val_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::cfg_fw_oneshotcal_req_ctrl_val
	4	**cfg_cfg_tx_fw_oneshotcal_req_ctrl_en** Default Value: 0b cfg_cfg_tx_fw_oneshotcal_req_ctrl_en_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::cfg_tx_fw_oneshotcal_req_ctrl_en
	3	**cfg_cfg_tx_pwr_cal_en_ovrd_val** Default Value: 0b cfg_cfg_tx_pwr_cal_en_ovrd_val_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::cfg_tx_pwr_cal_en_ovrd_val

DKLP_PCS_GLUE_TX1_FW_CALIB

	2	**cfg_cfg_tx_pwr_cal_en_ovrd_en** Default Value: 0b cfg_cfg_tx_pwr_cal_en_ovrd_en_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::cfg_tx_pwr_cal_en_ovrd_en
	1	**cfg_cfg_rate_cal_en_ovrd_val** Default Value: 0b cfg_cfg_rate_cal_en_ovrd_val_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::cfg_rate_cal_en_ovrd_val
	0	**cfg_odkl_tx_rate_ana_cal_en** Default Value: 0b cfg_odkl_tx_rate_ana_cal_en_defaultreset Access: R/W PCS_Glue::TX1_FW_CALIB::odkl_tx_rate_ana_cal_en

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD0

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168BF0h-168BF3h
Name:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD0
ShortName:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD0
Reset:	global

DFXMISC 7E

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**cri_dfx_marginmode** Default Value: 0b cri_dfx_marginmode_defaultreset Access: R/W Margin mode. Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
	14:13	**cri_dfx_evenodd_mask** Default Value: 00b cri_dfx_evenodd_mask_defaultreset Access: R/W Even/odd bit select for comparison. 00 : no masking; 01: select odd path and mask the even path; 10: select even path and mask the odd path; 11: reserved;
	12	**dfx_chk_sel** Default Value: 0b dfx_chk_sel_defaultreset Access: R/W This is to select where the rx data is compared. 0 If compared after Kalgin, and rx data is in 10b domain and running on rxsymbclk; 1 if compared after 10b-)8b, the rx data is 8b domain and running on txsymbclk;

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD0

11	**cri_dfx_synchdr_ignore_err** Default Value: 0b cri_dfx_synchdr_ignore_err_defaultreset Access: R/W Ignore Corrected Syncheader Errors. When enabled, the BoB LCE will ignore corrected single-bit syncheader errors in USB3 Gen2. 0: include corrected syncheader errors in errcnt 1: ignore corrected syncheader errors, do not add to errcnt. Applies only to BOB LCE.
10:8	**cri_dfx_maxerrcnt_2_0** Default Value: 000b cri_dfx_maxerrcnt_2_0_defaultreset Access: R/W Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. // 000 : Free running (default) // 001 : 2^16 // 010 : 2^10 // 011 : 2^8 // 100 : 2^4 // 101 : 2^2 // 110 : First Error // 111 : 2^32
7	**dfx_lcerx_dp_mode** Default Value: 0b dfx_lcerx_dp_mode_defaultreset Access: R/W 1= enable lcerx dp mode rxdata from upar sent to pipe as rxdata.
6	**cri_dfx_typec_dp_en** Default Value: 0b cri_dfx_typec_dp_en_defaultreset Access: R/W Enable to support Type-C TX1/TX2 data path in Base LCE. 0: ip74pppxdkltypecfamilyew_Normal LCE operating mode 1: LCE would replicate the lower 20/16b of it's output data on its upper 20/16b data. (16b/20b depends on whether encoder/decoder is bypassed or not)
5	**cri_dfx_eieos_sync_en** Default Value: 0b cri_dfx_eieos_sync_en_defaultreset Access: R/W BoB LCE Training Pattern control. 0: use EIEOS/SYNC + ISI pattern blocks 1: use only EIEOS/SYNC blocks

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD0

4	**cri_dfx_patbuftrainovr** Default Value: 0b cri_dfx_patbuftrainovr_defaultreset Access: R/W Pattern Buffer Training Override. Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
3	**cri_dfx_dword_align_en** Default Value: 0b cri_dfx_dword_align_en_defaultreset Access: R/W Dword align enable. 1: EnableDword 0: No Dword alignment (default)
2	**cri_dfx_patchken** Default Value: 0b cri_dfx_patchken_defaultreset Access: R/W Pattern Checker Enable. 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
1	**cri_dfx_patgenen** Default Value: 0b cri_dfx_patgenen_defaultreset Access: R/W Pattern Generator Enable. This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1: Enable Pattern Generator
0	**lce_en** Default Value: 0b lce_en_defaultreset Access: R/W Enable lce clock gating, must be set to 1'b1 first before lce is used

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168BF4h-168BF7h
Name:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1
ShortName:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1
Reset:	global

DFXPATBUFSIZE

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**dfx_cri__lcerxtrain** Default Value: 0b dfx_cri__lcerxtrain_defaultreset Access: RO Indicates that the LCE RX has received at least 1 training pattern for BASE in non-raw PRBS and PATBUF modes.
	14:12	**cri_dfx_prbspoly_2_0** Default Value: 000b cri_dfx_prbspoly_2_0_defaultreset Access: R/W PRBS Polynomial. Selects the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. For Base: 000 x^16 +x^5 +x^4 +x^3 +1 (USB3/PCIe Scrambler) (8b/16b/32b) 001 x^16 +x^15 +x^13 +x^4 +1 (SATA scrambler) (8b/16b/32b) 010 x^31 +x^28 +1 (8b/16b/32b) 011 x^7 +x^6 +1 (8b/16b/32b) 100 x^7 +x^6 +1 (10b/20b/40b) 101 Reserved 110 Reserved 111 Reserved For BOB: (Only 2 bits 5:4 are used. bit 6 is a don't care): 00 x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 01 x^31 + x^28 + 1 10 x^7 + x^6 + 1 11 Reserved

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1

	11	**cri_dfx_patbuftrain** Default Value: 0b cri_dfx_patbuftrain_defaultreset Access: R/W Pattern Buffer Manual Training. When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
	10	**cri_dfx_clrerrcnt** Default Value: 0b cri_dfx_clrerrcnt_defaultreset Access: R/W Clear Error ip74pppxdkltypecfamilyew_Counter. Resets the Pattern Checker's error ip74pppxdkltypecfamilyew_counter. 0 : Error ip74pppxdkltypecfamilyew_Counter allowed to run (default) 1 : Error ip74pppxdkltypecfamilyew_Counter held in reset
	9	**cri_dfx_lcereset** Default Value: 0b cri_dfx_lcereset_defaultreset Access: R/W Local Compare Engine Reset. Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
	8	**cri_dfx_lcestart** Default Value: 0b cri_dfx_lcestart_defaultreset Access: R/W Local Compare Engine Start. Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
	7	**cri_dfx_xor_data_en** Default Value: 0b cri_dfx_xor_data_en_defaultreset Access: R/W Patbuf data scrambling enable. Setting this bit will XOR the patbuf data with the PRBS pattern selected by cri_dfx_prbspoly. Applies to both Base and BoB pattern buffers. 0: Patbuf data is not scrambled by LFSR 1: Patbuf data is scrambled by selected LFSR pattern

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1

	6	**cri_dfx_last_sym_en** Default Value: 0b cri_dfx_last_sym_en_defaultreset Access: R/W Base Pattern Buffer Repeat Last Symbol. Enabling this mode will cause the Base patbuf to repeat bits [9:0] an extra 4 times at the end of each patbuf loop. 0: Do not repeat last symbol 1: Repeat last symbol 4 times
	5:4	**cri_dfx_patbufsize_1_0** Default Value: 00b cri_dfx_patbufsize_1_0_defaultreset Access: R/W Pattern Buffer Size. Selects how much of the Pattern Buffer to use, which allows for shorter pattern sequences. Base pattern gen: no effect, Base LCE is always 120 bits, 12 symbols. BoB pattern generator: The MSB will always be bit 127. The LSB will depend on this select. 00 : full 4x32b or 8x16b buffer (default) 01 : 3x32b (while in 32b mode), 7x16b (while in 16b mode) 10 : 2x32b (while in 32b mode), 5x16b (while in 16b mode) 11 : 1x32b (while in 32b mode), 3x16b (while in 16b mode)
	3	**cri_dfx_patbufloop** Default Value: 1b cri_dfx_patbufloop_defaultreset Access: R/W Pattern Buffer Looping enable. Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
	2	**cri_dfx_patbufdwidth** Default Value: 0b cri_dfx_patbufdwidth_defaultreset Access: R/W Pattern Buffer Data Width. For Base: Selects between 10/20/40 bit (8b/10b encoder on TX bypassed) or 8/16/32 bit data width for the Pattern Buffer. On the RX path, data is checked before K-align Block only for PRBS, when 10/20/40b mode is selected. 0 : 10/20/40b (default) 1 : 8/16/32b For BOB 0 : TX Block Encoder is bypassed/Data is Checked before RX Block Align, which is supported only in PRBS

<table>
<tr><th colspan="3">DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD1</th></tr>
<tr><td></td><td></td><td>1 : TX Block Encoder is used/Data is Checked after RX Block Align</td></tr>
<tr><td></td><td>1:0</td><td>cri_dfx_lcepatsrc
<table><tr><td>Default Value:</td><td>00b cri_dfx_lcepatsrc_defaultreset</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns.
00 : Pattern Buffer; use LCE default training pattern;
01: Pattern Buffer; use the first 40b of pattern buffer for training.
10: PRBS; use LCE default training pattern;
11: PRBS; use the first 40b of pattern buffer for training.</td></tr>
</table>

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD7

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD7

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168BF8h-168BFBh
Name:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD7
ShortName:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD7
Reset:	global

DFXPRBSSEED1

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:12	**cri_dfx_maxbitcnt_3_0** Default Value: 0h cri_dfx_maxbitcnt_3_0_defaultreset Access: R/W Selectable maximum value that the DFXBITCNT can reach before the Local Compare Engine is automatically stopped. // 000 : Feature is disabled // 1 : 2^13 (4096 words) // 2 : 2^14 (8192 words) // 3 : 2^15 (16384 words) // ... // 13: 2^25 (1.67E7 words) // 14: 2^29 (5.38E8 words) // 15: 2^32 (4.29E9 words)
	11	**cri_dfx_raw_high_16b_sel** Default Value: 0b cri_dfx_raw_high_16b_sel_defaultreset Access: R/W Chooses between upper 16 bits and lower 16bits of the actual and expected data logged to be read out in BOB 32b RX mode. (TBT3) 0: Selects lower 16bits of the expected/actual data in the error logging register 1: Selects upper 16bits of the expected/actual data in the error logging register
	10	**cri_dfx_errlog_freeze** Default Value: 0b cri_dfx_errlog_freeze_defaultreset Access: R/W Error Log register Freeze. This bit will freeze the error logging when in free-running mode so the actual and expected data can be read by software. This bit must be 0 in first-fail mode.

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD7

		This bit must be cleared to capture subsequent errors. This bit has no effect on the error ip74pppxdkltypecfamilyew_counter and only freezes the log registers. This bit applies to both Base and BoB LCE engines. 0: ip74pppxdkltypecfamilyew_Normal operation, log errors 1: Hold error log register values
	9	**cri_dfx_errlog_index** Default Value: 0b cri_dfx_errlog_index_defaultreset Access: R/W Error Log register bank Index. This bit is used to select which error log register bank is read from the Error Log registers. This bit applies to both Base and BoB LCE engines. 0: select bank 0 1: select bank 1
	8	**cri_dfx_errlog_mode** Default Value: 0b cri_dfx_errlog_mode_defaultreset Access: R/W Error Log storage mode. This bit applies to both Base and BoB LCE engines. 0: Capture first two failing cycles, then stop 1: Capture latest two failing cycles, free-running
	7:0	**cri_dfx_prbsseed_39_32** Default Value: 00h cfg_cri_dfx_prbsseed_39_32_defaultreset Access: R/W PRBS seed.

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD8

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD8

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168BFCh-168BFFh
Name:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD8
ShortName:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD8
Reset:	global

DFXPRBSSEED3

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**cri_dfx_prbsseed_23_16** Default Value: FFh cri_dfx_prbsseed_23_16_defaultreset Access: R/W reserved
	7:0	**cri_dfx_prbsseed_31_24** Default Value: FFh cri_dfx_prbsseed_31_24_defaultreset Access: R/W PRBS seed. Can be used for HVM determinism. The use of all zeroes can result in lockup.

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD9

DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD9

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168C00h-168C03h
Name:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD9
ShortName:	DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD9
Reset:	global

DFXPRBSSEED1

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**cri_dfx_prbsseed_7_0** Default Value: FFh cri_dfx_prbsseed_7_0_defaultreset Access: R/W reserved
	7:0	**cri_dfx_prbsseed_15_8** Default Value: FFh cri_dfx_prbsseed_15_8_defaultreset Access: R/W reserved

DKLP_PCS_PCS_DWORD3

DKLP_PCS_PCS_DWORD3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168BE8h-168BEBh
Name:	DKLP_PCS_PCS_DWORD3
ShortName:	DKLP_PCS_PCS_DWORD3
Reset:	global

PRBS

DWord	Bit	Description
0	31:24	**cri_kalign_timer_value_gen1** Default Value: 00h cri_kalign_timer_value_gen1_defaultreset Access: R/W When K-Align timer mode is enabled, this value represents the timer value for Gen1 rates.[3:0] = PS1 timer value. Multiply this value by 32ns[7:4] = Non-PS1 timer value. Multiply this value by 64ns
	23:6	**Reserved** Default Value: 00h Access: RO
	5	**Reserved**
	4	**o_cfg_pcs_dp_calbypass_disable** Access: R/W To disable the DP calbypass. Value: 0b — enable **[Default]** Value: 1b — disble
	3	**o_cri_tx_raw_mode_enable** Access: R/W To enable the PRBS raw mode for TX data. Value: 0b — disable **[Default]** Value: 1b — enable
	2:0	**Reserved**

DKLP_PCS_PCS_DWORD23

DKLP_PCS_PCS_DWORD23		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SET50		
DWord	**Bit**	**Description**
0	31:29	**cfg_reserved583** Default Value: 000b cfg_reserved583_defaultreset Access: RO Reserved
	28:24	**cfg_reserved584** Default Value: 00h cfg_reserved584_defaultreset Access: RO Hysteresis ip74pppxdkltypecfamilyew_timer value for corewell gating. Power gating criteria(expect PMC) must me met for these many susclks before power gating is initiated. Crireg resides in suswell and retained in aonwell.
	23:21	**cfg_reserved581** Default Value: 000b cfg_reserved581_defaultreset Access: RO Reserved
	20:16	**cfg_reserved582** Default Value: 00h cfg_reserved582_defaultreset Access: RO Hysteresis ip74pppxdkltypecfamilyew_timer value for suswell gating. Power gating criteria(expect PMC) must me met for these many susclks before power gating is initiated. Crireg resides in aonwell.
	15:9	**cfg_reserved579** Default Value: 00h cfg_reserved579_defaultreset Access: RO Reserved
	8	**cfg_reserved580** Default Value: 0b cfg_reserved580_defaultreset Access: RO pianclkbufen assertion to rxidle deassertion delay ip74pppxdkltypecfamilyew_timer override

DKLP_PCS_PCS_DWORD23

	7:3	**cfg_reserved578** Default Value: 00h cfg_reserved578_defaultreset Access: RO Reserved
	2	**cfg_cri_disable_powerdown_based_gating** Default Value: 1b cfg_cri_disable_powerdown_based_gating_defaultreset Access: R/W This is for just incase something unexpected happen and internally we powergate in be;ow PS0.
	1	**cfg_reg_rxlpsen_enable_raw_all_powerdown** Default Value: 0b cfg_reg_rxlpsen_enable_raw_all_powerdown_defaultreset Access: R/W When set to 1 raw mode is enabled in all powerdown state. lfpsen from PIPE is passed to RxuP asynchronously.
	0	**cfg_reg_rxlfpsen_use_raw** Default Value: 0b cfg_reg_rxlfpsen_use_raw_defaultreset Access: R/W When set to 1, in PS3 (and above) susclk is not requested. As a result, lfps is not reported on rxelecidle. Additionally lfpsen from PIPE is passed to RxuP asynchronously. Implemented with AON retention.

DKLP_PCS_PCS_DWORD25

DKLP_PCS_PCS_DWORD25

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168BECh-168BEFh
Name:	DKLP_PCS_PCS_DWORD25
ShortName:	DKLP_PCS_PCS_DWORD25
Reset:	global

Used for INDEX_REGISTERS programming, to program DKLP_PCS_INDEXED_PCS_ICL_INDEXED_DWORD* registers.
INDEX 0 refers to DWORD0 and INDEX 63 refers to DWORD63.

DWord	Bit	Description
0	31:24	**dfx_regaccess_31_24** Default Value: 00h dfx_regaccess_31_24_defaultreset Access: R/W Upper 3 bits are RNW(MSB) Bit31 - 0 - Read 1 - Write Bit30 - Byte1_sel Bit29 - Byte0_sel
	23:16	**dfx_regaccess_23_16** Default Value: 00h dfx_regaccess_23_16_defaultreset Access: R/W Lower 6bits i.e., [21:16] are address select
	15:8	**dfx_regaccess_15_8** Default Value: 00h dfx_regaccess_15_8_defaultreset Access: R/W Write or Read Data[15:8]
	7:0	**dfx_regaccess_7_0** Default Value: 00h dfx_regaccess_7_0_defaultreset Access: R/W Write or Read Data[7:0]

DKLP_PLL0_BIAS

DKLP_PLL0_BIAS		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
BIAS Register		
DWord	**Bit**	**Description**
0	31	**cfg_i_tdc_fine_res** Default Value: 1b cfg_i_tdc_fine_res_defaultreset Access: R/W RET DFUSE STRAP TDC fine resolution select 0: Coarse resolution / 8 1: Coarse resolution / 4
	30	**cfg_i_fracnen_h** Default Value: 1b cfg_i_fracnen_h_defaultreset Access: R/W RET DFUSE STRAP Enables fractional modulator. For SSC, this bit needs to be set to '1', even though it starts with integer division ratio. This is not part of direct pin IF. This is only integer to integer with BW optimization across all supported interger divisions or fractional to fractional with small PPM changes. Integer to fractional or vice versa is not supported.
	29:24	**cfg_i_fbdiv_frac_21_16** Default Value: 0Dh cfg_i_fbdiv_frac_21_16_defaultreset Access: R/W RET DFUSE STRAP Fractional Modulator settings
	23:16	**cfg_i_fbdiv_frac_15_8** Default Value: 55h cfg_i_fbdiv_frac_15_8_defaultreset Access: R/W RET DFUSE STRAP Fractional Modulator settings
	15:8	**cfg_i_fbdiv_frac_7_0** Default Value: 55h cfg_i_fbdiv_frac_7_0_defaultreset Access: R/W RET DFUSE STRAP Fractional Modulator settings
	7:0	**cfg_i_sscinj_stepsize_7_0** Default Value: 00h cfg_i_sscinj_stepsize_7_0_defaultreset Access: R/W RET DFUSE SSCInjection Step Size [7:0]

DKLP_PLL0_DIV0

DKLP_PLL0_DIV0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
DIV0 Register		
DWord	**Bit**	**Description**
0	31:30	**cfg_i_truelock_criteria_1_0** Default Value: 01b cfg_i_truelock_criteria_1_0_defaultreset Access: R/W RET DFUSE STRAP True lock indicator criteria. After early lock generation, external PLL lock indicator asserted high when phase error is less than threshold value for 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	29:28	**cfg_i_earlylock_criteria_1_0** Default Value: 11b cfg_i_earlylock_criteria_1_0_defaultreset Access: R/W RET DFUSE STRAP Early lock indicator criteria. Early PLL lock indicator asserted high when phase error is less than threshold value for 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	27:25	**cfg_i_afc_startup_2_0** Default Value: 000b cfg_i_afc_startup_2_0_defaultreset Access: R/W RET DFUSE STRAP This is for AFC start point. NOTE: i_afc_startup[2] - DW4, byte17, bit[0] 000: fine = 511 001: fine = 639 (+128) 010: fine = 767 (+256) 011: fine = 895 (+384) 100: NA 101: fine = 127 (-384) 110: fine = 255 (-256) 111: fine = 383 (-128)
	24	**cfg_i_divretimeren** Default Value: 0b cfg_i_divretimeren_defaultreset Access: R/W RET DFUSE STRAP Retiming of feedback clock
	23:21	**cfg_i_gainctrl_2_0** Default Value: 001b cfg_i_gainctrl_2_0_defaultreset Access: R/W RET DFUSE STRAP Adjustable gain for loop filter. Both coefficients shifted right by gainctrl before lock

DKLP_PLL0_DIV0

	20:16	**cfg_i_int_coeff_4_0** Default Value: 07h cfg_i_int_coeff_4_0_defaultreset Access: R/W RET DFUSE STRAP integral coeff. = 2^(-int_coeff), tageting up to 2^-11
	15:12	**cfg_i_prop_coeff_3_0** Default Value: 3h cfg_i_prop_coeff_3_0_defaultreset Access: R/W RET DFUSE STRAP proportional coeff. = 2^(-prop_coeff+1)
	11:8	**cfg_i_fbprediv_3_0** Default Value: 2h cfg_i_fbprediv_3_0_defaultreset Access: R/W RET DFUSE STRAP predivider ratio 0000,0001 : reserved 0010: /2 0100: /4 0011: reserved Rest: reserved For external IF pin use case with
	7:0	**cfg_i_fbdiv_intgr_7_0** Default Value: 82h cfg_i_fbdiv_intgr_7_0_defaultreset Access: R/W RET DFUSE STRAP Feedback divider post division (M2)

DKLP_PLL0_DIV1

DKLP_PLL0_DIV1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
DIV1 Register		
DWord	**Bit**	**Description**
0	31	**cfg_i_bw_ampmeas_window** Default Value: 0b cfg_i_bw_ampmeas_window_defaultreset Access: R/W RET DFUSE STRAP 0: 10 modulation cycles of averaging for mplitude measurement 1: 20 modulation cycles of averaging for mplitude measurement
	30:29	**cfg_i_bias_calib_stepsize_1_0** Default Value: 00b cfg_i_bias_calib_stepsize_1_0_defaultreset Access: R/W RET DFUSE STRAP Bias Calibration Step Size during linear search 00: 1 01: 2 10: 3 11: 4
	28:24	**cfg_i_ctrim_4_0** Default Value: 0Ch cfg_i_ctrim_4_0_defaultreset Access: R/W RET DFUSE STRAP ip74pppxdkltypecfamilyew_Cap trimming for irefout. This also has refclock dependency. Current default is for 24MHz.
	23	**cfg_i_fastlock_internal_reset** Default Value: 1b cfg_i_fastlock_internal_reset_defaultreset Access: R/W RETCLR DFUSE STRAP clears internal fastlock memory so that next cold start will do both TDC and AFC calibration instead of fast lock. NOTE: this does not clear the i_fastlock_en_h register bit, clears functional register and self-clears Formerly, i_bbthresh[3] (no longer strap)
	22:21	**cfg_i_bias_r_programability_1_0** Default Value: 10b cfg_i_bias_r_programability_1_0_defaultreset Access: R/W RET DFUSE STRAP [1:0] : Bias Filter R programmability - note mapped to bias_bonus[1:0]
	20:16	**cfg_i_ireftrim_4_0** Default Value: 1Ch cfg_i_ireftrim_4_0_defaultreset Access: R/W RET DFUSE STRAP Output current trim . Mirror ratio is changed based on constant current

DKLP_PLL0_DIV1

		requirement. SInce it is refclock dependent, needs to be reconfigurable. i_ireftrim[4:0] - 38.4/19.2 MHz - 5'h1C i_ireftrim[4:0] - 25/100 MHz = 5'h18 Step size: 20 uA
	15	**cfg_i_biasfilter_en_delay** Default Value: 1b cfg_i_biasfilter_en_delay_defaultreset Access: R/W RET DFUSE 0: Filter enabled even before pll enabled 1: Filter enable is delay until lock acquisition This bit is sensitive only when i_bias_filter_en is set (bit3)
	14	**cfg_i_bias_filter_en** Default Value: 1b cfg_i_bias_filter_en_defaultreset Access: R/W RET DFUSE 0: Disables bias filter 1: Enables bias filter
	13	**cfg_i_biascal_en_h** Default Value: 0b cfg_i_biascal_en_h_defaultreset Access: R/W RET DFUSE STRAP Bias Calibration Signal. Bias cal should be disable when override DCO coarse code.
	12	**cfg_i_dcodither_config** Default Value: 0b cfg_i_dcodither_config_defaultreset Access: R/W RET DFUSE Whenever we have binary weighted MFC ip74pppxdkltypecfamilyew_cap, this should be set to 1'b0. Ex: i_dcofine_resolution = 1'b0. For this case, this should be set to 1'b0. 0: No floating dither 1: Floating dither (511+Nobinary - Floating dither)
	11:8	**cfg_i_lockthresh_3_0** Default Value: 5h cfg_i_lockthresh_3_0_defaultreset Access: R/W RET DFUSE STRAP Digital lock detect threshold, the PLL will generate plllockout when the phase error detected by TDC is within lockthresh number of TDC counts for 64 consecutive cycles 5*16 (TDC Code) = 80 (16 is internally hard coded scalar value) - This setting isin middle of coarse range
	7:0	**cfg_i_tdctargetcnt_7_0** Default Value: 11h cfg_i_tdctargetcnt_7_0_defaultreset Access: R/W RET DFUSE STRAP TDC tristate buffer calibration ip74pppxdkltypecfamilyew_counter value. Delay line loop oscillation is counted over two refclk cycles. This is used for TDC coarse code calibration

DKLP_PLL0_FRAC_LOCK

DKLP_PLL0_FRAC_LOCK		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
FRAC_LOCK Register		
DWord	**Bit**	**Description**
0	31:30	**cfg_i_cml2cmosbonus_1_0** Default Value: 00b cfg_i_cml2cmosbonus_1_0_defaultreset Access: R/W RET DFUSE STRAP NOTE: These bits are ported to anatop bit [0] mapped to cml2cmosbonus[1] port - o_plllc_ck_dcocmosclkp_ana disable '1' = o_plllc_ck_dcocmosclkp_ana is disabled (ie for MG B0) '0' = both phases of the cmos clock ip74pppxdkltypecfamilyew_toggle at the interface bit[1] mapped to cml2cmosbonus[2] port - available
	29:27	**cfg_i_bb_gain2_2_0** Default Value: 000b cfg_i_bb_gain2_2_0_defaultreset Access: R/W RET DFUSE STRAP bb_gain2[2:0] : BB gain for second BB range; expect bb_gain2 >= bb_gain1
	26:24	**cfg_i_bb_gain1_2_0** Default Value: 000b cfg_i_bb_gain1_2_0_defaultreset Access: R/W RET DFUSE STRAP BB gain for first BB range
	23	**cfg_i_fastlock_en_h** Default Value: 0b cfg_i_fastlock_en_h_defaultreset Access: R/W RET DFUSE STRAP Enable FLL based AFC; this replaces binary search based AFC. FLL based AFC faster than binary search
	22:19	**cfg_i_fllafc_gain_3_0** Default Value: 8h cfg_i_fllafc_gain_3_0_defaultreset Access: R/W RET DFUSE STRAP Initial FLL gain that decrements down to 1 every refclk cycle in the beginning of FLL based AFC

DKLP_PLL0_FRAC_LOCK

	18:16	**cfg_i_fllafc_lockcnt_2_0** Default Value: 100b cfg_i_fllafc_lockcnt_2_0_defaultreset Access: R/W RET DFUSE STRAP Number of refclk cycles for FLL lock after gain is reduced to 1
	15:8	**cfg_i_max_cselafc_7_0** Default Value: 3Fh cfg_i_max_cselafc_7_0_defaultreset Access: R/W RET DFUSE STRAP Max. AFC code for a given DCO
	7:0	**cfg_i_init_cselafc_7_0** Default Value: 6Ah cfg_i_init_cselafc_7_0_defaultreset Access: R/W RET DFUSE STRAP Initial AFC code for FLL AFC; apply approximate AFC, and starting at closer frequency helps fast/accurate calibration

DKLP_PLL0_LF

DKLP_PLL0_LF		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
LF Register		
DWord	**Bit**	**Description**
0	31	**cfg_i_afc_divratio** Default Value: 0b cfg_i_afc_divratio_defaultreset Access: R/W RET DFUSE STRAP 0: DCO/4 (prediv: 2, Mdithdiv: 2) 1: DCO/8 (prediv: 4 Mdithdiv: 2)
	30:29	**cfg_i_plllock_sel_1_0** Default Value: 00b cfg_i_plllock_sel_1_0_defaultreset Access: R/W RET DFUSE select between lockdetect-based plllock or ip74pppxdkltypecfamilyew_counter based plllock 11: Sticky lock 10: ip74pppxdkltypecfamilyew_Counter-based 01: Lock Detection + ip74pppxdkltypecfamilyew_Counter 00: Lock Detection
	28:24	**cfg_i_bwphase_4_0** Default Value: 00h cfg_i_bwphase_4_0_defaultreset Access: R/W RET DFUSE STRAP Phase amplitude for bandwidth measurement
	23:21	**cfg_i_ft_mode_sel_2_0** Default Value: 010b cfg_i_ft_mode_sel_2_0_defaultreset Access: R/W RET DFUSE STRAP ftmodesel[2:0] : 9b vs 10b finetune selection, lsb0 tuning 3'b000 : 10b Nom -> Dither = LSB0, LSB0 = LSB0 3'b001 : 10b+ -> Dither = LSB+, LSB0 = LSB0+ 3'b010 : 10b- -> Dither = LSB-, LSB0 = LSB0- 3'b011 : 10b DNL -> Dither = LSB01, LSB0 = LSB0+ 3'h1xx: 9b -> Dither = LSB1, LSB0 = N/A
	20:19	**cfg_i_bw_mode_1_0** Default Value: 00b cfg_i_bw_mode_1_0_defaultreset Access: R/W RET DFUSE STRAP 00: No measurement 01: BW measurement 10: BW calibration up to +1 direction 11: BW calibration up to +2 direction
	18:16	**cfg_i_bw_upperbound_2_0** Default Value: 000b cfg_i_bw_upperbound_2_0_defaultreset Access: R/W RET DFUSE STRAP Upper bound setting for BW 000: 0.1MHz 001: 1 MHz 010: 2 MHz 011: 5 MHz 100: 6 MHz 101: 8 MHz 110: 16 MHz 111: 25MHz

DKLP_PLL0_LF

15:13 cfg_i_bw_lowerbound_2_0

Default Value:	000b cfg_i_bw_lowerbound_2_0_defaultreset
Access:	R/W

RET DFUSE STRAP Lower bound setting for BW 000: 0.1MHz 001: 1 MHz 010: 2 MHz 011: 5 MHz 100: 6 MHz 101: 8 MHz 110: 16 MHz 111: 25MHz

12:9 cfg_i_dcoamp_3_0

Default Value:	0h cfg_i_dcoamp_3_0_defaultreset
Access:	R/W

RET DFUSE Amplitude override value for DCO, 0000 is min amplitude, 1111 is max amplitude, applied when i_dcoampovrden_h is high. 4bit is left shifted to generate 6bit code (x4)

8 cfg_i_dcoampovrden_h

Default Value:	0b cfg_i_dcoampovrden_h_defaultreset
Access:	R/W

RET DFUSE DCO amplitude override enable: 0 DCO amplitude set internally (default) 1 DCO amplitude is set by i_dcoamp[3:0]

7:5 cfg_i_bbthresh2_2_0

Default Value:	000b cfg_i_bbthresh2_2_0_defaultreset
Access:	R/W

RET DFUSE STRAP threshold for second (outer) BB range; expect bbthresh2 >= bbthresh1

4:2 cfg_i_bbthresh1_2_0

Default Value:	000b cfg_i_bbthresh1_2_0_defaultreset
Access:	R/W

RET DFUSE STRAP threshold for first (inner) bang-bang (BB) range

1:0 cfg_i_tdc_offset_lock_1_0

Default Value:	00b cfg_i_tdc_offset_lock_1_0_defaultreset
Access:	R/W

RET DFUSE TDC Offset during lock for integer mode

DKLP_PLL0_TDC_COLDST_BIAS

DKLP_PLL0_TDC_COLDST_BIAS

Register Space: MMIO: 0/2/0

Size (in bits): 32

TDC_COLDST_BIAS Register

DWord	Bit	Description
0	31:29	**cfg_i_cloadctrllext_4_2** Default Value: 000b cfg_i_cloadctrllext_4_2_defaultreset Access: R/W RET VFUSE cload control override for H Vernier line. This is applied when i_tdccalexten_h = 1
	28:24	**cfg_i_tribufctrlext_4_0** Default Value: 00h cfg_i_tribufctrlext_4_0_defaultreset Access: R/W RET VFUSE Tribufctrl control override. This is applied when i_tdccalexten_h = 1
	23:16	**cfg_i_dcocoarse_7_0** Default Value: 00h cfg_i_dcocoarse_7_0_defaultreset Access: R/W RET VFUSE STRAP DCO coarse tune frequency value, when dcocoarse_ovrd_h is '1', this input is used to override the value calculated from the Automatic Frequency Calibration (AFC) block
	15:8	**cfg_i_sscstepsize_7_0** Default Value: 13h cfg_i_sscstepsize_7_0_defaultreset Access: R/W RET DFUSE STRAP Fractional value for one SSC frequency step.
	7:0	**cfg_i_feedfwrdgain_7_0** Default Value: 1Ch cfg_i_feedfwrdgain_7_0_defaultreset Access: R/W RET DFUSE STRAP Feedforwad gain for fractional mode/SSC mode PLL This setting is needed whenever PLL is configured in fractional mode or configured for SSC clock generation.

DKLP_PLL1_BIAS

DKLP_PLL1_BIAS		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
BIAS Register		
DWord	**Bit**	**Description**
0	31	**cfg_i_tdc_fine_res** Default Value: 1b cfg_i_tdc_fine_res_defaultreset Access: R/W RET DFUSE STRAP TDC fine resolution select 0: Coarse resolution / 8 1: Coarse resolution / 4
	30	**cfg_i_fracnen_h** Default Value: 1b cfg_i_fracnen_h_defaultreset Access: R/W RET DFUSE STRAP Enables fractional modulator. For SSC, this bit needs to be set to '1', even though it starts with integer division ratio. This is not part of direct pin IF. This is only integer to integer with BW optimization across all supported interger divisions or fractional to fractional with small PPM changes. Integer to fractional or vice versa is not supported.
	29:24	**cfg_i_fbdiv_frac_21_16** Default Value: 1Eh cfg_i_fbdiv_frac_21_16_defaultreset Access: R/W RET DFUSE STRAP Fractional Modulator settings
	23:16	**cfg_i_fbdiv_frac_15_8** Default Value: 00h cfg_i_fbdiv_frac_15_8_defaultreset Access: R/W RET DFUSE STRAP Fractional Modulator settings
	15:8	**cfg_i_fbdiv_frac_7_0** Default Value: 00h cfg_i_fbdiv_frac_7_0_defaultreset Access: R/W RET DFUSE STRAP Fractional Modulator settings
	7:0	**cfg_i_sscinj_stepsize_7_0** Default Value: 00h cfg_i_sscinj_stepsize_7_0_defaultreset Access: R/W RET DFUSE SSCInjection Step Size [7:0]

DKLP_PLL1_DIV0

DKLP_PLL1_DIV0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
DIV0 Register		
DWord	**Bit**	**Description**
0	31:30	**cfg_i_truelock_criteria_1_0** Default Value: 01b cfg_i_truelock_criteria_1_0_defaultreset Access: R/W RET DFUSE STRAP True lock indicator criteria. After early lock generation, external PLL lock indicator asserted high when phase error is less than threshold value for 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	29:28	**cfg_i_earlylock_criteria_1_0** Default Value: 01b cfg_i_earlylock_criteria_1_0_defaultreset Access: R/W RET DFUSE STRAP Early lock indicator criteria. Early PLL lock indicator asserted high when phase error is less than threshold value for 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	27:25	**cfg_i_afc_startup_2_0** Default Value: 000b cfg_i_afc_startup_2_0_defaultreset Access: R/W RET DFUSE STRAP This is for AFC start point. NOTE: i_afc_startup[2] - DW4, byte17, bit[0] 000: fine = 511 001: fine = 639 (+128) 010: fine = 767 (+256) 011: fine = 895 (+384) 100: NA 101: fine = 127 (-384) 110: fine = 255 (-256) 111: fine = 383 (-128)
	24	**cfg_i_divretimeren** Default Value: 0b cfg_i_divretimeren_defaultreset Access: R/W RET DFUSE STRAP Retiming of feedback clock
	23:21	**cfg_i_gainctrl_2_0** Default Value: 001b cfg_i_gainctrl_2_0_defaultreset Access: R/W RET DFUSE STRAP Adjustable gain for loop filter. Both coefficients shifted right by gainctrl before lock

DKLP_PLL1_DIV0

	20:16	**cfg_i_int_coeff_4_0** Default Value: 07h cfg_i_int_coeff_4_0_defaultreset Access: R/W RET DFUSE STRAP integral coeff. = 2^(-int_coeff), tageting up to 2^-11
	15:12	**cfg_i_prop_coeff_3_0** Default Value: 3h cfg_i_prop_coeff_3_0_defaultreset Access: R/W RET DFUSE STRAP proportional coeff. = 2^(-prop_coeff+1)
	11:8	**cfg_i_fbprediv_3_0** Default Value: 2h cfg_i_fbprediv_3_0_defaultreset Access: R/W RET DFUSE STRAP predivider ratio 0000,0001 : reserved 0010: /2 0100: /4 0011: reserved Rest: reserved For external IF pin use case with
	7:0	**cfg_i_fbdiv_intgr_7_0** Default Value: 69h cfg_i_fbdiv_intgr_7_0_defaultreset Access: R/W RET DFUSE STRAP Feedback divider post division (M2)

DKLP_PLL1_DIV1

DKLP_PLL1_DIV1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
DIV1 Register		
DWord	**Bit**	**Description**
0	31	**cfg_i_bw_ampmeas_window** Default Value: 0b cfg_i_bw_ampmeas_window_defaultreset Access: R/W RET DFUSE STRAP 0: 10 modulation cycles of averaging for mplitude measurement 1: 20 modulation cycles of averaging for mplitude measurement
	30:29	**cfg_i_bias_calib_stepsize_1_0** Default Value: 00b cfg_i_bias_calib_stepsize_1_0_defaultreset Access: R/W RET DFUSE STRAP Bias Calibration Step Size during linear search 00: 1 01: 2 10: 3 11: 4
	28:24	**cfg_i_ctrim_4_0** Default Value: 0Ch cfg_i_ctrim_4_0_defaultreset Access: R/W RET DFUSE STRAP ip74pppxdkltypecfamilyew_Cap trimming for irefout. This also has refclock dependency. Current default is for 24MHz.
	23	**cfg_i_fastlock_internal_reset** Default Value: 1b cfg_i_fastlock_internal_reset_defaultreset Access: R/W RETCLR DFUSE STRAP clears internal fastlock memory so that next cold start will do both TDC and AFC calibration instead of fast lock. NOTE: this does not clear the i_fastlock_en_h register bit, clears functional register and self-clears Formerly, i_bbthresh[3] (no longer strap)
	22:21	**cfg_i_bias_r_programability_1_0** Default Value: 10b cfg_i_bias_r_programability_1_0_defaultreset Access: R/W RET DFUSE STRAP [1:0] : Bias Filter R programmability - note mapped to bias_bonus[1:0]
	20:16	**cfg_i_ireftrim_4_0** Default Value: 1Ch cfg_i_ireftrim_4_0_defaultreset Access: R/W RET DFUSE STRAP Output current trim . Mirror ratio is changed based on constant current

DKLP_PLL1_DIV1

		requirement. SInce it is refclock dependent, needs to be reconfigurable. i_ireftrim[4:0] - 38.4/19.2 MHz - 5'h1C i_ireftrim[4:0] - 25/100 MHz = 5'h18 Step size: 20 uA
	15	**cfg_i_biasfilter_en_delay** Default Value: 1b cfg_i_biasfilter_en_delay_defaultreset Access: R/W RET DFUSE 0: Filter enabled even before pll enabled 1: Filter enable is delay until lock acquisition This bit is sensitive only when i_bias_filter_en is set (bit3)
	14	**cfg_i_bias_filter_en** Default Value: 1b cfg_i_bias_filter_en_defaultreset Access: R/W RET DFUSE 0: Disables bias filter 1: Enables bias filter
	13	**cfg_i_biascal_en_h** Default Value: 0b cfg_i_biascal_en_h_defaultreset Access: R/W RET DFUSE STRAP Bias Calibration Signal. Bias cal should be disable when override DCO coarse code.
	12	**cfg_i_dcodither_config** Default Value: 0b cfg_i_dcodither_config_defaultreset Access: R/W RET DFUSE Whenever we have binary weighted MFC ip74pppxdkltypecfamilyew_cap, this should be set to 1'b0. Ex: i_dcofine_resolution = 1'b0. For this case, this should be set to 1'b0. 0: No floating dither 1: Floating dither (511+Nobinary - Floating dither)
	11:8	**cfg_i_lockthresh_3_0** Default Value: 5h cfg_i_lockthresh_3_0_defaultreset Access: R/W RET DFUSE STRAP Digital lock detect threshold, the PLL will generate plllockout when the phase error detected by TDC is within lockthresh number of TDC counts for 64 consecutive cycles 5*16 (TDC Code) = 80 (16 is internally hard coded scalar value) - This setting isin middle of coarse range
	7:0	**cfg_i_tdctargetcnt_7_0** Default Value: 22h cfg_i_tdctargetcnt_7_0_defaultreset Access: R/W RET DFUSE STRAP TDC tristate buffer calibration ip74pppxdkltypecfamilyew_counter value. Delay line loop oscillation is counted over two refclk cycles. This is used for TDC coarse code calibration

DKLP_PLL1_FRAC_LOCK

DKLP_PLL1_FRAC_LOCK

Register Space: MMIO: 0/2/0

Size (in bits): 32

FRAC_LOCK Register

DWord	Bit	Description
0	31:30	**cfg_i_cml2cmosbonus_1_0** Default Value: 00b cfg_i_cml2cmosbonus_1_0_defaultreset Access: R/W RET DFUSE STRAP NOTE: These bits are ported to anatop bit [0] mapped to cml2cmosbonus[1] port - o_plllc_ck_dcocmosclkp_ana disable '1' = o_plllc_ck_dcocmosclkp_ana is disabled (ie for MG B0) '0' = both phases of the cmos clock ip74pppxdkltypecfamilyew_toggle at the interface bit[1] mapped to cml2cmosbonus[2] port - available
	29:27	**cfg_i_bb_gain2_2_0** Default Value: 000b cfg_i_bb_gain2_2_0_defaultreset Access: R/W RET DFUSE STRAP bb_gain2[2:0] : BB gain for second BB range; expect bb_gain2 >= bb_gain1
	26:24	**cfg_i_bb_gain1_2_0** Default Value: 000b cfg_i_bb_gain1_2_0_defaultreset Access: R/W RET DFUSE STRAP BB gain for first BB range
	23	**cfg_i_fastlock_en_h** Default Value: 0b cfg_i_fastlock_en_h_defaultreset Access: R/W RET DFUSE STRAP Enable FLL based AFC; this replaces binary search based AFC. FLL based AFC faster than binary search
	22:19	**cfg_i_fllafc_gain_3_0** Default Value: 8h cfg_i_fllafc_gain_3_0_defaultreset Access: R/W RET DFUSE STRAP Initial FLL gain that decrements down to 1 every refclk cycle in the beginning of FLL based AFC
	18:16	**cfg_i_fllafc_lockcnt_2_0** Default Value: 100b cfg_i_fllafc_lockcnt_2_0_defaultreset Access: R/W RET DFUSE STRAP Number of refclk cycles for FLL lock after gain is reduced to 1

DKLP_PLL1_FRAC_LOCK		
	15:8	**cfg_i_max_cselafc_7_0** Default Value: 7Fh cfg_i_max_cselafc_7_0_defaultreset Access: R/W RET DFUSE STRAP Max. AFC code for a given DCO
	7:0	**cfg_i_init_cselafc_7_0** Default Value: 6Ah cfg_i_init_cselafc_7_0_defaultreset Access: R/W RET DFUSE STRAP Initial AFC code for FLL AFC; apply approximate AFC, and starting at closer frequency helps fast/accurate calibration

DKLP_PLL1_LF

DKLP_PLL1_LF		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
LF Register		
DWord	**Bit**	**Description**
0	31	**cfg_i_afc_divratio** Default Value: 0b cfg_i_afc_divratio_defaultreset Access: R/W RET DFUSE STRAP 0: DCO/4 (prediv: 2, Mdithdiv: 2) 1: DCO/8 (prediv: 4 Mdithdiv: 2)
	30:29	**cfg_i_plllock_sel_1_0** Default Value: 00b cfg_i_plllock_sel_1_0_defaultreset Access: R/W RET DFUSE select between lockdetect-based plllock or ip74pppxdkltypecfamilyew_counter based plllock 11: Sticky lock 10: ip74pppxdkltypecfamilyew_Counter-based 01: Lock Detection + ip74pppxdkltypecfamilyew_Counter 00: Lock Detection
	28:24	**cfg_i_bwphase_4_0** Default Value: 00h cfg_i_bwphase_4_0_defaultreset Access: R/W RET DFUSE STRAP Phase amplitude for bandwidth measurement
	23:21	**cfg_i_ft_mode_sel_2_0** Default Value: 010b cfg_i_ft_mode_sel_2_0_defaultreset Access: R/W RET DFUSE STRAP ftmodesel[2:0] : 9b vs 10b finetune selection, lsb0 tuning 3'b000 : 10b Nom -> Dither = LSB0, LSB0 = LSB0 3'b001 : 10b+ -> Dither = LSB+, LSB0 = LSB0+ 3'b010 : 10b- -> Dither = LSB-, LSB0 = LSB0- 3'b011 : 10b DNL -> Dither = LSB01, LSB0 = LSB0+ 3'h1xx: 9b -> Dither = LSB1, LSB0 = N/A
	20:19	**cfg_i_bw_mode_1_0** Default Value: 00b cfg_i_bw_mode_1_0_defaultreset Access: R/W RET DFUSE STRAP 00: No measurement 01: BW measurement 10: BW calibration up to +1 direction 11: BW calibration up to +2 direction
	18:16	**cfg_i_bw_upperbound_2_0** Default Value: 000b cfg_i_bw_upperbound_2_0_defaultreset Access: R/W RET DFUSE STRAP Upper bound setting for BW 000: 0.1MHz 001: 1 MHz 010: 2 MHz 011: 5 MHz 100: 6 MHz 101: 8 MHz 110: 16 MHz 111: 25MHz

DKLP_PLL1_LF

	15:13	**cfg_i_bw_lowerbound_2_0** Default Value: 000b cfg_i_bw_lowerbound_2_0_defaultreset Access: R/W RET DFUSE STRAP Lower bound setting for BW 000: 0.1MHz 001: 1 MHz 010: 2 MHz 011: 5 MHz 100: 6 MHz 101: 8 MHz 110: 16 MHz 111: 25MHz
	12:9	**cfg_i_dcoamp_3_0** Default Value: 0h cfg_i_dcoamp_3_0_defaultreset Access: R/W RET DFUSE Amplitude override value for DCO, 0000 is min amplitude, 1111 is max amplitude, applied when i_dcoampovrden_h is high. 4bit is left shifted to generate 6bit code (x4)
	8	**cfg_i_dcoampovrden_h** Default Value: 0b cfg_i_dcoampovrden_h_defaultreset Access: R/W RET DFUSE DCO amplitude override enable: 0 DCO amplitude set internally (default) 1 DCO amplitude is set by i_dcoamp[3:0]
	7:5	**cfg_i_bbthresh2_2_0** Default Value: 000b cfg_i_bbthresh2_2_0_defaultreset Access: R/W RET DFUSE STRAP threshold for second (outer) BB range; expect bbthresh2 >= bbthresh1
	4:2	**cfg_i_bbthresh1_2_0** Default Value: 000b cfg_i_bbthresh1_2_0_defaultreset Access: R/W RET DFUSE STRAP threshold for first (inner) bang-bang (BB) range
	1:0	**cfg_i_tdc_offset_lock_1_0** Default Value: 00b cfg_i_tdc_offset_lock_1_0_defaultreset Access: R/W RET DFUSE TDC Offset during lock for integer mode

DKLP_PLL1_TDC_COLDST_BIAS

DKLP_PLL1_TDC_COLDST_BIAS		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
TDC_COLDST_BIAS Register		
DWord	**Bit**	**Description**
0	31:29	**cfg_i_cloadctrllext_4_2** Default Value: 000b cfg_i_cloadctrllext_4_2_defaultreset Access: R/W RET VFUSE cload control override for H Vernier line. This is applied when i_tdccalexten_h = 1
	28:24	**cfg_i_tribufctrlext_4_0** Default Value: 00h cfg_i_tribufctrlext_4_0_defaultreset Access: R/W RET VFUSE Tribufctrl control override. This is applied when i_tdccalexten_h = 1
	23:16	**cfg_i_dcocoarse_7_0** Default Value: 00h cfg_i_dcocoarse_7_0_defaultreset Access: R/W RET VFUSE STRAP DCO coarse tune frequency value, when dcocoarse_ovrd_h is '1', this input is used to override the value calculated from the Automatic Frequency Calibration (AFC) block
	15:8	**cfg_i_sscstepsize_7_0** Default Value: 0Fh cfg_i_sscstepsize_7_0_defaultreset Access: R/W RET DFUSE STRAP Fractional value for one SSC frequency step.
	7:0	**cfg_i_feedfwrdgain_7_0** Default Value: 23h cfg_i_feedfwrdgain_7_0_defaultreset Access: R/W RET DFUSE STRAP Feedforwad gain for fractional mode/SSC mode PLL This setting is needed whenever PLL is configured in fractional mode or configured for SSC clock generation.

DKLP_PMD_LANE_ANA_CSR_DIG_LFPS_CAL

DKLP_PMD_LANE_ANA_CSR_DIG_LFPS_CAL

Register Space: MMIO: 0/2/0

Size (in bits): 32

PMD_LANE_ANA_CSR::DIG_LFPS_CAL

DWord	Bit	Description
0	31:23	**cfg_reserved1** Default Value: 000h cfg_reserved1_defaultreset Access: R/W PMD_LANE_ANA_CSR::DIG_LFPS_CAL::reserved1
	22	**cfg_filter1** Default Value: 0b cfg_filter1_defaultreset Access: R/W PMD_LANE_ANA_CSR::DIG_LFPS_CAL::filter1
	21	**cfg_osc_dfx_en** Default Value: 0b cfg_osc_dfx_en_defaultreset Access: R/W PMD_LANE_ANA_CSR::DIG_LFPS_CAL::osc_dfx_en
	20:19	**cfg_ck2logic_sel** Default Value: 00b cfg_ck2logic_sel_defaultreset Access: R/W PMD_LANE_ANA_CSR::DIG_LFPS_CAL::ck2logic_sel
	18	**cfg_ck_div_en** Default Value: 1b cfg_ck_div_en_defaultreset Access: R/W PMD_LANE_ANA_CSR::DIG_LFPS_CAL::ck_div_en
	17:12	**cfg_osc_trim** Default Value: 3Fh cfg_osc_trim_defaultreset Access: R/W Reserved

DKLP_PMD_LANE_ANA_CSR_DIG_LFPS_CAL

	11	**cfg_reserved** Default Value: 0b cfg_reserved_defaultreset Access: R/W added by Yoni to provide local fix.
	10:1	**cfg_amon_sel** Default Value: 000h cfg_amon_sel_defaultreset Access: R/W added by Yoni to provide local fix.
	0	**cfg_amon_puldn_en** Default Value: 1b cfg_amon_puldn_en_defaultreset Access: R/W modified by Yoni to provide local fix. originally width 24 RW, reset value - 800FDA

DKLP_PMD_LANE_CDR_CDR_SAVE_RESTORE1

DKLP_PMD_LANE_CDR_CDR_SAVE_RESTORE1		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
PMD_LANE_CDR::CDR_SAVE_RESTORE1		
DWord	**Bit**	**Description**
0	31:28	**cfg_reserved1** Default Value: 0h cfg_reserved1_defaultreset Access: R/W PMD_LANE_CDR::CDR_SAVE_RESTORE1::reserved1
	27:19	**cfg_dco_coarse_backup_sr** Default Value: 000h cfg_dco_coarse_backup_sr_defaultreset Access: R/W this is a save restore register, to save last dco calibration code, for reuse in warm boot.
	18:10	**cfg_dco_coarse_init** Default Value: 098h cfg_dco_coarse_init_defaultreset Access: R/W PMD_LANE_CDR::CDR_SAVE_RESTORE1::dco_coarse_init
	9:5	**cfg_kp_datalock_acq** Default Value: 16h cfg_kp_datalock_acq_defaultreset Access: R/W PMD_LANE_CDR::CDR_SAVE_RESTORE1::kp_datalock_acq
	4:0	**cfg_ki_datalock_acq** Default Value: 18h cfg_ki_datalock_acq_defaultreset Access: R/W PMD_LANE_CDR::CDR_SAVE_RESTORE1::ki_datalock_acq

DKLP_PMD_LANE_SUSWELL_LFPS_SPARE

DKLP_PMD_LANE_SUSWELL_LFPS_SPARE		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
PMD_LANE_SUSWELL::LFPS_SPARE		
DWord	**Bit**	**Description**
0	31:17	**cfg_reserved1** Default Value: 0000h cfg_reserved1_defaultreset Access: R/W Reserved
	16	**cfg_enable_squelch_periodic_cal** Default Value: 0b cfg_enable_squelch_periodic_cal_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::enable_squelch_periodic_cal
	15:11	**cfg_rx_lfps_delay_filter_depth** Default Value: 04h cfg_rx_lfps_delay_filter_depth_defaultreset Access: R/W rx_lfps_delay_filter_depth
	10:9	**cfg_counter_init** Default Value: 00b cfg_counter_init_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::counter_init
	8	**cfg_1ms_timer_en** Default Value: 0b cfg_1ms_timer_en_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::1ms_timer_en
	7	**cfg_rx_lfps_delay_timer_en** Default Value: 0b cfg_rx_lfps_delay_timer_en_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::rx_lfps_delay_timer_en
	6	**cfg_mipi_dif_pn_hs_filt_dis** Default Value: 0b cfg_mipi_dif_pn_hs_filt_dis_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::mipi_dif_pn_hs_filt_dis
	5	**cfg_ecsr_force_val_pmd_txdorxdetect_tx1** Default Value: 0b cfg_ecsr_force_val_pmd_txdorxdetect_tx1_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::ecsr_force_val_pmd_txdorxdetect_tx1

DKLP_PMD_LANE_SUSWELL_LFPS_SPARE		
	4	**cfg_ecsr_force_en_pmd_txdorxdetect_tx1** Default Value: 0b cfg_ecsr_force_en_pmd_txdorxdetect_tx1_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::ecsr_force_en_pmd_txdorxdetect_tx1
	3:0	**cfg_idig_lfps_spare** Default Value: 0h cfg_idig_lfps_spare_defaultreset Access: R/W PMD_LANE_SUSWELL::LFPS_SPARE::idig_lfps_spare

DKLP_PMD_LANE_SUSWELL_TX1_RCV_DETECT_CTRL

DKLP_PMD_LANE_SUSWELL_TX1_RCV_DETECT_CTRL		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
PMD_LANE_SUS_LN0/1::TX1_RCV_DETECT_CTRL		
DWord	**Bit**	**Description**
0	31	**reserved1** Access: RO
	30	**ecsr_tx_rcv_detect_shunt_low_tx1** HASH(0x18841C0)
	29	**ecsr_tx_rcv_detect_shunt_high_tx1** HASH(0x18CD070)
	28:22	**ecsr_tx_rcv_detect_cell_hz_tx1** Default Value: 0x7F HASH(0x188F060)
	21	**Reserved**
	20:19	**ecsr_tx_rcv_detect_fltr_sel_tx1** Default Value: 0x2 wait state during sampling select beween 1,2,3 wait states
	18	**ecsr_tx_rcv_detect_status_force_val_tx1** force detection value
	17	**ecsr_tx_rcv_detect_status_force_en_tx1** force detection value
	16:12	**ecsr_tx_rcv_detect_fsm_force_val_tx1** force rcv detect fsm state
	11	**ecsr_tx_rcv_detect_fsm_force_en_tx1** force rcv detect fsm
	10:4	**ecsr_tx_rcv_detect_cnt_limit_tx1** Default Value: 0x5 count limit of valid to sample tx detect signal
	3	**ecsr_tx_rcv_detect_p_on_high_en_tx1** take detect on high level
	2	**ecsr_tx_rcv_detect_n_on_high_en_tx1** HASH(0x1AC4C40)
	1	**ecsr_tx_rcv_detect_inv_p_ana_sig_tx1** invert analog input
	0	**ecsr_tx_rcv_detect_inv_n_ana_sig_tx1** HASH(0x197E1B0)

DKLP_TX_GLUE_TX_DWORD14

DKLP_TX_GLUE_TX_DWORD14		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
TX related, imported from PMD_LANE_MISC		
DWord	**Bit**	**Description**
0	31:25	**cfg_reserved_1** Default Value: 00h cfg_reserved_1_defaultreset Access: R/W Tx_Glue::tx_dword14::reserved_1
	24:14	**cfg_ecsr_tx_clk_dccdacctrl_offset** Default Value: 000h cfg_ecsr_tx_clk_dccdacctrl_offset_defaultreset Access: R/W reserved
	13	**cfg_ecsr_tx_dccdacenrbp** Default Value: 0b cfg_ecsr_tx_dccdacenrbp_defaultreset Access: R/W if set, chooses coarse step (x2) of dccdacctrl
	12:0	**cfg_ecsr_tx_clk_dccdacctrl** Default Value: 148Ch cfg_ecsr_tx_clk_dccdacctrl_defaultreset Access: R/W ecsr_tx_clk_dccdacctrl

DKLP_TX2_PMD_LANE_MISC_TX1_SPARE

DKLP_TX2_PMD_LANE_MISC_TX1_SPARE		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
TX2_PMD_LANE_MISC::TX1_SPARE		
DWord	**Bit**	**Description**
0	31:8	**cfg_reserved1** Default Value: 000000h cfg_reserved1_defaultreset Access: R/W Reserved
	7:0	**cfg_dig_tx_spare_tx1** Default Value: 0Fh cfg_dig_tx_spare_tx1_defaultreset Access: R/W Spare Config Bits for Tx

DMA Address Register 0 High

DMA_ADDR_0_HIGH - DMA Address Register 0 High

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

The lower 32 bits of the first DMA address register.

Programming Notes

This register is saved in the power context

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24	**Access Region** 0h: Main Memory **[Default]** 1h: SRAM
	23:21	**Reserved** Access: RO Format: MBZ
	20:16	**Address Space** 0h: Normal Memory Access **[Default]** – Use the Per-process GTT if enabled, otherwise uses the Global GTT 7h: WOPCM Access 8h: Global GTT Memory Access **Programming Notes**: This field is ignored if the selected Access Region is SRAM.
	15:0	**Address Upper DWord** Format: GraphicsAddress[47:32]

DMA Address Register 0 Low

DMA_ADDR_0_LOW - DMA Address Register 0 Low		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
The lower 32 bits of the first DMA address register.		
Programming Notes		
This register is saved in the power context		

DWord	Bit	Description
0	31:0	**Address** Format: GraphicsAddress[31:0] This field contains an offset into the associated space or a Graphics Address.

DMA Address Register 1 High

DMA_ADDR_1_HIGH - DMA Address Register 1 High

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

The lower 32 bits of the second DMA address register.

Programming Notes

This register is saved in the power context

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24	**Access Region** 0h: Main Memory **[Default]** 1h: SRAM
	23:21	**Reserved** Access: RO Format: MBZ
	20:16	**Address Space** 0h: Normal Memory Access **[Default]** 7h: WOPCM Access 8h: Global GTT Memory Access **Programming Notes** This field is ignored if the selected Access Region is SRAM.
	15:0	**Address Upper DWord** Format: GraphicsAddress[47:32]

DMA Address Register 1 Low

DMA_ADDR_1_LOW - DMA Address Register 1 Low	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

The lower 32 bits of the second DMA address register.

Programming Notes
This register is saved in the power context

DWord	Bit	Description
0	31:0	**Address** Format: GraphicsAddress[31:0] This field contains an offset into the associated space or a Graphics Address.

DMA Configuration

DMA_CFG - DMA Configuration

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

Programming Notes
This register is saved in the power context. SW shall set bits[1:0] = '00'
Programming of Bits[1:0] are only applies to explicit DMA operation's triggered by FW Or HOST.

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2	**C6 Restore Control** 0h – Active C6 Restore **[Default]** – SRAM contents will be restored as part of the C6 restore. 1h – Lazy C6 Restore – SRAM contents will only be restored on the first active write to the GuC. **Programming Notes**: Hardware restores SRAM contents coming out of RC6 only after a valid kernel has been loaded. If host SW uses DMA to load multiple entities (e.g micro-apps and then kernel), it shall inhibit RC6 entry till the kernel is loaded.
	1	**Main Memory To SRAM Performance Optimization Mode** Mode selection control when bit 0 is set. 0h – **[Default]** – If bit 0 is set, stream writes will be done only uOS/uApp being DMA-ed. 1h – If bit 0 is set, stream writes will be done for all DMA to SRAM. Note that if MinIA is active, this setting can cause writes to be dropped.
	0	**Main Memory To SRAM Performance Optimization** 0h – Reorder Writes **[Default]** – Reorder DMA writes to be in order when DMA'ing from GAM to SRAM. 1h – Stream – Stream DMA writes as the read data comes in. Use the 'tag' field in the read return as the address to SRAM.

DMA Control

DMA_CTRL - DMA Control

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

Programming Notes

This register is saved in the power context
The DMA hardware performs several checks of the parameters provided in the DMA registers before allowing DMA to proceed. These checks are documented in the GuC DMA description PRM section.
If these checks fail then DMA will not start (i.e: it will appear that writes to this register were dropped)

DWord	Bit	Description
0	31:16	**Write Enable Mask** Format: Mask[15:0] A write enable mask for bits 15:0
	15	**Catastrophic Error Encountered during DMA** This bit is set if the DMA transfer encountered a catastrophic fault during its operation. Bit is reset when the next DMA transfer is initiated.
	14:11	**Reserved** Access: RO Format: MBZ
	10	**Last DFX DMA** Allow for SHA to preserve signature between DMA transfers - This feature should be enabled only when DFX PRIMARY Control bit C068[7] is 1 . Dfx now needs to indicate to GUC which is the last DMA in its set of DMA transfers, whose SHA is being accumulated. Dfx will program all these DMAs as uApp at different destination addresses. When Dfx sets this bit along with C314[0], it indicates the last DMA in Dfx's set of DMA transfers.
	9	**Reserved**
	8	**BOOTROM in WOPCM** Allows host to DMA BootROM code to WOPCM region.BootROM code shall be located at offset 0 in GuC's WOPCM regionMode available with fuse_auth_disable == '1'
	7:6	**uApp Index** Specific AppID for one of the 2 uApps, for storing into WOPCM area as destination. Will be only valid when WOPCM is the Destination. Value: [0,1] Name:
	5	**uApp Move** Whether the uApp (index specified the "uApp Index" field) is being moved to WOPCM.

DMA_CTRL - DMA Control

		Programming Notes Must be set only when the DMA is moving uApp Code, and not uOS code.
	4	**uOS Move** Whether the uOS is being moved to WOPCM. **Programming Notes** Must be set only when the DMA is moving uOS Code, and not uApp code.
	3	**DMA Completion Interrupt Enable** Whether an interrupt will be generated when the DMA copy is complete.
	2	**DMA Completion Interrupt Routing** Where the DMA completion interrupt will be routed. **Value** / **Name** / **Description** 0h / Host **[Default]** / Interrupt will be routed to the host CPU. 1h / Reserved / Reserved
	1	**DMA Source** Which DMA address register contains the source of the DMA transfer. **Value** / **Name** / **Description** 0h / Register 0 **[Default]** / Address register 0 is the source of the DMA transfer, address register 1 is the destination. 1h / Register 1 / Address register 1 is the source of the DMA transfer, address register 0 is the destination.
	0	**Start DMA Transfer** This bit should be programmed last since it will trigger the DMA transfer. Hardware will clear this bit once DMA completes.

DMA Copy Size

DMA_COPY_SIZE - DMA Copy Size

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Size of the DMA copy.

Programming Notes

The following rules hold good regarding the uOS and uApp size:

- uOS and uApps sizes are always divisible by 64-bytes.
- uOS and uApps hash value take into account any padding needed for uOS/uApps divisible by 64-byte requirement.

This register is saved in the power context

DWord	Bit	Description
0	31:0	**DMA Transfer Size** **Description** Size of the DMA transfer, in bytes. For smaller transfers SW should use the MinuteIA core directly (DMA programming overhead is higher than copying the data using the MinuteIA core. Approximate inflection point would be ~ 256 bits.)

DMA Global MicroController WOPCM Offset

DMA_GUC_WOPCM_OFFSET - DMA Global MicroController WOPCM Offset

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Programming Notes

The WOPCM space referenced by this base address/offset is not IA visible space. uKernel/uApps are stored here.

This register is required to be programmed before the DMA engine can be invoked to load uKernel (access WOPCM memory). The register is locked after the write - (Write Once).

This register is saved in the power context

DWord	Bit	Description
0	31:14	**GuC WOPCM Offset** Format: WOPCMBaseOffset[31:14] This bit field defines the "GuC WOPCM Start Address" as an 16KB alligned offset from "WOPCM Base".
	13:2	**Reserved** Access: RO Format: MBZ
	1	**Reserved**
	0	**Offset Valid** Reports whether the "GuC WOPCM Offset" is valid and loaded. HW sets this bit when the register is programmed with the GuC WOPCM Offset value.

DMA Microkernel Base

DMA_UOS_BASE - DMA Microkernel Base

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Programming Notes

This register is saved in the power context

DWord	Bit	Description
0	31:6	**Microkernel Base Offset** Format: WOPCMBaseOffset[31:6] This is the value that was programmed by the host. The value is relative to the SRAM base == 0x0 offset in WOPCM.
	5:4	**State of Microkernel** This field is valid only if the "Valid" field (bit 0) is set Value / Name / Description: 0h / In WOPCM **[Default]** / The microkernel is in WOPCM. 1h / In WOPCM and SRAM / The microkernel is in WOPCM and SRAM. 2h / In WOPCM and SRAM and partially SRAM / The microkernel is in WOPCM and partially in SRAM.
	3:1	**Reserved** Access: RO Format: MBZ
	0	**Valid** Format: Boolean Whether a microkernel has been loaded into WOPCM and the hash check has passed.

DMA Microkernel Top

DMA_UOS_TOP - DMA Microkernel Top

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Programming Notes
This register is saved in the power context

DWord	Bit	Description
0	31:6	**Microkernel Top Address** Format: WOPCMBaseOffset[31:6] This value is derived from the initial uOS DMA programming to WOPCM by the host. The value is relative to the SRAM base == 0x0 offset in WOPCM. This offset will point to the beginning of the last cacheline DMA'd.
	5:0	**Reserved** Access: RO Format: MBZ

DMA Protected Range

DPR_0_0_0_PCI - DMA Protected Range

Register Space:	PCI: 0/0/0
Size (in bits):	32
Address:	0005Ch

DMA protected range register.

DWord	Bit	Description
0	31:20	**Top of DPR** Default Value: 000000000000b Access: RO _Custom_GTIReset: BUS RESERVED for DEVICE 2 shadow copy. Device 0 maintains these register bits. Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.
	19:12	**Reserved** Access: RO Format: MBZ
	11:4	**DPRSIZE** Default Value: 00000000b Access: R/W Lock _Custom_GTIReset: BUS This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255MB. The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1. Note: If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or ME stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation or LT NoDMA lookup. Therefore incoming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are OR'ed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all of the above checks must pass before a cycle is allowed to DRAM.
	3	**Reserved** Access: RO Format: MBZ

DPR_0_0_0_PCI - DMA Protected Range

	2	**EPM** Default Value: 0b Access: R/W Lock _Custom_GTIReset: BUS This field controls DMA accesses to the DMA Protected Range (DPR) region. 0: DPR is disabled. 1: DPR is enabled. All DMA requests accessing DPR region are blocked. Dev 0 HW reports the status of DPR enable/disabled through the PRS field in this register.
	1	**Protected Range Status** Default Value: 0b Access: RO _Custom_GTIReset: BUS RESERVED for DEVICE 2 shadow copy. Dev0 maintains this bit. This field indicated the status of DPR. 0: DPR protection disabled. 1: DPR protection enabled.
	0	**Lock** Default Value: 0b Access: R/W Key Lock _Custom_GTIReset: BUS All bits which may be updated by SW in this register are locked down when this bit is set.

Doorbell Control

DOORBELL_CTRL - Doorbell Control

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

Programming Notes
This register is saved in the power context

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24:16	**Write Enable Mask** Format: Mask[8:0] A write enable mask for bits 8:0
	15:9	**Reserved** Access: RO Format: MBZ
	8	**Interrupt Routing** Where interrupts will be routed. 0h – Host **[Default]** – Interrupts will be routed to the host CPU. 1h – Reserved – Reserved
	7	**Doorbell Rung in Group 7** Format: Boolean Whether a doorbell has rung in group 7 (doorbells 224 through 255). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU. 0h – None **[Default]** – No doorbell in the group was rung 1h – Doorbell Rung – A doorbell in the group was rung.
	6	**Doorbell Rung in Group 6** Format: Boolean Whether a doorbell has rung in group 6 (doorbells 192 through 223). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU. 0h – None **[Default]** – No doorbell in the group was rung 1h – Doorbell Rung – A doorbell in the group was rung.

DOORBELL_CTRL - Doorbell Control

5 — Doorbell Rung in Group 5

Format:	Boolean

Whether a doorbell has rung in group 5 (doorbells 160 through 191). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU..

Value	Name	Description
0h	None **[Default]**	No doorbell in the group was rung
1h	Doorbell Rung	A doorbell in the group was rung.

4 — Doorbell Rung in Group 4

Format:	Boolean

Whether a doorbell has rung in group 4 (doorbells 128 through 159). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU.

Value	Name	Description
0h	None **[Default]**	No doorbell in the group was rung
1h	Doorbell Rung	A doorbell in the group was rung.

3 — Doorbell Rung in Group 3

Format:	Boolean

Whether a doorbell has rung in group 3 (doorbells 96 through 127). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU.

Value	Name	Description
0h	None **[Default]**	No doorbell in the group was rung
1h	Doorbell Rung	A doorbell in the group was rung.

2 — Doorbell Rung in Group 2

Format:	Boolean

Whether a doorbell has rung in group 2 (doorbells 64 through 95). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU.

Value	Name	Description
0h	None **[Default]**	No doorbell in the group was rung
1h	Doorbell Rung	A doorbell in the group was rung.

1 — Doorbell Rung in Group 1

Format:	Boolean

Whether a doorbell has rung in group 1 (doorbells 32 through 63). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU.

Value	Name	Description
0h	None **[Default]**	No doorbell in the group was rung
1h	Doorbell Rung	A doorbell in the group was rung.

DOORBELL_CTRL - Doorbell Control

	0	**Doorbell Rung in Group 0** Format: Boolean Whether a doorbell has rung in group 0 (doorbells 0 through 31). This field is written by GTI, or the host CPU. It is cleared by the GuC interrupt hardware, and is read by the host CPU. **Value** / **Name** / **Description** 0h / None **[Default]** / No doorbell in the group was rung 1h / Doorbell Rung / A doorbell in the group was rung.

Doorbell Cookie Register 0..255

DRB0..255COOK - Doorbell Cookie Register 0..255		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 01A00h - 01DFCh		
DWord	**Bit**	**Description**
0	31:0	**Doorbell #0 Cookie Data** Access: R/W _Custom_GTIReset: BUS Value of the cookie data for doorbell.
..	..	..
255	31:0	**Doorbell #255 Cookie Data** Access: R/W _Custom_GTIReset: BUS Value of the cookie data for doorbell.

Doorbell IDI Register

DRBIDI1 - Doorbell IDI Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01988h	
DWord	**Bit**	**Description**
0	31:10	**Reserved** Access: RO Format: MBZ
	9:8	**Doorbell Class of Service** Access: R/W _Custom_GTIReset: BUS Identifies the Class of Service (CLOS) to send with all C2UREQ initiated by doorbell unit. CLOS determines one of 4 possible uses in number of ways of LLC. Since the doorbells are used with only all 16 ways available, these registers should be programmed to match the CLOS which allocates all 16 ways. It is also expected that these values are changed once before any doorbells are armed/active and will stay static for the duration of any test. 00=> MDRB will echo CLOS of 0 with each C2UREQ - DEFAULT 01=> MDRB will echo CLOS of 1 with each C2UREQ 10=> MDRB will echo CLOS of 2 with each C2UREQ 11=> MDRB will echo CLOS of 3 with each C2UREQ
	7:0	**Reserved** Access: RO Format: MBZ

Doorbell Lower Address Register 0..255

DRB0..255REGL - Doorbell Lower Address Register 0..255

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	01000h - 017F8h

DWord	Bit	Description
0	31:6	**Address to be monitored** Access: R/W _Custom_GTIReset: BUS Address to be Monitored: Value of the cacheline address that needs to be monitored. This address has to be HPA in case of 2nd level translations are enabled, else it is GPA.
	5:3	**Reserved** Access: RO Format: MBZ
	2	**RFO request** Access: RO _Custom_GTIReset: BUS RFO request pending: This is a hardware-maintained flag that an RFO (Request for ownership) needs to be sent to BGF. This is set to 1 when Ownership pending is activated and reset to 0 when the RFO is sent to uncore via BGF. This bit is reflected to MMIO else managed within HW.
	1	**Ownership Flow Pending** Access: RO _Custom_GTIReset: BUS Ownership Flow Pending: This is a hardware-maintained flag which would indicate that corresponding flag has lost ownership and pending for RFO. This is set to 1 when RFO is needed through snoop hit or activation of valid and reset to 0 when the RFO is completed (data and response received). It is reflected to MMIO else managed within HW.
	0	**Valid** Access: R/W _Custom_GTIReset: BUS Valid: Determines whether the doorbell is active or not. As part of the register update flow, SW first need to write the upper portion of this register (i.e. 63:32) and update the lower portion along with the VALID flag which activates the monitor system. SW has to clear the contents of this register before allocating a new doorbell.
..	..	..

DRB0..255REGL - Doorbell Lower Address Register 0..255

255	31:6	**Address to be monitored** Access: R/W _Custom_GTIReset: BUS Address to be Monitored: Value of the cacheline address that needs to be monitored. This address has to be HPA in case of 2nd level translations are enabled, else it is GPA.
	5:3	**Reserved** Access: RO Format: MBZ
	2	**RFO request** Access: RO _Custom_GTIReset: BUS RFO request pending: This is a hardware-maintained flag that an RFO (Request for ownership) needs to be sent to BGF. This is set to 1 when Ownership pending is activated and reset to 0 when the RFO is sent to uncore via BGF. This bit is reflected to MMIO else managed within HW.
	1	**Ownership Flow Pending** Access: RO _Custom_GTIReset: BUS Ownership Flow Pending: This is a hardware-maintained flag which would indicate that corresponding flag has lost ownership and pending for RFO. This is set to 1 when RFO is needed through snoop hit or activation of valid and reset to 0 when the RFO is completed (data and response received). It is reflected to MMIO else managed within HW.
	0	**Valid** Access: R/W _Custom_GTIReset: BUS Valid: Determines whether the doorbell is active or not. As part of the register update flow, SW first need to write the upper portion of this register (i.e. 63:32) and update the lower portion along with the VALID flag which activates the monitor system. SW has to clear the contents of this register before allocating a new doorbell.

Doorbell Upper Address Register 0..255

DRB0..255REGU - Doorbell Upper Address Register 0..255

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 01004h - 017FCh

DWord	Bit	Description
0	31:7	**Reserved** Access: RO Format: MBZ
	6:0	**Address to be monitored** Access: R/W _Custom_GTIReset: BUS Upper Address to be Monitored: Value of the cacheline address that needs to be monitored. This address corresponds to address bits [38:32],and has to be HPA in case of 2nd level translations are enabled, else it is GPA.
..	..	..
255	31:7	**Reserved** Access: RO Format: MBZ
	6:0	**Address to be monitored** Access: R/W _Custom_GTIReset: BUS Upper Address to be Monitored: Value of the cacheline address that needs to be monitored. This address corresponds to address bits [38:32],and has to be HPA in case of 2nd level translations are enabled, else it is GPA.

DOUBLE_BUFFER_CTL

DOUBLE_BUFFER_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44500h-44503h
Name:	Double Buffer Control
ShortName:	DOUBLE_BUFFER_CTL
Reset:	soft

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:4	**Reserved** Access: RO Format: MBZ
	3:1	**Reserved** Access: RO Format: MBZ
	0	**Global Double Buffer Update Disable** Description: This field is used to disable double buffer updates for all pipes and transcoders. 0b – Not Disabled 1b – Disabled

DP_TP_CTL

DP_TP_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60540h-60543h
Name:	DisplayPort Transport Control
ShortName:	DP_TP_CTL_A
Reset:	soft
Address:	61540h-61543h
Name:	DisplayPort Transport Control
ShortName:	DP_TP_CTL_B
Reset:	soft
Address:	62540h-62543h
Name:	DisplayPort Transport Control
ShortName:	DP_TP_CTL_C
Reset:	soft
Address:	63540h-63543h
Name:	DisplayPort Transport Control
ShortName:	DP_TP_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**Transport Enable** This bit enables the DisplayPort transport function. Value: 0b – Disable; 1b – Enable
	30	**FEC Enable** Forward Error Correction (FEC) coding for Display Ports (DP). The data M and data N must account for the FEC overhead when FEC is enabled. FEC can only be enabled after DP_TP_CTL isenabled. FEC can only be disabled after DP_TP_CTL is disabled. Value: 0b – disable; 1b – enable

DP_TP_CTL

29:28 **Reserved**

Access:	RO
Format:	MBZ

27 **Transport Mode Select**

This bit selects between DisplayPort SST and MST modes of operation.

This bit must be programmed for all version of displayport protocol.

Value	Name	Description
0b	SST mode	DisplayPort SST mode
1b	MST mode	DisplayPort MST mode

Restriction
The DisplayPort mode (SST or MST) selected here must match the mode selected in the Transcoder DDI Function Control registers for the transcoders attached to this transport. This field must not be changed while the DDI function is enabled.

26 **Reserved**

Access:	RO
Format:	MBZ

25 **Force ACT**

This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again.

Value	Name	Description
0b	Do not force	Do not force ACT to be sent
1b	Force	Force ACT to be sent one time

24:21 **Reserved**

Access:	RO
Format:	MBZ

20:19 **Training Pattern 4 Select**

Value	Name	Description
00b	Training Pattern 4a **[Default]**	**CP2520 Pattern 3**:SR-BS-BS-SR-248 00hs (after data symbol scrambling and ANSI8B/10B coding)
01b	Training Pattern 4b	**CP2520 Pattern 2**:SR-BF-BF-SR-248 00hs (after data symbol scrambling and ANSI8B/10B coding)
10b	Training Pattern 4c	**CP2520 Pattern 1**:SR-CP-CP-SR-248 of 00hs (after data symbol scrambling and ANSI8B/10B coding)
11b	Reserved	

DP_TP_CTL

18 Enhanced Framing Enable

This bit selects enhanced framing for DisplayPort SST.

Hardware internally enables enhanced framing for DisplayPort MST.

Value	Name
0b	Disabled
1b	Enabled

Restriction
In DisplayPort MST mode this bit must be set to Disabled. This field must not be changed while the DDI function is enabled.

17:11 Reserved

Access:	RO
Format:	MBZ

10:8 DP Link Training Enable

These bits are used for DisplayPort link initialization as defined in the DisplayPort specification. During training patterns, hardware will internally manage enabling and disabling of scrambling. Scrambling disable bit will be ignored at that time.
DP_TP_STATUS has an indication that the required number of idle patterns has been sent.

Value	Name	Description
000b	Pattern 1	Training Pattern 1 enabled.
001b	Pattern 2	Training Pattern 2 enabled.
010b	Idle	Idle Pattern enabled.
011b	Normal	Link not in training: Send normal pixels
100b	Pattern 3	Training Pattern 3 enabled.
101b	Pattern 4	Training Pattern 4 enabled.
Others	Reserved	Reserved

Restriction
When enabling or re-enabling the port, it must be turned on with pattern 1 enabled.

7 Reserved

6 Alternate SR Enable

This bit enables the DisplayPort Alternate Scrambler Reset, intended for use only with embedded DisplayPort receivers.

Value	Name
0b	Disable
1b	Enable

DP_TP_CTL		
		Restriction This field must not be changed while the DDI function is enabled.
	5:0	**Reserved** Access: RO Format: MBZ

DP_TP_STATUS

DP_TP_STATUS	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60544h-60547h
Name:	DisplayPort Transport Status
ShortName:	DP_TP_STATUS_A
Reset:	soft
Address:	61544h-61547h
Name:	DisplayPort Transport Status
ShortName:	DP_TP_STATUS_B
Reset:	soft
Address:	62544h-62547h
Name:	DisplayPort Transport Status
ShortName:	DP_TP_STATUS_C
Reset:	soft
Address:	63544h-63547h
Name:	DisplayPort Transport Status
ShortName:	DP_TP_STATUS_D
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**FEC enable live status** Access: RO This bit provides live status of FEC enable/disable in hardware.
	27	**Idle Link Frame Status** Access: R/WC This bit indicates if a link frame boundary has been sent in idle pattern. This is a sticky bit, cleared by writing 1b to it. Value: 0b — Name: Idle link frame not sent Value: 1b — Name: Idle link frame sent

DP_TP_STATUS

26 **Active Link Frame Status**

Access:	R/WC

This bit indicates if a link frame boundary has been sent in active (at least one VC enabled). This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	Active link frame not sent
1b	Active link frame sent

25 **Min Idles Sent**

Access:	RO

This bit indicates that the minimum required number of idle patterns has been sent when DP_TP_CTL is set to send idle patterns. This bit will clear itself when DP_TP_CTL is not longer set to send idle patterns.

Value	Name
0b	Min idles not sent
1b	Min idles sent

24 **ACT Sent Status**

Access:	R/WC

This bit indicates if DisplayPort MST ACT has been sent. This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	ACT not sent
1b	ACT sent

23 **Mode Status**

Access:	RO

This bit indicates what mode the transport is currently in.

Value	Name	Description
0b	SST	Single-stream mode
1b	MST	Multi-stream mode

22 **DP Stream Status**

Access:	RO

Value	Name
0b	Init
1b	Active

21:19 **DP Init Status**

Access:	RO

Value	Name	Description

DP_TP_STATUS

000b	Pattern1	Training Pattern 1
001b	Pattern2	Training Pattern 2
010b	Pattern3	Training Pattern 3
100b	Idle SST	Sending SST Idle Pattern
101b	Idle MST	Sending MST Idle Pattern
110b	Active SST	In Active SST Mode
111b	Active MST	In Active MST Mode
011b	Reserved	Reserved

18:16 **Streams Enabled**

Access:	RO

This field indicates the number of streams (transcoders) enabled on this port during multistream operation. This field should be ignored in single stream mode.

Value	Name
000b	0
001b	1
010b	2
011b	3
100b	4

15:14 **Reserved**

Access:	RO
Format:	MBZ

13:12 **Payload Mapping VC3**

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 3 during multistream operation. This field should be ignored if the number of streams enabled is less than four. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	D	Transcoder D mapped to this VC

11:10 **Reserved**

Access:	RO
Format:	MBZ

DP_TP_STATUS

9:8 Payload Mapping VC2

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 2 during multistream operation. This field should be ignored if the number of streams enabled is less than three. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	D	Transcoder D mapped to this VC

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Payload Mapping VC1

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 1 during multistream operation. This field should be ignored if the number of streams enabled is less than two. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	D	Transcoder D mapped to this VC

3:2 Reserved

Access:	RO
Format:	MBZ

1:0 Payload Mapping VC0

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 0 during multistream operation. This field should be ignored if the number of streams enabled is less than one. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	D	Transcoder D mapped to this VC

DPCLKA_CFGCR0

DPCLKA_CFGCR0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	164280h-164283h
Name:	DPCLKA_CFGCR0
ShortName:	DPCLKA_CFGCR0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28:27	**Reserved** Access: RO Format: MBZ
	26	**Reserved**
	25	**Reserved**
	24	**DDIC Clock Off** This field gates off the clock going to the display engine. 0b: On 1b: Off **[Default]**
	23	**TC6 Clock Off** This field gates off the clock going to the display engine. 0b: On 1b: Off **[Default]**
	22	**TC5 Clock Off** This field gates off the clock going to the display engine. 0b: On 1b: Off **[Default]**
	21	**TC4 Clock Off** This field gates off the clock going to the display engine.

DPCLKA_CFGCR0

	Value / **Name** 0b – On 1b – Off **[Default]**
20	**Reserved**
19	**Reserved**
18	**Reserved**
17	**Reserved**
16	**Reserved**
15	**Reserved**
14	**TC3 Clock Off** This field gates off the clock going to the display engine. **Value** / **Name** 0b – On 1b – Off **[Default]**
13	**TC2 Clock Off** This field gates off the clock going to the display engine. **Value** / **Name** 0b – On 1b – Off **[Default]**
12	**TC1 Clock Off** This field gates off the clock going to the display engine. **Value** / **Name** 0b – On 1b – Off **[Default]**
11	**DDIB Clock Off** This field gates off the DDIB clock going to the display engine. DSI1 clock gating is independent and controlled by the MIPI DSI mode programming. **Value** / **Name** 0b – On 1b – Off **[Default]**
10	**DDIA Clock Off** This field gates off the DDIA clock going to the display engine. DSI0 clock gating is independent and controlled by the MIPI DSI mode programming. **Value** / **Name** 0b – On 1b – Off **[Default]**
9:8	**Reserved**

DPCLKA_CFGCR0

	7:6	**Reserved**
	5:4	**DDIC Clock Select** This field selects which DPLL will drive the port clock for DDIC.

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL4

	3:2	**DDIB Clock Select** This field selects which DPLL will drive the port clock for DDIB and DSI1.

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL4

	1:0	**DDIA Clock Select** This field selects which DPLL will drive the port clock for DDIA and DSI0.

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL4

DPFC_CONTROL_SA

DPFC_CTL_SA - DPFC_CONTROL_SA

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100100h

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**CPUFNCEN** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0: Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer. 1: Display Buffer exists in a CPU fence.
	28:5	**Reserved** Access: RO Format: MBZ
	4:0	**CPUFNCNUM** Default Value: 00h Access: R/W _Custom_GTIReset: BUS This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.

DPFC_CPU_FENCE_OFFSET

DPFC_CFO - DPFC_CPU_FENCE_OFFSET

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100104h

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21:0	**YFNCDISP** Default Value: 000000h Access: R/W _Custom_GTIReset: BUS Y offset from the CPU fence to the Display Buffer base

DPHY_CLK_TIMING_PARAM

DPHY_CLK_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	162180h-162183h
Name:	DPHY 0 Clock Lane Timing Parameter
ShortName:	DPHY_CLK_TIMING_PARAM_0
Reset:	global

Address:	6C180h-6C183h
Name:	DPHY 1 Clock Lane Timing Parameter
ShortName:	DPHY_CLK_TIMING_PARAM_1
Reset:	global

This register specifies the D-PHY timing parameters for the Clock Lane, if SW is overriding the HW defaults.
This register is located within the combo-PHY and is used to apply the overrides to the Clock Lane. The DSI Controller within the Display Core has an identical register (DSI_CLK_TIMING_PARAM) that is used to calculate the transition latencies of the Clock Lane. Both registers should be programmed by Software if an override is to be applied to the Clock Lane.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
The programming of this register must be equal to or less than the programming of its sister register that lives within the Display Core (DSI_CLK_TIMING_PARAM).

DWord	Bit	Description
0	31	**CLK_PREPARE Override** Access: R/W This field controls the override of the CLK-PREPARE timing parameter. Value 0b: HW maintains **[Default]** Value 1b: SW overrides
	30:28	**CLK_PREPARE** Access: R/W This parameter defines the time that the Host drives the Clock Lane with the LP-00 Lane state (the Bridge state) immediately before the HS-0 Line state. This field represents a hexadecimal value with a precision of 1.2 i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency) HW maintains this timing parameter at1 Escape clock (minimum50ns)

DPHY_CLK_TIMING_PARAM

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.00 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 95ns for this parameter.

27 **CLK_ZERO Override**

Access:	R/W

This field controls the override of the CLK-ZERO timing parameter

Value	Name
0	HW Maintains
1	SW overrides

26:24 **Reserved**

Access:	RO
Format:	MBZ

23:20 **CLK_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane.
HW maintains this parameter at 5 Escape clocks (minimum250ns)

19 **CLK_PRE Override**

Access:	R/W

This field controls the override of the CLK-PRE timing parameter.

Value	Name
0	HW Maintains
1	SW overrides

18 **Reserved**

Access:	RO
Format:	MBZ

DPHY_CLK_TIMING_PARAM

	17:16	**CLK_PRE** Access: R/W This parameter defines the time that the HS clock shall be driven by the Host prior to any Data Lane beginning its transition from the LP state to the HS state. HW maintains this parameter at 8 UI (1 Byte clock). This field will override the parameter with a value measured in Escape clocks which will be much greater than 8 UI.
	15	**CLK_POST Override** Access: R/W This field controls the override of the CLK-POST timing parameter Value: 0 — Name: HW Maintains Value: 1 — Name: SW overrides
	14:11	**Reserved** Access: RO Format: MBZ
	10:8	**CLK_POST** Access: R/W This parameter defines the time the Host continues to transmit the HS clock after the last Data Lane has transitioned to the LP state. HW maintains this parameter at 1.25 Escape clocks plus 7 Byte clocks (minimum62.5ns + 56 UI)
	7	**CLK_TRAIL Override** Access: R/W This field controls the override of the CLK-TRAIL timing parameter Value: 0 — Name: HW Maintains Value: 1 — Name: SW overrides
	6:3	**Reserved** Access: RO Format: MBZ
	2:0	**CLK_TRAIL** Access: R/W This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane after the CLK-POST time has been achieved. HW maintains this parameter at 1.25 Escape clocks (minimum 62.5ns)

DPHY_DATA_TIMING_PARAM

DPHY_DATA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	162184h-162187h
Name:	DPHY 0 Data Lane Timing Parameter
ShortName:	DPHY_DATA_TIMING_PARAM_0
Reset:	global

Address:	6C184h-6C187h
Name:	DPHY 1 Data Lane Timing Parameter
ShortName:	DPHY_DATA_TIMING_PARAM_1
Reset:	global

This register specifies the D-PHY timing parameters for the Data Lane, if SW is overriding the HW defaults.
This register is located within the combo-PHY and is used to apply the overrides to the Data Lanes. The DSI Controller within the Display Core has an identical register (DSI_DATA_TIMING_PARAM) that is used to calculate the transition latencies of the Data Lanes. Both registers should be programmed by Software if an override is to be applied to the Clock Lane.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
The programming of this register must be equal to or less than the programming of it's sister register that lives within the Display Core (DSI_DATA_TIMING_PARAM).

DWord	Bit	Description
0	31	**HS_PREPARE Override** Access: R/W This field controls the override of the HS-PREPARE timing parameter. Value 0: HW maintains Value 1: SW overrides
	30:27	**Reserved** Access: RO Format: MBZ
	26:24	**HS_PREPARE** Access: R/W This parameter defines the time that the Host drives a Data Lane with the LP-00 Lane state (the Bridge state) immediately before driving the HS-0 Line state.

DPHY_DATA_TIMING_PARAM

This field represents a hexadecimal value with a precision of 1.2 i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this parameter at 1 Escape clock (minimum 50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.0 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 85ns + 6UI for this parameter.

23 **HS_ZERO Override**

Access:	R/W

This field controls the override of the HS-ZERO timing parameter

Value	Name
0	HW maintains
1	SW overrides

22:20 **Reserved**

Access:	RO
Format:	MBZ

19:16 **HS_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on a Data Lane.
HW maintains this parameter at 2 Escape clocks plus 1 Byte clock (minimum 100ns + 8UI)

15 **HS_TRAIL Override**

Access:	R/W

This field controls the override of the HS-TRAIL timing parameter

Value	Name
0	HW maintains
1	SW overrides

DPHY_DATA_TIMING_PARAM

	14:11	**Reserved** Access: RO Format: MBZ
	10:8	**HS_TRAIL** Access: R/W This parameter defines the time that the Host drives the flipped differential state of the last payload data bit of a HS transmission on a Data Lane. HW maintains this parameter at 1.5 Escape clocks (minimum 75ns)
	7	**HS_EXIT Override** Access: R/W This field controls the override of the HS-EXIT timing parameter Value: 0 — Name: HW maintains Value: 1 — Name: SW overrides
	6:3	**Reserved** Access: RO Format: MBZ
	2:0	**HS_EXIT** Access: R/W This parameter defines the time that the Host drives the LP-11 Lane state (i.e. the Stop state) following a HS burst. HW maintains this parameter at 2 Escape clocks (minimum 100ns)

DPHY_ESC_CLK_DIV

DPHY_ESC_CLK_DIV

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	162190h-162193h
Name:	DPHY 0 Escape Clock Divider
ShortName:	DPHY_ESC_CLK_DIV_0
Reset:	global
Address:	6C190h-6C193h
Name:	DPHY 1 Escape Clock Divider
ShortName:	DPHY_ESC_CLK_DIV_1
Reset:	global

This register defines the clock divider variable M needed to generate an Escape clock from the 8X clock.
This register is located within the combo-PHY. There is an identical register (DSI_ESC_CLK_DIV) located within the Display Core. Both of these registers should be programmed by Software.

Restriction :
The programming of this register must be identical to the programming of its sister register that lives within the Display Core (DSI_ESC_CLK_DIV).
If operating in Dual Link mode, then both Combo-PHY registers (DPHY_ESC_CLK_DIV_0 and DPHY_ESC_CLK_DIV_1) have to be programmed to the same value as the sister register that lives within the Display Core's primary port (DSI_ESC_CLK_DIV_0)

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:16	**Byte Clocks per Escape Clock** Access: RO This field reports the number of Byte clocks present within a given Escape clock. The DSI transcoder calculates this variable based off of the Escape clock divider M. N = Ceiling(M/8) The DSI complex (transcoder and D-PHY) use this information to emulate an Escape clock using the Byte clock.
	15:9	**Reserved** Access: RO Format: MBZ

DPHY_ESC_CLK_DIV

	8:0	**Escape Clock Divider M** Access: R/W **Description** This field specifies the divider variable (M) needed to derive the Escape clock from the Link clock (i.e. the 8X frequency) Escape frequency= 8X frequency / M The DSI transcoder does not use a physical Escape clock, so there is no physical divider, but the transcoder needs to know the value of M to emulate the Escape clock in Byte clocks. **Restriction** The Escape clock frequency must be as close to, but not greater than 20MHz. Therefore, the programming of M should be: M = Ceiling(8X Frequency (in MHz) / 20 MHz)

DPHY_TA_TIMING_PARAM

DPHY_TA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	162188h-16218Bh
Name:	DPHY 0 Turnaround Timing Parameter
ShortName:	DPHY_TA_TIMING_PARAM_0
Reset:	global

Address:	6C188h-6C18Bh
Name:	DPHY 1 Turnaround Timing Parameter
ShortName:	DPHY_TA_TIMING_PARAM_1
Reset:	global

This register specifies the D-PHY timing parameters used for the Bus Turn-Around flow, if SW is overriding the HW defaults.
All fields are defined in number of Escape clocks.

Restriction
Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters. If operating in Dual Link mode, then SW should program both Combo-PHY registers (DPHY_TA_TIMING_PARAM_0 and DPHY_TA_TIMING_PARAM_1), if necessary.

DWord	Bit	Description
0	31	**TA_SURE Override** Access: R/W This field controls the override of the TA-SURE timing parameter Value: 0 — Name: HW maintains Value: 1 — Name: SW overrides
	30:21	**Reserved** Access: RO Format: MBZ
	20:16	**TA_SURE** Access: R/W This parameter defines the time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. This field represents a hexadecimal value with a precision of 3.2 i.e. the most significant 3 bits are the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 7.75 (12.5ns to 387.5ns assuming an Escape clock with a 20MHz frequency)

DPHY_TA_TIMING_PARAM

HW maintains this parameter at 1 Escape clock (minimum 50ns).

Programming Notes
1. Caution: The MIPI D-PHY specification has a maximum of 2 Escape clocks for this parameter 2. If operating at or below an 800MHz Link frequency, this parameter should be overridden and programmed to a value of 0

15 TA_GO Override

Access:	R/W

This field controls the override of the TA-GO timing parameter

Value	Name
0	HW maintains
1	SW overrides

14:12 Reserved

Access:	RO
Format:	MBZ

11:8 TA_GO

Access:	R/W

This parameter defines the time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.
HW maintains this parameter at 4 Escape clocks (minimum 200ns)

Programming Notes
Caution: The MIPI D-PHY specification has a fixed requirement of 4 Escape clocks for this parameter

7 TA_GET Override

Access:	R/W

This field controls the override of the TA-GET timing parameter

Value	Name
0	HW maintains
1	SW overrides

6:4 Reserved

Access:	RO
Format:	MBZ

3:0 TA_GET

Access:	R/W

This parameter defines the time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.
HW maintains this parameter at 5 Escape clocks (minimum 250ns)

DPHY_TA_TIMING_PARAM		
		Programming Notes
		Caution: The MIPI D-PHY specification has a fixed requirement of 5 Escape clocks for this parameter

DPHY_TRIG_EXT

DPHY_TRIG_EXT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	16218Ch-16218Fh
Name:	DPHY 0 Trigger Extension
ShortName:	DPHY_TRIG_EXT_0
Reset:	global
Address:	6C18Ch-6C18Fh
Name:	DPHY 1 Trigger Extension
ShortName:	DPHY_TRIG_EXT_1
Reset:	global

This register specifies the amount of time to extend a Trigger message to the Peripheral.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Trigger Extension** Access: R/W This field specifies the number of Escape clocks to extend a trigger message by. This effectively extends the duration that the trigger is asserted at the Peripherals Protocol Layer. This field is only used if a Trigger Message is initiated from the DSI_LP_MSG register.

DPLC_CTL

DPLC_CTL

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled

Address:	49400h-49403h
Name:	Pipe A LDPST Control
ShortName:	DPLC_CTL_A
Reset:	soft

Restriction : LDPST is supported for horizontal and vertical pipe sizes up to 4096 pixels.

Restriction

In cases where software wants to use the Image enhancement functionality with pre-determined IE values when the pipe starts, the following programming sequence should be followed.

1. Enable LDPST with the Orientation and the Tile Size bits programmed correctly.
2. Program IE coefficients
3. Enable pipe.

Orientation and Tile Size must not be changed when the LDPST function is enabled.

DWord	Bit	Description
0	31	**Function Enable** This field enables the LDPST function. Histogram is enabled directly by this field. Image enhancement is enabled if both this field and IE Enable are set. **Value** / **Name** 0b / Disable 1b / Enable
	30	**IE Enable** This field enables LDPST image enhancement. This field is ignored if the function is disabled. **Value** / **Name** / **Description** 0b / Disable / Input pixels are routed to output with no modification 1b / Enable / Input pixels will go through image enhancement before output
	29	**Load IE** Access: R/W Set This field is set by software to request the new image enhancement table to be loaded into the working RAMs on the next start of vertical blank or Pipe not enabled. Hardware clears this field after the load is complete.

DPLC_CTL

Value	Name
0b	Ready/Done
1b	Loading

28 **Orientation**

This field sets the orientation. In case of preload when there is a change in Orientation for next frame, this bit needs to be set before the IE correction points are written.

Value	Name	Description
0b	Landscape	16x9 tile arrangement
1b	Portrait	9x16 tile arrangement

27 **Frame Histogram Done**

Access:	R/WC

This bit is set by H/W when done creating histograms for all valid tiles (based on hsize and vsize). S/W should start reading from histogram buffers only when this bit is set. S/W must clear the bit by a write of '1' once the histogram read is complete.

Value	Name	Description
0b	Not Done	Histogram creation not done
1b	Done	Histogram creation done

26 **Histogram Buffer ID**

Access:	RO

This bit is set or cleared by H/W to indicate which double buffered BANK H/W is working on for creating histogram for current frame. This bit toggles one clk after Vblank if Hist_buffer_delay bit is not set.

Value	Name	Description
0b	Bank0	Creating Histogram in Bank0
1b	Bank1	Creating Histogram in Bank1

25 **IE Buffer ID**

Access:	RO

This bit is set or cleared by H/W to indicate which double buffered BANK H/W is using for reading correction factors for current frame. This bit will toggle at Vblank when load IE bit is set.

Value	Name	Description
0b	Bank0	Reading correction factors from Bank 0
1b	Bank1	Reading correction factors from Bank 0

24 **Allow Double Buffer Update Disable**

Access:	R/W

This field controls whether double buffer updates are allowed to be disabled for the double buffered LACE (DPLC) registers. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled.

DPLC_CTL

		Value / **Name** 0b – Not Allowed 1b – Allowed **[Default]**
	23	**Fast Access Mode Enable** This field enables the fast access mode where hardware transfers the histogram and IET to and from memory. **Value** / **Name** 0b – Disable 1b – Enable
	22	**Reserved**
	21	**Reserved**
	20	**Reserved**
	19	**Reserved**
	18:14	**Reserved** Access: RO Format: MBZ
	13:12	**Enhancement mode** These bits are the control bits to select between Look up table mode and Multiplier mode. **Value** / **Name** / **Description** 00b – Direct **[Default]** – Direct look up Mode 01b – Multiplicative – Multiplicative Mode 10b – Reserved – Reserved 11b – Reserved – Reserved
	11	**Reserved**
	10	**Reserved**
	9	**Reserved**
	8	**Reserved**
	7	**Reserved**
	6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3	**Reserved**
	2	**Reserved**

DPLC_CTL		
	1	**Hist Buffer Delay** Access: R/W This field controls when the histogram readback buffer is loaded in H/W. S/W can set this bit while reading the histogram bin registers to ensure that the H/W does not overwrite the histogram registers with the data for the new frame. This bit must be cleared by the S/W as soon as the histogram bin read is complete.
	0	**Reserved**

DPLC_FA_IIR

DPLC_FA_IIR

Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	49468h-4946Bh
Name:	Pipe A LDPST Fast Access Interrupt Identity
ShortName:	DPLC_FA_IIR_A
Reset:	soft

This register holds the persistent values of the interrupt bits which are unmasked by IMR. Bits set in this register will propagate to the LACE interrupt in the Pipe Interrupts.

DWord	Bit	Description
0	31:23	**Reserved** Access: RO Format: MBZ
	22	**Part B Histogram Copy Done** This field is set by hardware when DMC indicates it has finished copying this part to memory. Clear by writing with a 1. 0b – Not Done 1b – Done
	21	**Part B Load IE** This field is set by hardware on the rising edge of the load of the image enhancement table for this part. Clear by writing with a 1. 0b – Ready/Done 1b – Loading
	20	**Part B Histogram Ready** This field is set by hardware on the rising edge of when the histogram for this part is ready inside LACE. Clear by writing with a 1. 0b – Not ready 1b – Ready
	19	**Part B IET Overlap** This field is set by LACE hardware when the IET for this part is not loaded (Part Load IE bit set) before the other part is loaded. Clear by writing with a 1. 0b – Not Late

DPLC_FA_IIR

	1b	Late

18 Part B IET Late

This field is set by LACE hardware when the IET for this part is not loaded (Part Load IE bit set) before this part starts in the next frame. Clear by writing with a 1.

Value	Name
0b	Not Late
1b	Late

17 Part B Histogram Overlap

This field is set by LACE hardware when the histogram for this part is not read out (Part Histogram Done bit cleared) before the other part histogram becomes ready. Clear by writing with a 1.

Value	Name
0b	Not Overlap
1b	Overlap

16 Part B Histogram Late

This field is set by LACE hardware when the histogram for this part is not read out (Part Histogram Done bit cleared) before this part starts in the next frame. Clear by writing with a 1.

Value	Name
0b	Not Late
1b	Late

15:7 Reserved

Access:	RO
Format:	MBZ

6 Part A Histogram Copy Done

This field is set by hardware when DMC indicates it has finished copying this part to memory. Clear by writing with a 1.

Value	Name
0b	Not Done
1b	Done

5 Part A Load IE

This field is set by hardware on the rising edge of the load of the image enhancement table for this part. Clear by writing with a 1.

Value	Name
0b	Ready/Done
1b	Loading

4 Part A Histogram Ready

This field is set by hardware on the rising edge of when the histogram for this part is ready inside LACE. Clear by writing with a 1.

DPLC_FA_IIR

Value	Name
0b	Not ready
1b	Ready

3	**Part A IET Overlap** This field is set by hardware when the IET for this part is not loaded (Part Load IE bit set) before the other part is loaded. Clear by writing with a 1.

Value	Name
0b	Not Late
1b	Late

2	**Part A IET Late** This field is set by hardware when the IET for this part is not loaded (Part Load IE bit set) before this part starts in the next frame. Clear by writing with a 1.

Value	Name
0b	Not Late
1b	Late

1	**Part A Histogram Overlap** This field is set by hardware when the histogram for this part is not read out (Part Histogram Done bit cleared) before the other part histogram becomes ready. Clear by writing with a 1.

Value	Name
0b	Not Overlap
1b	Overlap

0	**Part A Histogram Late** This field is set by hardware when the histogram for this part is not read out (Part Histogram Done bit cleared) before this part starts in the next frame. Clear by writing with a 1.

Value	Name
0b	Not Late
1b	Late

DPLC_FA_IMR

DPLC_FA_IMR

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	49464h-49467h
Name:	Pipe A LDPST Fast Access Interrupt Mask
ShortName:	DPLC_FA_IMR_A
Reset:	soft

This register contains a bit mask which selects the events that will be reported in the IIR.

DWord	Bit	Description
0	31:23	**Reserved** Access: RO Format: MBZ
	22	**Part B Histogram Copy Done Mask** Access: R/W 0b: Unmask 1b: Mask **[Default]**
	21	**Part B Load IE Mask** Access: R/W 0b: Unmask 1b: Mask **[Default]**
	20	**Part B Histogram Ready Mask** Access: R/W 0b: Unmask 1b: Mask **[Default]**
	19	**Part B IET Overlap Mask** Access: R/W 0b: Unmask

DPLC_FA_IMR

	1b	Mask **[Default]**
18	**Part B IET Late Mask**	
	Access:	R/W
	Value	**Name**
	0b	Unmask
	1b	Mask **[Default]**
17	**Part B Histogram Overlap Mask**	
	Access:	R/W
	Value	**Name**
	0b	Unmask
	1b	Mask **[Default]**
16	**Part B Histogram Late Mask**	
	Access:	R/W
	Value	**Name**
	0b	Unmask
	1b	Mask **[Default]**
15:7	**Reserved**	
	Access:	RO
	Format:	MBZ
6	**Part A Histogram Copy Done Mask**	
	Access:	R/W
	Value	**Name**
	0b	Unmask
	1b	Mask **[Default]**
5	**Part A Load IE Mask**	
	Access:	R/W
	Value	**Name**
	0b	Unmask
	1b	Mask **[Default]**
4	**Part A Histogram Ready Mask**	
	Access:	R/W

DPLC_FA_IMR

Value	Name
0b	Unmask
1b	Mask **[Default]**

3 **Part A IET Overlap Mask**

Access:	R/W

Value	Name
0b	Unmask
1b	Mask **[Default]**

2 **Part A IET Late Mask**

Access:	R/W

Value	Name
0b	Unmask
1b	Mask **[Default]**

1 **Part A Histogram Overlap Mask**

Access:	R/W

Value	Name
0b	Unmask
1b	Mask **[Default]**

0 **Part A Histogram Late Mask**

Access:	R/W

Value	Name
0b	Unmask
1b	Mask **[Default]**

DPLC_FA_STATUS

DPLC_FA_STATUS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	49460h-49463h
Name:	Pipe A LDPST Fast Access Status
ShortName:	DPLC_FA_STATUS_A
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18	**Part B Histogram Copy Done** Access: R/W Set This field is set by DMC when it finishes copying this part to memory. LACE hardware clears this field immediately. The pulse is used to set the histogram copy done interrupt. 0b – Not Done 1b – Done
	17	**Part B Load IE** Access: R/W Set This field is set by DSB to request LACE hardware to load the new image enhancement table for this part. LACE hardware clears this field at the end of this part. 0b – Ready/Done 1b – Loading
	16	**Part B Histogram Ready** Access: R/WC This field is set by LACE hardware when the histogram for this part is ready inside LACE. DMC writes 1 to clear this field after reading out the histogram. 0b – Not ready 1b – Ready
	15:3	**Reserved** Access: RO Format: MBZ

DPLC_FA_STATUS

	2	**Part A Histogram Copy Done** Access: R/W Set This field is set by DMC when it finishes copying this part to memory. LACE hardware clears this field immediately. The pulse is used to set the histogram copy done interrupt. **Value** / **Name** 0b – Not Done 1b – Done
	1	**Part A Load IE** Access: R/W Set This field is set by DSB to request LACE hardware to load the new image enhancement table for this part. LACE hardware clears this field at the end of this part. **Value** / **Name** 0b – Ready/Done 1b – Loading
	0	**Part A Histogram Ready** Access: R/WC This field is set by LACE hardware when the histogram for this part is ready inside LACE. DMC writes 1 to clear this field after reading out the histogram. **Value** / **Name** 0b – Not ready 1b – Ready

DPLC_FA_SURF

DPLC_FA_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	49470h-49473h
Name:	Pipe A LDPST Fast Access Surface Part A
ShortName:	DPLC_FA_SURF_PARTA_A
Reset:	soft
Address:	49474h-49477h
Name:	Pipe A LDPST Fast Access Surface Part B
ShortName:	DPLC_FA_SURF_PARTB_A
Reset:	soft

DWord	Bit	Description
0	31:12	**Surface Base Address** This field specifies the surface base address bits 31:12 that the LACE histogram is copied to in fast access mode. It is mapped to physical pages through the global GTT. **Restriction** The surface must be linear. This address must be at least 4KB aligned.
	11:0	**Reserved** Access: RO Format: MBZ

DPLC_FA_SURF_LIVE

DPLC_FA_SURF_LIVE			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	49478h-4947Bh		
Name:	Pipe A LDPST Fast Access Surface Live Part A		
ShortName:	DPLC_FA_SURF_LIVE_PARTA_A		
Reset:	soft		
Address:	4947Ch-4947Fh		
Name:	Pipe A LDPST Fast Access Surface Live Part B		
ShortName:	DPLC_FA_SURF_LIVE_PARTB_A		
Reset:	soft		
DWord	**Bit**	**Description**	
0 The live register updates at the start of the associated part.	31:12	**Surface Base Address** This field specifies the live (double-buffered value in use currently) surface base address.	
	11:0	**Reserved**	
		Access:	RO
		Format:	MBZ

DPLC_HIST_DATA

DPLC_HIST_DATA	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	49408h-4940Bh
Name:	Pipe A LDPST Histogram Data
ShortName:	DPLC_HIST_DATA_A
Reset:	soft

This register contains the histogram values for the array of LDPST Histogram table entries.
The data format is arranged as 32 dwords for each tile, containing 32 bins. The index register controls which bin and dword is accessed.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16:0	**Bin** Histogram Data for Bin

DPLC_HIST_INDEX

DPLC_HIST_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	49404h-49407h
Name:	Pipe A LDPST Histogram Index
ShortName:	DPLC_HIST_INDEX_A
Reset:	soft

Description

The LDPST Histogram table tile entries are accessed through index and data registers.
Each tile is composed of 32 histogram bins in 32 data Dwords.
The index fields address the individual tiles and Dwords.
Hardware will automatically walk the indexes through each Dword and raster scan through the X and Y, starting from the upper left corner of the display. The automatic walk is based on the programmed pipe source size.
Software can manually program the index to access specific tiles and Dwords.

There are 260 tiles arranged in a 20x13 (horizontal x vertical) or 13x20 array, depending on the DPLC_CTL Orientation setting.

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:16	**Y Index** Access: Write/Read Status This index points to the current vertical tile row in the array. This index auto increments by one after each horizontal tile row is completed. It will automatically rollover when the final (20th or 13th) vertical tile row is completed. Value: [0,19] — Name:
	15:13	**Reserved** Access: RO Format: MBZ
	12:8	**X Index** Access: Write/Read Status This index points to current horizontal tile in the array. This index auto increments by one after the final (32nd) Dword is accessed. It will automatically rollover when the final (20th or 13th) horizontal tile is completed.

DPLC_HIST_INDEX

		Value / **Name** [0,19] /
	7:5	**Reserved** Access: RO Format: MBZ
	4:0	**DW Index** Access: Write/Read Status This index points to the next Dword within the tile. This index auto increments by one after each read to the data register is completed. It will automatically rollover when the final (32nd) Dword is accessed. **Value** / **Name** [0,31] /

DPLC_IE_DATA

DPLC_IE_DATA	
Register Space:	MMIO: 0/2/0
Access:	Write/Read Status
Size (in bits):	32
Address:	49410h-49413h
Name:	Pipe A LDPST Image Enhancement Data
ShortName:	DPLC_IE_DATA_A
Reset:	soft

This register contains the image enhanced pixel values for the array of LDPST Image Enhancement table entries. The data format is arranged as 17 dwords for each tile, containing 33 image enhancement points. The points are packed two per dword, aligned on 16 bit boundaries. The index register controls which bin and dword is accessed.
Point 34 is invalid and not used.
Direct Lookup mode:
If the calculated Image enhancement value is using less than 12 bits, it must be shifted left to 12 bits before programming.
Multiplicative mode:
Mulitplicative image enhancement values must be programmed directly in the 3.9 fixed point format.

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27:16	**Odd Point** Enhancement Data for Point 2*N+1
	15:12	**Reserved** Access: RO Format: MBZ
	11:0	**Even Point** Enhancement Data for Point 2*N

DPLC_IE_INDEX

DPLC_IE_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4940Ch-4940Fh
Name:	Pipe A LDPST Image Enhancement Index
ShortName:	DPLC_IE_INDEX_A
Reset:	soft

Description

The LDPST Histogram table tile entries are accessed through index and data registers.
Each tile is composed of 33 image enhancement points in 17 data Dwords. Any IE data writes must start from DW index 0 and update all 17 Dwords
The index fields address the individual tiles and Dwords.
Hardware will automatically walk the indexes through each Dword and raster scan through the X and Y, starting from the upper left corner of the display. The automatic walk is based on the programmed pipe source size.
Software can manually program the index to access specific tiles and Dwords.

There are 260 tiles arranged in a 20x13 (horizontal x vertical) or 13x20 array, depending on the DPLC_CTL Orientation setting.

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:16	**Y Index** Access: Write/Read Status This index points to the current vertical tile row in the array. This index auto increments by one after each horizontal tile row is completed. It will automatically rollover when the final (20th or 13th) vertical tile row is completed. Value: [0,19] — Name:
	15:13	**Reserved** Access: RO Format: MBZ
	12:8	**X Index** Access: Write/Read Status This index points to current horizontal tile in the array. This index auto increments by one after the final (17th) Dword is accessed. It will automatically rollover when the final (20th or 13th) horizontal tile is completed.

DPLC_IE_INDEX

		Value / **Name** [0,19] /
	7:5	**Reserved** Access: RO Format: MBZ
	4:0	**DW Index** Access: Write/Read Status This index points to the next Dword within the tile. This index auto increments by one after each read or write to the data register is completed. It will automatically rollover when the final (17th) Dword is accessed. **Value** / **Name** [0,16] /

DPLC_PART_CTL

DPLC_PART_CTL		
Register Space:	MMIO: 0/2/0	
Access:	Double Buffered	
Size (in bits):	32	
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank or pipe not enabled		
Address:	49430h-49433h	
Name:	Pipe A LDPST Partition Control	
ShortName:	DPLC_PART_CTL_A	
Reset:	soft	

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:21	**Part B End Tile Row** This field specifies the tile row that ends part B.
	20:16	**Part B Start Tile Row** This field specifies the tile row that starts part B.
	15:10	**Reserved** Access: RO Format: MBZ
	9:5	**Part A End Tile Row** This field specifies the tile row that ends part A.
	4:0	**Part A Start Tile Row** This field specifies the tile row that starts part A.

DPLC_PTRCFG

DPLC_PTRCFG		
Register Space:	MMIO: 0/2/0	
Access:	Double Buffered	
Size (in bits):	32	
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled	
Address:	49434h-49437h	
Name:	Pipe A LDPST Pointer Config Part A	
ShortName:	DPLC_PTRCFG_PARTA_A	
Reset:	soft	
Address:	49438h-4943Bh	
Name:	Pipe A LDPST Pointer Config Part B	
ShortName:	DPLC_PTRCFG_PARTB_A	
Reset:	soft	

DWord	Bit	Description
0	31:0	**Histogram Index** This field specifies the histogram index for fast LACE access.

DPLC_PTRCFG_LIVE

DPLC_PTRCFG_LIVE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	49444h-49447h
Name:	Pipe A LDPST Pointer Config Live Part A
ShortName:	DPLC_PTRCFG_LIVE_PARTA_A
Reset:	soft
Address:	49448h-4944Bh
Name:	Pipe A LDPST Pointer Config Live Part B
ShortName:	DPLC_PTRCFG_LIVE_PARTB_A
Reset:	soft

DWord	Bit	Description
0 The live register updates at the start of the associated part.	31:0	**Histogram Index** This field specifies the live (double-buffered value in use currently) histogram index for fast LACE access.

DPLC_RDLENGTH

DPLC_RDLENGTH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	4943Ch-4943Fh
Name:	Pipe A LDPST Read Length Part A
ShortName:	DPLC_RDLENGTH_PARTA_A
Reset:	soft
Address:	49440h-49443h
Name:	Pipe A LDPST Read Length Part B
ShortName:	DPLC_RDLENGTH_PARTB_A
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Read Length** This field specifies the number of cachelines of histogram to read for fast LACE access. Program CEILING(number of histogram DWords/16).

DPLC_RDLENGTH_LIVE

DPLC_RDLENGTH_LIVE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	4944Ch-4944Fh
Name:	Pipe A LDPST Read Length Live Part A
ShortName:	DPLC_RDLENGTH_LIVE_PARTA_A
Reset:	soft
Address:	49450h-49453h
Name:	Pipe A LDPST Read Length Live Part B
ShortName:	DPLC_RDLENGTH_LIVE_PARTB_A
Reset:	soft

DWord	Bit	Description
0 The live register updates at the start of the associated part.	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Read Length** This field specifies the live (double-buffered value in use currently) number of cachelines of histogram to read for fast LACE access.

DPLL_CFGCR0

DPLL_CFGCR0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	164284h-164287h
Name:	DPLL0_CFGCR0
ShortName:	DPLL0_CFGCR0
Reset:	global
Address:	16428Ch-16428Fh
Name:	DPLL1_CFGCR0
ShortName:	DPLL1_CFGCR0
Reset:	global
Address:	16429Ch-16429Fh
Name:	TBTPLL_CFGCR0
ShortName:	TBTPLL_CFGCR0
Reset:	global
Address:	164294h-164297h
Name:	DPLL4_CFGCR0
ShortName:	DPLL4_CFGCR0
Reset:	global

This register is used to configure the DPLL mode, frequency, and SSC.
This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24:10	**DCO Fraction** Default Value: 0x4000 (DCO Frequency/Reference Frequency - INT(DCO Frequency/Reference Frequency)) * 2^15
	9:0	**DCO Integer** Default Value: 0x151 INT (DCO Frequency/Reference Frequency)

DPLL_CFGCR1

DPLL_CFGCR1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	164288h-16428Bh
Name:	DPLL0_CFGCR1
ShortName:	DPLL0_CFGCR1
Reset:	global
Address:	164290h-164293h
Name:	DPLL1_CFGCR1
ShortName:	DPLL1_CFGCR1
Reset:	global
Address:	1642A0h-1642A3h
Name:	TBTPLL_CFGCR1
ShortName:	TBTPLL_CFGCR1
Reset:	global
Address:	164298h-16429Bh
Name:	DPLL4_CFGCR1
ShortName:	DPLL4_CFGCR1
Reset:	global

This register, together with DPLL_CFGCR0, is used to configure the DPLL frequency.

This register is not reset by the device 2 FLR.

Programming Notes

The post divider is P*Q*K

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:10	**Qdiv Ratio** This field specifies the Q divider ratio. This field is only used when Qdiv Mode is set to Enable to get a divider value other than 1.
	9	**Qdiv Mode** This field enables the Q divider when the ratio is not 1. Value: 0b — Name: Disable — Description: Q divider = 1

DPLL_CFGCR1

1b	Enable	Q divider = Qdiv Ratio

Restriction
If K is not 2, Q MUST be 1 to ensure 50% duty cycle.

8:6 **Kdiv**

This field specifies the K divider ratio.

Value	Name
001b	1 **[Default]**
010b	2
100b	3

5:2 **Pdiv**

This field specifies the P divider ratio.

Value	Name
0001b	2
0010b	3 **[Default]**
0100b	5
1000b	7

1:0 **cfselovrd**

Display controller programs this field to set desired reference clock source in the case of genlocked systems.

Value	Name	Description
00b	Normal XTAL	Normal XTAL cannot be picked as genlock clock source if the transcoder is programmed as genlock remote secondary.
01b	Unfiltered genlock ref	
11b	Filtered genlock ref	
10b	Reserved	

DPLL_DIV0

DPLL_DIV0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	164B00h-164B03h
Name:	DPLL0_DIV0
ShortName:	DPLL0_DIV0
Reset:	global
Address:	164C00h-164C03h
Name:	DPLL1_DIV0
ShortName:	DPLL1_DIV0
Reset:	global
Address:	164E00h-164E03h
Name:	DPLL4_DIV0
ShortName:	DPLL4_DIV0
Reset:	global

DPLL tuning.

DWord	Bit	Description
0	31:30	**i_truelock_criteria_1_0** Default Value: 01b True lock indicator criteria. After early lock generation, external PLL lock indicator asserted high when phase error is less than threshold value. 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	29:28	**i_earlylock_criteria_1_0** Default Value: 11b Early lock indicator criteria. Early PLL lock indicator asserted high when phase error is less than threshold value. 00: 16 consecutive cycles 01: 32 consecutive cycles 10: 48 consecutive cycles 11: 64 consecutive cycles
	27:25	**i_afc_startup_2_0** Default Value: 000b This is for AFC start point. 000: fine = 511

DPLL_DIV0		
		001: fine = 639 (+128) 010: fine = 767 (+256) 011: fine = 895 (+384) 100: NA 101: fine = 127 (-384) 110: fine = 255 (-256) 111: fine = 383 (-128).
	24	**i_divretimeren** Retiming of feedback clock.
	23:21	**i_gainctrl_2_0** Default Value: 001b Adjustable gain for loop filter. Both coefficients shifted right by gainctrl before lock.
	20:16	**i_int_coeff_4_0** Default Value: 7h integral coeff. = 2^(-int_coeff), tageting up to 2^-11.
	15:12	**i_prop_coeff_3_0** Default Value: 0010b proportional coeff. = 2^(-prop_coeff+1).
	11:8	**i_fbprediv_3_0** Default Value: 0010b Predivider ratio 0000,0001 : reserved 0010: /2 0100: /4 0011: reserved Rest: reserved
	7:0	**i_fbdiv_intgr** Default Value: 69h Feedback divider post division (M2 integer).

DPLL_ENABLE

DPLL_ENABLE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	46010h-46013h
Name:	DPLL 0 Enable
ShortName:	DPLL0_ENABLE
Reset:	soft
Address:	46014h-46017h
Name:	DPLL 1 Enable
ShortName:	DPLL1_ENABLE
Reset:	soft
Address:	46018h-4601Bh
Name:	DPLL 4 Enable
ShortName:	DPLL4_ENABLE
Reset:	soft
Address:	46020h-46023h
Name:	Thunderbolt PLL Enable
ShortName:	TBT_PLL_ENABLE
Reset:	soft
Address:	46030h-46033h
Name:	MG PLL 1 Enable
ShortName:	MGPLL1_ENABLE
Reset:	soft
Address:	46034h-46037h
Name:	MG PLL 2 Enable
ShortName:	MGPLL2_ENABLE
Reset:	soft
Address:	46038h-4603Bh
Name:	MG PLL 3 Enable
ShortName:	MGPLL3_ENABLE
Reset:	soft
Address:	4603Ch-4603Fh
Name:	MG PLL 4 Enable

DPLL_ENABLE

ShortName:	MGPLL4_ENABLE
Reset:	soft

Address:	46040h-46043h
Name:	MG PLL 5 Enable
ShortName:	MGPLL5_ENABLE
Reset:	soft

Address:	46044h-46047h
Name:	MG PLL 6 Enable
ShortName:	MGPLL6_ENABLE
Reset:	soft

These registers are used to enable the PLLs for driving the ports.

Note that MG register instances are being used for TypeC in general, so they include the Dekel PLLs as well.

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the PLL. Value: 0b = Disable; 1b = Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the PLL Lock. Value: 0b = Not locked or not enabled; 1b = Locked
	29	**Reserved**
	28	**Reserved** Access: RO Format: MBZ
	27	**Power Enable** This field enables or disables the PLL power. Value: 0b = Disable; 1b = Enable
	26	**Power State** Access: RO This fields indicates the status of the PLL power.

DPLL_ENABLE

		Value / **Name** 0b / Disabled 1b / Enabled
	25:12	**Reserved** Access: RO Format: MBZ
	11	**Reserved** Access: RO Format: MBZ
	10:0	**Reserved** Access: RO Format: MBZ

DPLL_SSC

DPLL_SSC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	164B10h-164B13h
Name:	DPLL0_SSC
ShortName:	DPLL0_SSC
Reset:	global
Address:	164C10h-164C13h
Name:	DPLL1_SSC
ShortName:	DPLL1_SSC
Reset:	global
Address:	164E10h-164E13h
Name:	DPLL4_SSC
ShortName:	DPLL4_SSC
Reset:	global

DPLL SSC tuning

DWord	Bit	Description
0	31:29	**iref_ndivratio** Default Value: 0x4 Refclock divider control
	28:26	**sscstepnum_offset** SSC step number offset
	25	**sscinj_adapt_en_h** SSC injection Adaptive Gain Change Enable Value: 0b — Name: Disable Value: 1b — Name: Enable
	24	**sscinj_en_h** SSC injection enable Value: 0b — Name: Disable Value: 1b — Name: Enable
	23:16	**sscsteplength** Num of refclk cycles of one SSC step

<table>
<tr><th colspan="3">DPLL_SSC</th></tr>
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Select frequency update rate for FLL SSC</td></tr>
<tr><td></td><td>13:11</td><td>sscstepnum
<table><tr><td>Default Value:</td><td>0x4</td></tr></table>SSC step number</td></tr>
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Openloop SSC enable</td></tr>
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Enables SSC modulator<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table></td></tr>
<tr><td></td><td>8</td><td>sscfllen
Enable frequency adjustment for FLL SSC</td></tr>
<tr><td></td><td>7:6</td><td>bias_gb_sel
<table><tr><td>Default Value:</td><td>0x3</td></tr></table>Select guard band after bias calibration</td></tr>
<tr><td></td><td>5:0</td><td>init_dcoamp
<table><tr><td>Default Value:</td><td>0x3F</td></tr></table>Initial DCOAMP value</td></tr>
</table>

DPST_BIN

DPST_BIN	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank

Address:	490C4h-490C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_A
Reset:	soft

Address:	491C4h-491C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_B
Reset:	soft

Address:	492C4h-492C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_C
Reset:	soft

Address:	493C4h-493C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_D
Reset:	soft

Access to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index.Updates take place at the start of vertical blank.

DWord	Bit	Description

0	31	**Busy Bit**
		If (DPST_CTL:Bin Register Function Select = Threshold Count) {
		This is a read only bit. If set, the engine is busy and the rest of the register is undefined. If clear, the register contains valid data.
		}
		Else (Image Enhancement) {
		This bit is reserved.
		}

	30:24	**Reserved** Access: RO Format: MBZ

DPST_BIN		

	23:0	**Data**
		If (DPST_CTL : Bin Register Function Select = Threshold Count) {
		Bits 23:0 are read only bits when the Restore DPST bit (DPST_CTL) is cleared and read/write when the Restore DPST bit is set.
		They indicate the total number of pixels in this bin. The bin value is updated when guardband interrupt delay is met, and is not valid until after a histogram event has occurred. The bin value will stop incrementing once the maximum has been reached.
		}
		Else (Image Enhancement) {
		Bits 23:10 are reserved and should be written as zeroes. Bits 9:0 are R/W double-buffered and program the correction value for this bin. Writes to this register are double buffered on the next vblank. The value written here is the 10bit corrected channel value for the lowest point of the bin.
		}

DPST_CTL

DPST_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	490C0h-490C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_A
Reset:	soft
Address:	491C0h-491C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_B
Reset:	soft
Address:	492C0h-492C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_C
Reset:	soft
Address:	493C0h-493C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**IE Histogram Enable** This bit enables the Image Enhancement histogram logic to collect data. The collected data will be valid after a histogram event has occurred. **Value** / **Name** 0b – Disable 1b – Enable **Programming Notes** If histogram is enabled while no planes are enabled on the pipe, it may get an incorrect pixel count for a frame.
	30:29	**Reserved** Access: RO Format: MBZ

DPST_CTL

28 Reserved

Access:	RO
Format:	MBZ

27 IE Modification Table Enable

This bit enables the Image Enhancement modification table. When enabled, modifications begin after the next vertical blank.

Value	Name
0b	Disable
1b	Enable

26:25 Reserved

Access:	RO
Format:	MBZ

24 Histogram Mode Select

Value	Name	Description
0b	YUV	YUV Luma Mode
1b	HSV	HSV Intensity Mode

23:16 Reserved

Access:	RO
Format:	MBZ

15 IE Table Value Format

This field indicates what format is used for the image enhancement table values in multiplicative mode. The other modes use a 0.10 (0 integer and 10 fractional bits) format.

Value	Name	Description
0b	1.9	1 integer and 9 fractional bits
1b	2.8	2 integer and 8 fractional bits

14:13 Enhancement mode

Value	Name	Description
00b	Direct	Direct look up mode
01b	Additive	Additive mode
10b	Multiplicative	Multiplicative mode
11b	Reserved	Reserved

12 Reserved

Access:	RO
Format:	MBZ

DPST_CTL

	11	**Bin Register Function Select** This field indicates what data is being written to or read from the bin data register. **Value** / **Name** / **Description** 0b / TC / Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1b / IE / Image Enhancement Value. Valid range for the Bin Index is 0 to 32
	10:7	**Reserved** Access: RO Format: MBZ
	6:0	**Bin Register Index** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

DPST_GUARD

DPST_GUARD	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank
Address:	490C8h-490CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_A
Reset:	soft
Address:	491C8h-491CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_B
Reset:	soft
Address:	492C8h-492CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_C
Reset:	soft
Address:	493C8h-493CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_D
Reset:	soft

Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Histogram Interrupt enable** Value / Name / Description 0b / Disable / Disabled 1b / Enable / This generates a histogram interrupt once a Histogram event occurs.
	30	**Histogram Event status** Access: R/WC When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, clear this bit by writing a '1'. Value / Name / Description 0b / Not Occurred / Histogram event has not occurred 1b / Occurred / Histogram event has occurred

DPST_GUARD		
	29:22	**Guardband Interrupt Delay** An interrupt is always generated after this many consecutive frames of the guardband threshold being surpassed .This value is double buffered on start of vblank. **Restriction** A value of 0 is invalid.
	21:0	**Threshold Guardband** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank. This value is shifted left 2 bits (multiplied by 4) for use with the 24 bit bin values.

Driver Media Force Wake Ack

DRIVER_MEDIA_FWAKE_ACK - Driver Media Force Wake Ack	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D88h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Media ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Can be powered down (default) 1'b1 : GT Media cannot be powered down

DRIVER MEDIA FORCE WAKE REQ

DRIVER_MEDIA_FWAKE - DRIVER MEDIA FORCE WAKE REQ

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A270h

The newly loaded Gfx driver must first initialize this register by clearing all bits (0xFF00).

DWord	Bit	Description
0	31:16	**Multiple Force Wake Mask** Access: R/W _Custom_GTIReset: DEV Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0 is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15	**Force Wake Request for Thread 15** Access: R/W _Custom_GTIReset: DEV Thread 15 - When set with corresponding mask bit 31, Media cannot be powered down.
	14	**Force Wake Request for Thread 14** Access: R/W _Custom_GTIReset: DEV Thread 14 - When set with corresponding mask bit 30, Media cannot be powered down.
	13	**Force Wake Request for Thread 13** Access: R/W _Custom_GTIReset: DEV Thread 13 - When set with corresponding mask bit 29, Media cannot be powered down.
	12	**Force Wake Request for Thread 12** Access: R/W _Custom_GTIReset: DEV Thread 12 - When set with corresponding mask bit 28, Media cannot be powered down.
	11	**Force Wake Request for Thread 11** Access: R/W _Custom_GTIReset: DEV Thread 11 - When set with corresponding mask bit 27, Media cannot be powered down.

DRIVER_MEDIA_FWAKE - DRIVER MEDIA FORCE WAKE REQ

	10	**Force Wake Request for Thread 10** Access: R/W _Custom_GTIReset: DEV Thread 10 - When set with corresponding mask bit 26, Media cannot be powered down.
	9	**Force Wake Request for Thread 9** Access: R/W _Custom_GTIReset: DEV Thread 9 - When set with corresponding mask bit 25, Media cannot be powered down.
	8	**Force Wake Request for Thread 8** Access: R/W _Custom_GTIReset: DEV Thread 8 - When set with corresponding mask bit 24, Media cannot be powered down.
	7	**Force Wake Request for Thread 7** Access: R/W _Custom_GTIReset: DEV Thread 7 - When set with corresponding mask bit 23, Media cannot be powered down.
	6	**Force Wake Request for Thread 6** Access: R/W _Custom_GTIReset: DEV Thread 6 - When set with corresponding mask bit 22, Media cannot be powered down.
	5	**Force Wake Request for Thread 5** Access: R/W _Custom_GTIReset: DEV Thread 5 - When set with corresponding mask bit 21, Media cannot be powered down.
	4	**Force Wake Request for Thread 4** Access: R/W _Custom_GTIReset: DEV Thread 4 - When set with corresponding mask bit 20, Media cannot be powered down.
	3	**Force Wake Request for Thread 3** Access: R/W _Custom_GTIReset: DEV Thread 3 - When set with corresponding mask bit 19, Media cannot be powered down.

DRIVER_MEDIA_FWAKE - DRIVER MEDIA FORCE WAKE REQ

	2	**Force Wake Request for Thread 2** Access: R/W _Custom_GTIReset: DEV Thread 2 - When set with corresponding mask bit 18, Media cannot be powered down.
	1	**Force Wake Request for Thread 1** Access: R/W _Custom_GTIReset: DEV Thread 1 - When set with corresponding mask bit 17, Media cannot be powered down.
	0	**Force Wake Request for Thread 0** Access: R/W _Custom_GTIReset: DEV Thread 0 - When set with corresponding mask bit 16, Media cannot be powered down.

Driver Render Force Wake Ack

DRIVER_RENDER_FWAKE_ACK - Driver Render Force Wake Ack	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D84h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Render Can be powered down (default) 1'b1 : GT Render cannot be powered down

Driver VDBox0 Force Wake Ack

DRIVER_VDBOX0_FWAKE_ACK - Driver VDBox0 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D50h
Name:	Driver VDBox0 Force Wake Ack
ShortName:	DRIVER_VDBOX0_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox0 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox0 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 0 can be powered down (default) 1'b1 : GT Media Slice 0 cannot be powered down

Driver VDBox1 Force Wake Ack

DRIVER_VDBOX1_FWAKE_ACK - Driver VDBox1 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D54h
Name:	Driver VDBox1 Force Wake Ack
ShortName:	DRIVER_VDBOX1_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox1 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox1 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 0 can be powered down (default) 1'b1 : GT Media Slice 0 cannot be powered down

Driver VDBox2 Force Wake Ack

DRIVER_VDBOX2_FWAKE_ACK - Driver VDBox2 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D58h
Name:	Driver VDBox2 Force Wake Ack
ShortName:	DRIVER_VDBOX2_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox2 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox2 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 1 can be powered down (default) 1'b1 : GT Media Slice 1 cannot be powered down

Driver VDBox3 Force Wake Ack

DRIVER_VDBOX3_FWAKE_ACK - Driver VDBox3 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D5Ch
Name:	Driver VDBox3 Force Wake Ack
ShortName:	DRIVER_VDBOX3_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox3 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox3 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 1 can be powered down (default) 1'b1 : GT Media Slice 1 cannot be powered down

Driver VDBox4 Force Wake Ack

DRIVER_VDBOX4_FWAKE_ACK - Driver VDBox4 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D60h
Name:	Driver VDBox4 Force Wake Ack
ShortName:	DRIVER_VDBOX4_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox4 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox4 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 2 can be powered down (default) 1'b1 : GT Media Slice 2 cannot be powered down

Driver VDBox5 Force Wake Ack

DRIVER_VDBOX5_FWAKE_ACK - Driver VDBox5 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D64h
Name:	Driver VDBox5 Force Wake Ack
ShortName:	DRIVER_VDBOX5_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox5 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox5 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 2 can be powered down (default) 1'b1 : GT Media Slice 2 cannot be powered down

Driver VDBox6 Force Wake Ack

DRIVER_VDBOX6_FWAKE_ACK - Driver VDBox6 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D68h
Name:	Driver VDBox6 Force Wake Ack
ShortName:	DRIVER_VDBOX6_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox6 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox6 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 3 can be powered down (default) 1'b1 : GT Media Slice 3 cannot be powered down

Driver VDBox7 Force Wake Ack

DRIVER_VDBOX7_FWAKE_ACK - Driver VDBox7 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D6Ch
Name:	Driver VDBox7 Force Wake Ack
ShortName:	DRIVER_VDBOX7_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox7 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vdbox7 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 3 can be powered down (default) 1'b1 : GT Media Slice 3 cannot be powered down

Driver VEBox0 Force Wake Ack

DRIVER_VEBOX0_FWAKE_ACK - Driver VEBox0 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D70h
Name:	Driver VEBox0 Force Wake Ack
ShortName:	DRIVER_VEBOX0_FWAKE_ACK

This register is used for GPM to handshake the driver's VEBox0 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vebox0 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 0 can be powered down (default) 1'b1 : GT Media Slice 0 cannot be powered down

Driver VEBox1 Force Wake Ack

DRIVER_VEBOX1_FWAKE_ACK - Driver VEBox1 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D74h
Name:	Driver VEBox1 Force Wake Ack
ShortName:	DRIVER_VEBOX1_FWAKE_ACK

This register is used for GPM to handshake the driver's VEBox1 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vebox1 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Slice 1 can be powered down (default) 1'b1 : GT Media Slice 1 cannot be powered down

Driver Vebox2 Force Wake Ack

DRIVER_VEBOX2_FWAKE_ACK - Driver Vebox2 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D78h
Name:	Driver Vebox2 Force Wake Ack
ShortName:	DRIVER_VEBOX2_FWAKE_ACK

This register stores the ACK, from GPMunit, once the driver forcewake has been serviced
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vebox2 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Can be powered down (default) 1'b1 : GT Media cannot be powered down

Driver Vebox3 Force Wake Ack

DRIVER_VEBOX3_FWAKE_ACK - Driver Vebox3 Force Wake Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D7Ch
Name:	Driver Vebox3 Force Wake Ack
ShortName:	DRIVER_VEBOX3_FWAKE_ACK

This register stores the Force wake ACK, from GPM, for driver forcewake to VEBOX3
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**GPM Driver Vebox3 ForceWake Ack** Access: R/W _Custom_GTIReset: BUS 1'b0 : GT Media Can be powered down (default) 1'b1 : GT Media cannot be powered down

DSB_BUFRPT_CNT

DSB_BUFRPT_CNT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B48h-70B4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_0_A
Reset:	soft
Address:	70C48h-70C4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_1_A
Reset:	soft
Address:	70D48h-70D4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_2_A
Reset:	soft
Address:	71B48h-71B4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_0_B
Reset:	soft
Address:	71C48h-71C4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_1_B
Reset:	soft
Address:	71D48h-71D4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_2_B
Reset:	soft
Address:	72B48h-72B4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_0_C
Reset:	soft
Address:	72C48h-72C4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_1_C

DSB_BUFRPT_CNT

Reset:	soft

Address:	72D48h-72D4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_2_C
Reset:	soft

Address:	73B48h-73B4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_0_D
Reset:	soft

Address:	73C48h-73C4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_1_D
Reset:	soft

Address:	73D48h-73D4Bh
Name:	DSB BUFFER REPEAT COUNTER
ShortName:	DSB_BUFRPT_CNT_2_D
Reset:	soft

This register can be updated only before the DSB_CTRL register is programmed to enable the DSB engine.

DWord	Bit	Description
0	31:0	**REPEAT_COUNT** Default Value: 00000008h repeat_value Access: R/W Number of times that the buffer play will be repeated when the Buffer Re-iterate is set in DSB_CTRL register. Do not program this value to 0 if buffer re-iterate is set to 1 in DSB_CTRL register.

DSB_CTRL

DSB_CTRL	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B08h-70B0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_0_A
Reset:	soft
Address:	70C08h-70C0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_1_A
Reset:	soft
Address:	70D08h-70D0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_2_A
Reset:	soft
Address:	71B08h-71B0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_0_B
Reset:	soft
Address:	71C08h-71C0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_1_B
Reset:	soft
Address:	71D08h-71D0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_2_B
Reset:	soft
Address:	72B08h-72B0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_0_C
Reset:	soft
Address:	72C08h-72C0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_1_C

DSB_CTRL

Reset:	soft
Address:	72D08h-72D0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_2_C
Reset:	soft
Address:	73B08h-73B0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_0_D
Reset:	soft
Address:	73C08h-73C0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_1_D
Reset:	soft
Address:	73D08h-73D0Bh
Name:	DSB Control
ShortName:	DSB_CTRL_2_D
Reset:	soft

This register controls the Display State Buffer (DSB) engines.

DWord	Bit	Description
0	31	**DSB Enable** Access: R/W This bit enables the DSB engine. Notes: 1. The act of enabling the DSB engine will not result in the engine to start fetching a state buffer from memory. Only a write to the Tail Pointer will start a fetch 2. A write to the Tail Pointer of the DSB engine will have no affect if the DSB engine is not enabled 3. SW should not update the DSB control registers while DSB engine is not in IDLE state. Bit 0 indicates the status of DSB engine. 4. If SW desires to reset the DSB engine then following sequence can be followed. This sequence is also described in the DSB programming details 1. To reset the DSB engine, SW can set this bit to 0. Bit31 transition from 1 to 0 initiates a reset sequence in the DSB HW. 2. Poll for the DSB status (bit 0) to be in IDLE. 3. If DSB status is 0 then the DSB engine reset sequence is complete and DSB is in reset state.

DSB_CTRL

Value	Name
0b	Disabled
1b	Enabled

30 **Reserved**

Access:	RO
Format:	MBZ

29 **Buffer Reiterate**

Access:	R/W

This bit controls what the DSB engine does when finished with a state buffer program.
If this bit is cleared, then the engine will stop and wait for Software to update the Head/Tail pointers before it starts processing the next state buffer.
If this bit is set, then the engine will start to re-fetch the state buffer defined by the current Head/Tail pointers when it finishes with the current program.
Note that the DSB engine will not take any action on this bit if it is not currently processing a state buffer. I.e. When Software sets this bit on an idle DSB engine, it must then write to the Tail Pointer to start the reiteration process.

Value	Name
0b	Disabled
1b	Enabled

Programming Notes
Software should ensure there is some form of flow control when this bit is set (i.e. the state buffer has a Wait opcode and/or the Wait for VBLANK bit of this register is set)

28 **Wait for VBLANK**

Access:	R/W

This bit controls when the DSB engine starts to fetch a state buffer from memory.
When cleared, then the DSB engine will start fetching the state buffer immediately after Software writes the Tail Pointer
When set, then the DSB engine will start fetching the state buffer only after it sees a rising edge of VBLANK following the write to the Tail Pointer.
SW cannot have both bits 27 and 28 set at the same time.

27 **Wait for Line in Range**

Access:	R/W

This bit controls when the DSB engine starts to fetch a state buffer from memory.
When cleared, then the DSB engine will start fetching the state buffer immediately after Software writes the Tail Pointer
When set, then the DSB engine will start fetching the state buffer only when the scanline falls in the range defined in DSB_LINERANGE_PF register following the write to the Tail Pointer.
SW cannot have both bits 27 and 28 set at the same time.

DSB_CTRL

	26:17	**Reserved** Access: RO Format: MBZ
	16	**DSB Halt** Access: R/W When this bit is set DSB engine will halt. DMA engine will stop generating new memory requests and all the pending instructions in the buffer will be executed and DSB will be halted. The pointers will stop moving. SW can read the DSB_CURRENT_HEAD_PTR register to check the DMA engine pointer status.
	15:9	**Reserved** Access: RO Format: MBZ
	8	**Non Posted Enable** Access: R/W When this bit is set all the MMIO writes including the indexed writes will be non posted to the clients. If SW sets this bit within the DSB program then SW must ensure to include at least 4 NO Ops instructions following this register programming. This is required to allow the register in the DSB to be set correctly.
	7:1	**Reserved** Access: RO Format: MBZ
	0	**DSB Status** Access: RO This field reflects the status of the DSB engine. It is set when the DMA starts to read the state buffer and is cleared when the state buffer is finished and last instruction is completed. **Value** / **Name** 0b – Idle 1b – Busy

DSB_CURRENT_HEAD_PTR

DSB_CURRENT_HEAD_PTR	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	70B2Ch-70B2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_0_A
Reset:	soft
Address:	70C2Ch-70C2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_1_A
Reset:	soft
Address:	70D2Ch-70D2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_2_A
Reset:	soft
Address:	71B2Ch-71B2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_0_B
Reset:	soft
Address:	71C2Ch-71C2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_1_B
Reset:	soft
Address:	71D2Ch-71D2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_2_B
Reset:	soft
Address:	72B2Ch-72B2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_0_C
Reset:	soft
Address:	72C2Ch-72C2Fh
Name:	DSB CURRENT HEAD PTR

DSB_CURRENT_HEAD_PTR

ShortName:	DSB_CURRENT_HEAD_PTR_1_C
Reset:	soft

Address:	72D2Ch-72D2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_2_C
Reset:	soft

Address:	73B2Ch-73B2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_0_D
Reset:	soft

Address:	73C2Ch-73C2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_1_D
Reset:	soft

Address:	73D2Ch-73D2Fh
Name:	DSB CURRENT HEAD PTR
ShortName:	DSB_CURRENT_HEAD_PTR_2_D
Reset:	soft

DWord	Bit	Description
0	31:6	**Head Pointer** Access: RO This register will have the current head pointer of the DSB HW. Driver can read to check the status of the DSB pointer.
	5:0	**Reserved** Access: RO Format: MBZ

DSB_HEAD_PTR

DSB_HEAD_PTR	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B00h-70B03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_0_A
Reset:	soft
Address:	70C00h-70C03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_1_A
Reset:	soft
Address:	70D00h-70D03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_2_A
Reset:	soft
Address:	71B00h-71B03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_0_B
Reset:	soft
Address:	71C00h-71C03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_1_B
Reset:	soft
Address:	71D00h-71D03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_2_B
Reset:	soft
Address:	72B00h-72B03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_0_C
Reset:	soft
Address:	72C00h-72C03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_1_C

DSB_HEAD_PTR

Reset:	soft
Address:	72D00h-72D03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_2_C
Reset:	soft
Address:	73B00h-73B03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_0_D
Reset:	soft
Address:	73C00h-73C03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_1_D
Reset:	soft
Address:	73D00h-73D03h
Name:	DSB Head Pointer
ShortName:	DSB_HEAD_PTR_2_D
Reset:	soft

DWord	Bit	Description
0	31:6	**Head Pointer** Access: R/W This register defines the base address (i.e. head pointer) of the Display State Buffering memory. The address within this register is a graphics address. Restriction : 1. The address is cacheline aligned within this DWord (HW enforced by reserving register bits 5:0) 2. The address should be pointing to the first cacheline of the state buffer 3. Software should not modify this register while the DSB engine is busy
	5:0	**Reserved** Access: RO Format: MBZ

DSB_INTERRUPT

DSB_INTERRUPT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B28h-70B2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_0_A
Reset:	soft
Address:	70C28h-70C2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_1_A
Reset:	soft
Address:	70D28h-70D2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_2_A
Reset:	soft
Address:	71B28h-71B2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_0_B
Reset:	soft
Address:	71C28h-71C2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_1_B
Reset:	soft
Address:	71D28h-71D2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_2_B
Reset:	soft
Address:	72B28h-72B2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_0_C
Reset:	soft
Address:	72C28h-72C2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_1_C

DSB_INTERRUPT

Reset:	soft

Address:	72D28h-72D2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_2_C
Reset:	soft

Address:	73B28h-73B2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_0_D
Reset:	soft

Address:	73C28h-73C2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_1_D
Reset:	soft

Address:	73D28h-73D2Bh
Name:	DSB INTERRUPT
ShortName:	DSB_INTERRUPT_2_D
Reset:	soft

DWord	Bit	Description
0	31	**SPARE_31** Access: R/W
	30	**SPARE_30** Access: R/W
	29	**SPARE_29** Access: R/W
	28	**SPARE_28** Access: R/W
	27	**SPARE_27** Access: R/W
	26	**SPARE_26** Access: R/W
	25	**SPARE_25** Access: R/W
	24	**SPARE_24** Access: R/W
	23	**SPARE_23** Access: R/W

DSB_INTERRUPT		
	22	**SPARE_22** Access: R/W
	21	**SPARE_21** Access: R/W
	20	**SPARE_20** Access: R/W
	19	**DSB_gtt_fault_interrupt_enable** Access: R/W When set the interrupt for gtt faults is enabled. If faults occurs DSB_gtt_fault_interrupt is set.
	18	**DSB_rsptimeout_interrupt_enable** Access: R/W When set the interrupt for response timeout error is enabled. If error occurs DSB_rstimeout_interrupt is set.
	17	**DSB_poll_error_interrupt_enable** Access: R/W When set the interrupt for read poll error is enabled. If error occurs DSB_poll_error_interrupt is set.
	16	**DSB_program_interrupt_enable** Access: R/W When set the interrupt for interrupt instruction is enabled. If program interrupt instruction occurs DSB_program_interrupt is set.
	15	**SPARE_15** Access: R/W
	14	**SPARE_14** Access: R/W
	13	**SPARE_13** Access: R/W
	12	**SPARE_12** Access: R/W
	11	**SPARE_11** Access: R/W
	10	**SPARE_10** Access: R/W
	9	**SPARE_9** Access: R/W

DSB_INTERRUPT

	8	**SPARE_8** Access: R/W
	7	**SPARE_7** Access: R/W
	6	**SPARE_6** Access: R/W
	5	**SPARE_5** Access: R/W
	4	**SPARE_4** Access: R/W
	3	**DSB_gtt_fault_interrupt** Access: R/WC When gtt fault occurs this bit is set. SW must write a 1 to clear this status bit.
	2	**DSB_rsptimeout_interrupt** Access: R/WC When response timeout error occurs this bit is set. SW must write a 1 to clear this status bit.
	1	**DSB_poll_error_interrupt** Access: R/WC When read poll error occurs this bit is set. SW must write a 1 to clear this status bit.
	0	**DSB_program_interrupt** Access: R/WC When program interrupt occurs this bit is set. SW must write a 1 to clear this status bit.

DSB_MMIOCTRL

DSB_MMIOCTRL	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B0Ch-70B0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_0_A
Reset:	soft
Address:	70C0Ch-70C0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_1_A
Reset:	soft
Address:	70D0Ch-70D0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_2_A
Reset:	soft
Address:	71B0Ch-71B0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_0_B
Reset:	soft
Address:	71C0Ch-71C0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_1_B
Reset:	soft
Address:	71D0Ch-71D0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_2_B
Reset:	soft
Address:	72B0Ch-72B0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_0_C
Reset:	soft
Address:	72C0Ch-72C0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_1_C

DSB_MMIOCTRL

Reset:	soft

Address:	72D0Ch-72D0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_2_C
Reset:	soft

Address:	73B0Ch-73B0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_0_D
Reset:	soft

Address:	73C0Ch-73C0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_1_D
Reset:	soft

Address:	73D0Ch-73D0Fh
Name:	DSB MMIO Control
ShortName:	DSB_MMIOCTRL_2_D
Reset:	soft

This register can be updated only before the DSB_CTRL register is programmed to enable the DSB engine.

DWord	Bit	Description
0	31	**DSB HDR meta data delay en** Access: R/W SW must set this bit to 1 and program the bits 15:8 to correct values based on the cd and link clock ratios when DSB is used for HDR meta data transfer. Value: 0b — Name: Delay disabled **[Default]** Value: 1b — Name: Delay enabled
	30:16	**Reserved** Access: RO Format: MBZ
	15:8	**DSB MMIO Dead Clocks Count** Default Value: 00001000b Eight Access: R/W When this counter is enabled by programming bit 31 of this register, DSB will insert programmed number of dead clocks after every 8 back to back MMIO cycles. This is needed to take care of the clock crossing timing issues. Driver must ensure the cdclk/dotclock ratio to adjust the programming. Below is the formula to calculate the number of dead clock programming is as follows. If (cdclk/dotclk) <= 1 then DSB MMIO dead clock count = default value

<table>
<tr><th colspan="3">DSB_MMIOCTRL</th></tr>
<tr><td></td><td></td><td>else if (cdclk/dotclk) > 1 then DSB MMIO dead clock count = 11 *ROUNDUP(cdclk/dotclk)
elseDSB MMIO dead clock count = default value</td></tr>
<tr><td></td><td>7:0</td><td>DSB MMIO Cycles
<table><tr><td>Default Value:</td><td>00001000b Eight</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>These bits can be programmed to change the number of clocks that the DSB engine has control over the MMIO bus. DSB will send programmed number of MMIO cycles before giving away access of RMBUS.</td></tr>
</table>

DSB_PF_LN_LOWER

DSB_PF_LN_LOWER	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B40h-70B43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_0_A
Reset:	soft
Address:	70C40h-70C43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_1_A
Reset:	soft
Address:	70D40h-70D43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_2_A
Reset:	soft
Address:	71B40h-71B43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_0_B
Reset:	soft
Address:	71C40h-71C43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_1_B
Reset:	soft
Address:	71D40h-71D43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_2_B
Reset:	soft
Address:	72B40h-72B43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_0_C
Reset:	soft
Address:	72C40h-72C43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_1_C

DSB_PF_LN_LOWER

Reset:	soft
Address:	72D40h-72D43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_2_C
Reset:	soft
Address:	73B40h-73B43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_0_D
Reset:	soft
Address:	73C40h-73C43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_1_D
Reset:	soft
Address:	73D40h-73D43h
Name:	DSB PREFETCH SCANLINE LOWER LIMIT
ShortName:	DSB_PF_LN_LOWER_2_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Scanline_lower_limit** Access: R/W SW must program this register before Tail pointer is updated if the bit 27 in the DSB_CTRL register is set. This is the lower limit of the scanline number to be compared with the HW line number to start the DSB data prefetch.

DSB_PF_LN_UPPER

DSB_PF_LN_UPPER	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B44h-70B47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_0_A
Reset:	soft
Address:	70C44h-70C47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_1_A
Reset:	soft
Address:	70D44h-70D47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_2_A
Reset:	soft
Address:	71B44h-71B47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_0_B
Reset:	soft
Address:	71C44h-71C47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_1_B
Reset:	soft
Address:	71D44h-71D47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_2_B
Reset:	soft
Address:	72B44h-72B47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_0_C
Reset:	soft
Address:	72C44h-72C47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_1_C

DSB_PF_LN_UPPER

Reset:	soft
Address:	72D44h-72D47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_2_C
Reset:	soft
Address:	73B44h-73B47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_0_D
Reset:	soft
Address:	73C44h-73C47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_1_D
Reset:	soft
Address:	73D44h-73D47h
Name:	DSB PREFETCH SCANLINE UPPER LIMIT
ShortName:	DSB_PF_LN_UPPER_2_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Scanline_upper_limit** Access: R/W SW must program this register before Tail pointer is updated if the bit 27 in the DSB_CTRL register is set. This is the upper limit of the scanline number to be compared with the HW line number to start the DSB data prefetch.

DSB_PMCTRL_2

DSB_PMCTRL_2	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B3Ch-70B3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_0_A
Reset:	soft
Address:	70C3Ch-70C3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_1_A
Reset:	soft
Address:	70D3Ch-70D3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_2_A
Reset:	soft
Address:	71B3Ch-71B3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_0_B
Reset:	soft
Address:	71C3Ch-71C3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_1_B
Reset:	soft
Address:	71D3Ch-71D3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_2_B
Reset:	soft
Address:	72B3Ch-72B3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_0_C
Reset:	soft
Address:	72C3Ch-72C3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_1_C

DSB_PMCTRL_2

Reset:	soft

Address:	72D3Ch-72D3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_2_C
Reset:	soft

Address:	73B3Ch-73B3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_0_D
Reset:	soft

Address:	73C3Ch-73C3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_1_D
Reset:	soft

Address:	73D3Ch-73D3Fh
Name:	DSB POWER MANAGEMENT CONTROL 2
ShortName:	DSB_PMCTRL_2_2_D
Reset:	soft

This register can be updated only before the DSB_CTRL register or it can also be updated within DSB program with appropriate byte enable settings.

DWord	Bit	Description
0	31	**MMIOGEN_DEWAKE_dis** Access: R/W Setting this bit will disable the dewake logic from MMIO generation logic.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**FORCE_DEWAKE** Access: R/W Setting this bit will force a DEWAKE from the DSB engine.
	22:16	**Reserved** Access: RO Format: MBZ
	15	**BLOCK_DEWAKE_EXTENSION** Access: R/W

DSB_PMCTRL_2

Value	Name	Description
0	Extend Dewake	When this bit is set to 0 then the dewake is extended from the time it is set when the Program scanline number in PMCTRL is reached to the point when DSB is done processing all the instructions.
1	Disable Extend Dewake **[Default]**	When this bit is set to 1 then the dewake is not extended and will be de-asserted on a vblank. Dewake then depends on the other logic in DSB.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7 **OVERRIDE_DC5_DC6_OK**

Access:	R/W

Setting this bit will force a DC5 or DC6 OK from the DSB engine.

6:0 **Reserved**

Access:	RO
Format:	MBZ

DSB_PMCTRL

DSB_PMCTRL	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B38h-70B3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_0_A
Reset:	soft
Address:	70C38h-70C3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_1_A
Reset:	soft
Address:	70D38h-70D3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_2_A
Reset:	soft
Address:	71B38h-71B3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_0_B
Reset:	soft
Address:	71C38h-71C3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_1_B
Reset:	soft
Address:	71D38h-71D3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_2_B
Reset:	soft
Address:	72B38h-72B3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_0_C
Reset:	soft
Address:	72C38h-72C3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_1_C

DSB_PMCTRL

Reset:	soft

Address:	72D38h-72D3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_2_C
Reset:	soft

Address:	73B38h-73B3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_0_D
Reset:	soft

Address:	73C38h-73C3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_1_D
Reset:	soft

Address:	73D38h-73D3Bh
Name:	DSB POWER MANAGEMENT CONTROL
ShortName:	DSB_PMCTRL_2_D
Reset:	soft

This register can be updated only before the DSB_CTRL register is programmed to enable the DSB engine.

DWord	Bit	Description
0	31	**Enable DE Wake Generation** Access: R/W Setting this bit to 1 enables the DE wake generation logic based on the scan line number programmed to trigger DE wake.
	30:0	**Scanline number for DE Wake Generation** Access: R/W Scanline number which when reached will trigger a DE wake from DSB if memory is down. 31 bits to cover VRR range

DSB_POLLFUNC

DSB_POLLFUNC	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B10h-70B13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_0_A
Reset:	soft
Address:	70C10h-70C13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_1_A
Reset:	soft
Address:	70D10h-70D13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_2_A
Reset:	soft
Address:	71B10h-71B13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_0_B
Reset:	soft
Address:	71C10h-71C13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_1_B
Reset:	soft
Address:	71D10h-71D13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_2_B
Reset:	soft
Address:	72B10h-72B13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_0_C
Reset:	soft
Address:	72C10h-72C13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_1_C

DSB_POLLFUNC

Reset:	soft
Address:	72D10h-72D13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_2_C
Reset:	soft
Address:	73B10h-73B13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_0_D
Reset:	soft
Address:	73C10h-73C13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_1_D
Reset:	soft
Address:	73D10h-73D13h
Name:	DSB POLL FUNCTION
ShortName:	DSB_POLLFUNC_2_D
Reset:	soft

If poll function is needed, this register should be programmed before the Poll function is used in the DSB program. Can be part of the DSB program itself.

DWord	Bit	Description
0	31	**Poll Enable** This field enables the Poll function in DSB. Value: 0b – Disable **[Default]**; 1b – Enable
	30:23	**Wait in Microseconds** Default Value: 00000010b 2us Access: R/W This field defines the number of micro seconds that DSB will wait before retrying the poll.
	22:15	**Number of times** Default Value: 00110010b 50 times Access: R/W This field defines the number of times that DSB will retry the poll if not satisfied before time out.

DSB_POLLFUNC		
	14:0	**Reserved** Access: RO Format: MBZ

DSB_POLLMASK

DSB_POLLMASK	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B1Ch-70B1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_0_A
Reset:	soft
Address:	70C1Ch-70C1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_1_A
Reset:	soft
Address:	70D1Ch-70D1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_2_A
Reset:	soft
Address:	71B1Ch-71B1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_0_B
Reset:	soft
Address:	71C1Ch-71C1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_1_B
Reset:	soft
Address:	71D1Ch-71D1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_2_B
Reset:	soft
Address:	72B1Ch-72B1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_0_C
Reset:	soft
Address:	72C1Ch-72C1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_1_C

DSB_POLLMASK

Reset:	soft
Address:	72D1Ch-72D1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_2_C
Reset:	soft
Address:	73B1Ch-73B1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_0_D
Reset:	soft
Address:	73C1Ch-73C1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_1_D
Reset:	soft
Address:	73D1Ch-73D1Fh
Name:	DSB POLL MASK
ShortName:	DSB_POLLMASK_2_D
Reset:	soft

If poll function is needed, this register should be programmed before the Poll function is used in the DSB program. Can be part of the DSB program itself.

DWord	Bit	Description
0	31:0	**DSB_POLL_MASK** Access: R/W SW must program these masks bits before the POLL RD instruction is called in the DSB program. This register programming can be part of the DSB program itself and the MMIO write instruction to this register can be placed before the poll read instruction. HW will use these bits mask the bits that are not needed to be compared with the poll read data.

DSB_RM_TIMEOUT

DSB_RM_TIMEOUT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B30h-70B33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_0_A
Reset:	soft
Address:	70C30h-70C33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_1_A
Reset:	soft
Address:	70D30h-70D33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_2_A
Reset:	soft
Address:	71B30h-71B33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_0_B
Reset:	soft
Address:	71C30h-71C33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_1_B
Reset:	soft
Address:	71D30h-71D33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_2_B
Reset:	soft
Address:	72B30h-72B33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_0_C
Reset:	soft
Address:	72C30h-72C33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_1_C

DSB_RM_TIMEOUT

Reset:	soft

Address:	72D30h-72D33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_2_C
Reset:	soft

Address:	73B30h-73B33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_0_D
Reset:	soft

Address:	73C30h-73C33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_1_D
Reset:	soft

Address:	73D30h-73D33h
Name:	DSB RMTIMEOUT
ShortName:	DSB_RM_TIMEOUT_2_D
Reset:	soft

This register can be updated only before the DSB_CTRL register is programmed to enable the DSB engine.

DWord	Bit	Description
0	31	**RM Claim Timeout** Access: R/WC Sticky bit set to 1 when RM hits ready timeout when non posted cycles are enabled in DSB. Clear by writing with a 1.
	30	**RM Ready Timeout** Access: R/WC Sticky bit set to 1 when RM hits claim counter when non posted cycles are enabled in DSB. Clear by writing with a 1.
	29:24	**Reserved** Access: RO Format: MBZ
	23:16	**RM Claim Timeout Count** Default Value: 20h 32 Clocks Access: R/W Number of clocks that DSB will wait for a claim response from clients before generating a claim for error condition.

DSB_RM_TIMEOUT		
	15:0	**RM Ready Timeout Value** Access: R/W This field selects the RM timeout amount in microseconds. **Value** / **Name** FFFFh: 65,535 microseconds **[Default]** 0000h: Timeout disabled

DSB_RMTIMEOUTREG_CAPTURE

DSB_RMTIMEOUTREG_CAPTURE	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B34h-70B37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_0_A
Reset:	soft
Address:	70C34h-70C37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_1_A
Reset:	soft
Address:	70D34h-70D37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_2_A
Reset:	soft
Address:	71B34h-71B37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_0_B
Reset:	soft
Address:	71C34h-71C37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_1_B
Reset:	soft
Address:	71D34h-71D37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_2_B
Reset:	soft
Address:	72B34h-72B37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_0_C
Reset:	soft
Address:	72C34h-72C37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_1_C

DSB_RMTIMEOUTREG_CAPTURE

Reset:	soft

Address:	72D34h-72D37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_2_C
Reset:	soft

Address:	73B34h-73B37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_0_D
Reset:	soft

Address:	73C34h-73C37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_1_D
Reset:	soft

Address:	73D34h-73D37h
Name:	DSB RMTIMEOUT REGISTER ADDRESS CAPTURE
ShortName:	DSB_RMTIMEOUTREG_CAPTURE_2_D
Reset:	soft

This register captures the register on which the RMTIMEOUT error happened.

DWord	Bit	Description
0	31:0	**DSB TIMEOUT REGISTER CAPTURE** Access: RO Offset of the Register that caused RM TIMEOUT.

DSB_STATUS

DSB_STATUS	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B24h-70B27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_0_A
Reset:	soft
Address:	70C24h-70C27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_1_A
Reset:	soft
Address:	70D24h-70D27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_2_A
Reset:	soft
Address:	71B24h-71B27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_0_B
Reset:	soft
Address:	71C24h-71C27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_1_B
Reset:	soft
Address:	71D24h-71D27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_2_B
Reset:	soft
Address:	72B24h-72B27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_0_C
Reset:	soft
Address:	72C24h-72C27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_1_C

DSB_STATUS

Reset:	soft

Address:	72D24h-72D27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_2_C
Reset:	soft

Address:	73B24h-73B27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_0_D
Reset:	soft

Address:	73C24h-73C27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_1_D
Reset:	soft

Address:	73D24h-73D27h
Name:	DSB STATUS
ShortName:	DSB_STATUS_2_D
Reset:	soft

DWord	Bit	Description
0	31	**SPARE_31** Access: RO This bit indicates the status for hp idle state.
	30	**SPARE_30** Access: RO This bit indicates the status of the de wake state.
	29:27	**DSB_REQARB_SM_state** Access: RO Shows the DSB HP requests machine states. IDLE 3'b000 DSB0 3'b001 DSB1 3'b010 DSB2 3'b011
	26	**SPARE_26** Access: RO

DSB_STATUS

		Description This bit indicates the live status of the safe window signal.
	25:23	**DSB_VTDFAULT_ARB_SM_state** Access: RO Shows the DSB VTD Fault arbitration machine states. IDLE_VTD_ERR 3'b000 DSB0_VTD_ERR 3'b001 DSB1_VTD_ERR 3'b010 DSB2_VTD_ERR 3'b011 PIPEDMC_VTD_ERR 3'b100
	22	**SPARE_22** Access: RO Shows bit 2 of DSB_TLBTRANS_SM
	21:20	**DSB_TLBTRANS_SM_state** Access: RO Shows the DSB TLB translation machine states. IDLE 2'b00 INPUT_FIFO_RD 2'b01 WAIT_FOT_VTD 2'b10 OUTPUT_FIFO_WRITE 2'b11
	19	**SPARE_19** Access: R/WC **Description** This bit is set when DSB receives a safe window signal as 1 from dptunit. SW must write a 1 to clear this register bit.
	18:17	**DSB_POINTERS_SM_state** Access: RO Shows the DSB Pointers increment state machine states. IDLE 2'b00 LOAD_HTP 2'b01 INCREMENT_ADDR 2'b10 HALT 2'b11
	16	**SPARE_16** Access: R/WC

DSB_STATUS

		Description This bit is set when DSB is still in non-IDLE state after delayed vblank. SW must write a 1 to clear this register bit.
	15:13	**DSB_MMIO_ARB_SM_state** Access: RO Shows the DSB MMIO arbitor state machine states. MAIN_DMC 3'b000 PIPE_DMC 3'b001 DSB0 3'b010 DSB1 3'b011 DSB2 3'b100
	12	**SPARE_12** Access: RO
	11:7	**DSB_MMIO_INST_SM_state** Access: RO Shows the DSB MMIO Instructions state machine states. IDLE 5'b00000 MMIO_WR 5'b00001 WT_VBLANKS 5'b00010 WT_USEC 5'b00011 WT_LINES 5'b00100 WT_LINES_IN_RANGE 5'b00101 WT_LINES_OUT_OF_RANGE 5'b00110 GENERATE_INT 5'b00111 GENERATE_FRAME_START 5'b01000 WT_FOR_RMBUS_ACCESS 5'b01001 MMIO_INDEXED_WR 5'b01010 INDEXED_EVEN 5'b01011 WT_FOR_VALID_DATA 5'b01100 MMIO_POLL_RD 5'b01101 MMIO_POLL_RD_RECEIVED 5'b01110 WT_POLL_US 5'b01111 POLL_ERROR 5'b10000
	6	**SPARE_6** Access: RO
	5:4	**DSB_reset_SM_state** Access: RO Shows the DSB Reset state machine states. IDLE_RST 2'b00 STOP_REQ_WAIT_FOR_DATA 2'b01 START_SYNC_RESET 2'b10 DEASSERT_SYNC_RESET 2'b11

DSB_STATUS		
	3	**SPARE_3** Access: RO
	2:0	**DSB_run_SM_state** Access: RO Shows the DMA Run state machine states. IDLE 3'b000 DSB_CTRL_UPDATED 3'b001 WT_FOR_VBLANK_SCANLINE_IN_RANGE 3'b010 NOT_WT_FOR_VBLANK_SCANLINE_IN_RANGE 3'b011 VBLANK_LINE_IN_RANGE_HAPPENED 3'b100 DSB_RUN 3'b101

DSB_TAIL_PTR

DSB_TAIL_PTR	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	70B04h-70B07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_0_A
Reset:	soft
Address:	70C04h-70C07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_1_A
Reset:	soft
Address:	70D04h-70D07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_2_A
Reset:	soft
Address:	71B04h-71B07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_0_B
Reset:	soft
Address:	71C04h-71C07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_1_B
Reset:	soft
Address:	71D04h-71D07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_2_B
Reset:	soft
Address:	72B04h-72B07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_0_C
Reset:	soft
Address:	72C04h-72C07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_1_C

DSB_TAIL_PTR

Reset:	soft
Address:	72D04h-72D07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_2_C
Reset:	soft
Address:	73B04h-73B07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_0_D
Reset:	soft
Address:	73C04h-73C07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_1_D
Reset:	soft
Address:	73D04h-73D07h
Name:	DSB Tail Pointer
ShortName:	DSB_TAIL_PTR_2_D
Reset:	soft

DWord	Bit	Description
0	31:6	**Tail Pointer** Access: R/W This register defines the end address (i.e. tail pointer) of the Display Sate Buffer in memory. The address within this register is a graphics address. The act of writing to this register is the event that will activate the DSB engine (i.e. the DSB engine will start fetching the state buffer from memory) as long as the DSB is enabled Restriction : 1. The address is cacheline aligned (HW enforced) 2. The address should be pointing to the cacheline **after** the last cacheline of the state buffer (i.e. Tail Pointer = Number of State Buffer cachelines + 1) 3. This address should be greater than the Head Pointer address 4. Software should not modify this register while the DSB engine is busy
	5:0	**Reserved** Access: RO Format: MBZ

DSC_CRC_CTL

DSC_CRC_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7802Ch-7802Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC0_PA
Reset:	soft
Address:	7812Ch-7812Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC1_PA
Reset:	soft
Address:	7822Ch-7822Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC0_PB
Reset:	soft
Address:	7832Ch-7832Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC1_PB
Reset:	soft
Address:	7842Ch-7842Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC0_PC
Reset:	soft
Address:	7852Ch-7852Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC1_PC
Reset:	soft
Address:	7862Ch-7862Fh
Name:	DSC_CRC_CTL
ShortName:	DSC_CRC_CTL_DSC0_PD
Reset:	soft
Address:	7872Ch-7872Fh
Name:	DSC_CRC_CTL

DSC_CRC_CTL

ShortName: DSC_CRC_CTL_DSC1_PD

Reset: soft

DWord	Bit	Description
0	31	**Enable CRC** Access: R/W Enables the CRC calculations. The CRC will give a done indication and a new result at the end of each frame. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30	**CRC Done** Access: R/WC This bit is set on the rising edge of the CRC done indication. This is a sticky bit, cleared by writing 1b to it. Value: 0b — Name: Not Done Value: 1b — Name: Done
	29	**CRC Change** Access: R/WC This bit is set if the CRC result value changes from the previous value. This is a sticky bit, cleared by writing 1b to it. Value: 0b — Name: No Change Value: 1b — Name: Change
	28:0	**Reserved** Access: RO Format: MBZ

DSC_CRC_RES

DSC_CRC_RES	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	78030h-78033h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC0_PA
Reset:	soft
Address:	78130h-78133h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC1_PA
Reset:	soft
Address:	78230h-78233h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC0_PB
Reset:	soft
Address:	78330h-78333h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC1_PB
Reset:	soft
Address:	78430h-78433h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC0_PC
Reset:	soft
Address:	78530h-78533h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC1_PC
Reset:	soft
Address:	78630h-78633h
Name:	DSC_CRC_RES
ShortName:	DSC_CRC_RES_DSC0_PD
Reset:	soft
Address:	78730h-78733h
Name:	DSC_CRC_RES

DSC_CRC_RES

ShortName: DSC_CRC_RES_DSC1_PD

Reset: soft

DWord	Bit	Description
0	31:0	**CRC Result Value** This field contains the CRC result at the end of a CRC frame. The CRC done bit indicates when the result is valid.

DSC_PICTURE_PARAMETER_SET_0

DSC_PICTURE_PARAMETER_SET_0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78070h-78073h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC0_PA
Reset:	soft
Address:	78170h-78173h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC1_PA
Reset:	soft
Address:	78270h-78273h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC0_PB
Reset:	soft
Address:	78370h-78373h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC1_PB
Reset:	soft
Address:	78470h-78473h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC0_PC
Reset:	soft
Address:	78570h-78573h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC1_PC
Reset:	soft
Address:	78670h-78673h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC0_PD
Reset:	soft
Address:	78770h-78773h
Name:	DSC_PICTURE_PARAMETER_SET_0
ShortName:	DSC_PICTURE_PARAMETER_SET_0_DSC1_PD

DSC_PICTURE_PARAMETER_SET_0

Reset: soft

DWord	Bit	Description
0	31	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for this instance of DSC. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. NOTE: This bit itself is not double buffered Value: 0b – Not Allowed Value: 1b – Allowed
	30:26	**Reserved** Access: RO Format: MBZ
	25:20	**Reserved** Access: RO Format: MBZ
	19	**vbr_enable** Access: R/W Restriction : DSC variable bit rate mode is not supported. Value: 0b – Name: disable **[Default]** – Description: 0 padding bits are stuffed at the end of a slice to ensure that the total number of bits within the slice is equal to the slice bit budget. Value: 1b – Name: Enable – Description: Bit stuffing is bypassed
	18	**enable_422** Access: R/W This bit value shall be 0 if native_422 or native_420 is set to 1. DSC standard calls this mode as simple_422. This mode is currently not supported. Value: 0b – Name: 444 **[Default]** – Description: Input uses 4:4:4 sampling. Decoder does not drop samples to reconstruct a 4:2:2 picture Value: 1b – Name: 422 – Description: Input uses 4:2:2 sampling. Decoder drops samples to reconstruct a 4:2:2 picture.
	17	**convert_rgb** Access: R/W Indicates whether DSC color space conversion is active. Value: 0b – Name: YCbCr – Description: Color space is YCbCr

DSC_PICTURE_PARAMETER_SET_0

1b	convert_rgb	Encoder converts RGB to YCoCg-R, and decoder converts YCoCg-R to RGB.

16 block_pred_enable

Access:	R/W

Value	Name	Description
0b	disable	BP is not used to code any groups within the picture
1b	enable	Decoder must select between BP and MMAP

15:12 linebuf_depth

Access:	R/W

Contains the line buffer bit depth used to generate the bitstream. If a components bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits.
0x8 = 8 bits
0x9 = 9 bits
0xA = 10 bits
0xB = 11 bits
0xC = 12 bits
0xD = 13 bits
All other encodings are RESERVED

11:8 bits_per_component

Access:	R/W

Indicates the number of bits per component for the original pixels of the encoded picture.
0x8 = 8bpc
0xA = 10bpc
0xC = 12bpc
All other encodings are RESERVED

7:4 dsc_version_minor

Access:	R/W

Description
Contains the major version of DSC.

3:0 dsc_version_major

Access:	R/W

Contains the major version of DSC.
0x1 = Encoder implements DSC

DSC_PICTURE_PARAMETER_SET_1

DSC_PICTURE_PARAMETER_SET_1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78074h-78077h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC0_PA
Reset:	soft
Address:	78174h-78177h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC1_PA
Reset:	soft
Address:	78274h-78277h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC0_PB
Reset:	soft
Address:	78374h-78377h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC1_PB
Reset:	soft
Address:	78474h-78477h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC0_PC
Reset:	soft
Address:	78574h-78577h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC1_PC
Reset:	soft
Address:	78674h-78677h
Name:	DSC_PICTURE_PARAMETER_SET_1
ShortName:	DSC_PICTURE_PARAMETER_SET_1_DSC0_PD
Reset:	soft
Address:	78774h-78777h
Name:	DSC_PICTURE_PARAMETER_SET_1

DSC_PICTURE_PARAMETER_SET_1

ShortName: DSC_PICTURE_PARAMETER_SET_1_DSC1_PD

Reset: soft

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:10	**Reserved** Access: RO Format: MBZ
	9:0	**bits_per_pixel** Access: R/W Specifies the target bits/pixel (bpp) rate that is used by the encoder, in steps of 1 bit per pixel. Only values greater than or equal to 6.0 are allowed. If vbr_enable is cleared to 0, this value must be less than or equal to the sustained rate that would apply if MPP is always selected with QP = 0, which is a function of bits_per_component, convert_rgb, and rc_range_parameters[0]. If native_422 or native_420 is set to 1, this value shall be programmed to double the target bits per pixel rate.

DSC_PICTURE_PARAMETER_SET_2

DSC_PICTURE_PARAMETER_SET_2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78078h-7807Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC0_PA
Reset:	soft
Address:	78178h-7817Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC1_PA
Reset:	soft
Address:	78278h-7827Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC0_PB
Reset:	soft
Address:	78378h-7837Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC1_PB
Reset:	soft
Address:	78478h-7847Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC0_PC
Reset:	soft
Address:	78578h-7857Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC1_PC
Reset:	soft
Address:	78678h-7867Bh
Name:	DSC_PICTURE_PARAMETER_SET_2
ShortName:	DSC_PICTURE_PARAMETER_SET_2_DSC0_PD
Reset:	soft
Address:	78778h-7877Bh
Name:	DSC_PICTURE_PARAMETER_SET_2

DSC_PICTURE_PARAMETER_SET_2

ShortName: DSC_PICTURE_PARAMETER_SET_2_DSC1_PD

Reset: soft

DWord	Bit	Description
0	31:16	**pic_width** Access: Double Buffered **Description** Double buffer update will happen at the standard pipe double buffer point. On a single pipe if we are using 1 VDSC instance, picture_width of that VDSC instance = input frame picture_width. On a single pipe if we are using 2 VDSC instances, picture_width of each instance =input frame picture_width divided by 2. In the case a full frame is processed by2*N VDSC instances from N pipes, picture_width of each instance = input framepicture_width divided by 2*N.
	15:0	**pic_height** Access: Double Buffered **Description** Double buffer update will happen at the standard pipe double buffer point. This field is always programmed to input frame picture height.

DSC_PICTURE_PARAMETER_SET_3

DSC_PICTURE_PARAMETER_SET_3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7807Ch-7807Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC0_PA
Reset:	soft
Address:	7817Ch-7817Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC1_PA
Reset:	soft
Address:	7827Ch-7827Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC0_PB
Reset:	soft
Address:	7837Ch-7837Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC1_PB
Reset:	soft
Address:	7847Ch-7847Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC0_PC
Reset:	soft
Address:	7857Ch-7857Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC1_PC
Reset:	soft
Address:	7867Ch-7867Fh
Name:	DSC_PICTURE_PARAMETER_SET_3
ShortName:	DSC_PICTURE_PARAMETER_SET_3_DSC0_PD
Reset:	soft
Address:	7877Ch-7877Fh
Name:	DSC_PICTURE_PARAMETER_SET_3

DSC_PICTURE_PARAMETER_SET_3

ShortName: DSC_PICTURE_PARAMETER_SET_3_DSC1_PD

Reset: soft

DWord	Bit	Description
0	31:16	**slice_width** Access: R/W This defines the width of the slice in number of pixels.
	15:0	**slice_height** Access: R/W This defines the height of the slice in number of pixels.

DSC_PICTURE_PARAMETER_SET_4

DSC_PICTURE_PARAMETER_SET_4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78080h-78083h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC0_PA
Reset:	soft
Address:	78180h-78183h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC1_PA
Reset:	soft
Address:	78280h-78283h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC0_PB
Reset:	soft
Address:	78380h-78383h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC1_PB
Reset:	soft
Address:	78480h-78483h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC0_PC
Reset:	soft
Address:	78580h-78583h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC1_PC
Reset:	soft
Address:	78680h-78683h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC0_PD
Reset:	soft
Address:	78780h-78783h
Name:	DSC_PICTURE_PARAMETER_SET_4
ShortName:	DSC_PICTURE_PARAMETER_SET_4_DSC1_PD

DSC_PICTURE_PARAMETER_SET_4		
Reset: soft		
DWord	**Bit**	**Description**
0	31:16	**initial_dec_delay** Access: R/W
	15:10	**Reserved** Access: RO Format: MBZ
	9:0	**initial_xmit_delay** Access: R/W

DSC_PICTURE_PARAMETER_SET_5

DSC_PICTURE_PARAMETER_SET_5	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78084h-78087h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC0_PA
Reset:	soft
Address:	78184h-78187h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC1_PA
Reset:	soft
Address:	78284h-78287h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC0_PB
Reset:	soft
Address:	78384h-78387h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC1_PB
Reset:	soft
Address:	78484h-78487h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC0_PC
Reset:	soft
Address:	78584h-78587h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC1_PC
Reset:	soft
Address:	78684h-78687h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC0_PD
Reset:	soft
Address:	78784h-78787h
Name:	DSC_PICTURE_PARAMETER_SET_5
ShortName:	DSC_PICTURE_PARAMETER_SET_5_DSC1_PD

DSC_PICTURE_PARAMETER_SET_5

Reset: soft

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27:16	**scale_decrement_interval** Access: R/W
	15:0	**scale_increment_interval** Access: R/W

DSC_PICTURE_PARAMETER_SET_6

DSC_PICTURE_PARAMETER_SET_6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78088h-7808Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC0_PA
Reset:	soft
Address:	78188h-7818Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC1_PA
Reset:	soft
Address:	78288h-7828Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC0_PB
Reset:	soft
Address:	78388h-7838Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC1_PB
Reset:	soft
Address:	78488h-7848Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC0_PC
Reset:	soft
Address:	78588h-7858Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC1_PC
Reset:	soft
Address:	78688h-7868Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC0_PD
Reset:	soft
Address:	78788h-7878Bh
Name:	DSC_PICTURE_PARAMETER_SET_6
ShortName:	DSC_PICTURE_PARAMETER_SET_6_DSC1_PD

DSC_PICTURE_PARAMETER_SET_6

Reset: soft

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:24	**flatness_max_qp** Access: R/W
	23:21	**Reserved** Access: RO Format: MBZ
	20:16	**flatness_min_qp** Access: R/W
	15:13	**Reserved** Access: RO Format: MBZ
	12:8	**first_line_bpg_offset** Access: R/W
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**initial_scale_value** Access: R/W Specifies the initial rcXformScale factor value used at the beginning of a slice. This is an unsigned field with three fractional bits.

DSC_PICTURE_PARAMETER_SET_7

DSC_PICTURE_PARAMETER_SET_7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7808Ch-7808Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC0_PA
Reset:	soft
Address:	7818Ch-7818Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC1_PA
Reset:	soft
Address:	7828Ch-7828Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC0_PB
Reset:	soft
Address:	7838Ch-7838Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC1_PB
Reset:	soft
Address:	7848Ch-7848Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC0_PC
Reset:	soft
Address:	7858Ch-7858Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC1_PC
Reset:	soft
Address:	7868Ch-7868Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC0_PD
Reset:	soft
Address:	7878Ch-7878Fh
Name:	DSC_PICTURE_PARAMETER_SET_7
ShortName:	DSC_PICTURE_PARAMETER_SET_7_DSC1_PD

DSC_PICTURE_PARAMETER_SET_7		
Reset:	soft	
DWord	**Bit**	**Description**
0	31:16	**nfl_bpg_offset** Access: R/W Specifies the number of bits (including fractional bits) that are deallocated for each group, for groups after the first line of a slice. This is an unsigned value with 11 fractional bits.
	15:0	**slice_bpg_offset** Access: R/W Specifies the number of bits (including fractional bits) that are deallocated for each group to enforce the slice constraint (i.e., the final buffer model fullness cannot exceed the initial transmission delay times bits per group), while allowing a programmable initial_offset. This is an unsigned value with 11 fractional bits.

DSC_PICTURE_PARAMETER_SET_8

DSC_PICTURE_PARAMETER_SET_8	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78090h-78093h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC0_PA
Reset:	soft
Address:	78190h-78193h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC1_PA
Reset:	soft
Address:	78290h-78293h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC0_PB
Reset:	soft
Address:	78390h-78393h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC1_PB
Reset:	soft
Address:	78490h-78493h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC0_PC
Reset:	soft
Address:	78590h-78593h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC1_PC
Reset:	soft
Address:	78690h-78693h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC0_PD
Reset:	soft
Address:	78790h-78793h
Name:	DSC_PICTURE_PARAMETER_SET_8
ShortName:	DSC_PICTURE_PARAMETER_SET_8_DSC1_PD

DSC_PICTURE_PARAMETER_SET_8		
Reset: soft		
DWord	**Bit**	**Description**
0	31:16	**initial_offset** Access: R/W
	15:0	**final_offset** Access: R/W

DSC_PICTURE_PARAMETER_SET_9

DSC_PICTURE_PARAMETER_SET_9	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78094h-78097h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC0_PA
Reset:	soft
Address:	78194h-78197h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC1_PA
Reset:	soft
Address:	78294h-78297h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC0_PB
Reset:	soft
Address:	78394h-78397h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC1_PB
Reset:	soft
Address:	78494h-78497h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC0_PC
Reset:	soft
Address:	78594h-78597h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC1_PC
Reset:	soft
Address:	78694h-78697h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC0_PD
Reset:	soft
Address:	78794h-78797h
Name:	DSC_PICTURE_PARAMETER_SET_9
ShortName:	DSC_PICTURE_PARAMETER_SET_9_DSC1_PD

DSC_PICTURE_PARAMETER_SET_9

Reset: soft

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:16	**rc_edge_factor** Access: R/W
	15:0	**rc_model_Size** Access: R/W

DSC_PICTURE_PARAMETER_SET_10

DSC_PICTURE_PARAMETER_SET_10	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78098h-7809Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC0_PA
Reset:	soft
Address:	78198h-7819Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC1_PA
Reset:	soft
Address:	78298h-7829Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC0_PB
Reset:	soft
Address:	78398h-7839Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC1_PB
Reset:	soft
Address:	78498h-7849Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC0_PC
Reset:	soft
Address:	78598h-7859Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC1_PC
Reset:	soft
Address:	78698h-7869Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC0_PD
Reset:	soft
Address:	78798h-7879Bh
Name:	DSC_PICTURE_PARAMETER_SET_10
ShortName:	DSC_PICTURE_PARAMETER_SET_10_DSC1_PD

DSC_PICTURE_PARAMETER_SET_10

Reset: soft

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:20	**rc_tgt_offset_lo** Access: R/W
	19:16	**rc_tgt_offset_hi** Access: R/W
	15:13	**Reserved** Access: RO Format: MBZ
	12:8	**rc_quant_incr_limit1** Access: R/W
	7:5	**Reserved** Access: RO Format: MBZ
	4:0	**rc_quant_incr_limit0** Access: R/W

DSC_PICTURE_PARAMETER_SET_11

DSC_PICTURE_PARAMETER_SET_11	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7809Ch-7809Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC0_PA
Reset:	soft
Address:	7819Ch-7819Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC1_PA
Reset:	soft
Address:	7829Ch-7829Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC0_PB
Reset:	soft
Address:	7839Ch-7839Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC1_PB
Reset:	soft
Address:	7849Ch-7849Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC0_PC
Reset:	soft
Address:	7859Ch-7859Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC1_PC
Reset:	soft
Address:	7869Ch-7869Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC0_PD
Reset:	soft
Address:	7879Ch-7879Fh
Name:	DSC_PICTURE_PARAMETER_SET_11
ShortName:	DSC_PICTURE_PARAMETER_SET_11_DSC1_PD

DSC_PICTURE_PARAMETER_SET_11		
Reset: soft		
DWord	**Bit**	**Description**
0	31:0	**Reserved** Access: RO Format: MBZ

DSC_PICTURE_PARAMETER_SET_12

DSC_PICTURE_PARAMETER_SET_12	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	780A0h-780A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC0_PA
Reset:	soft
Address:	781A0h-781A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC1_PA
Reset:	soft
Address:	782A0h-782A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC0_PB
Reset:	soft
Address:	783A0h-783A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC1_PB
Reset:	soft
Address:	784A0h-784A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC0_PC
Reset:	soft
Address:	785A0h-785A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC1_PC
Reset:	soft
Address:	786A0h-786A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC0_PD
Reset:	soft
Address:	787A0h-787A3h
Name:	DSC_PICTURE_PARAMETER_SET_12
ShortName:	DSC_PICTURE_PARAMETER_SET_12_DSC1_PD

DSC_PICTURE_PARAMETER_SET_12		
Reset: soft		
DWord	**Bit**	**Description**
0	31:0	**Reserved** Access: RO Format: MBZ

DSC_PICTURE_PARAMETER_SET_13

DSC_PICTURE_PARAMETER_SET_13	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	780A4h-780A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC0_PA
Reset:	soft
Address:	781A4h-781A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC1_PA
Reset:	soft
Address:	782A4h-782A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC0_PB
Reset:	soft
Address:	783A4h-783A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC1_PB
Reset:	soft
Address:	784A4h-784A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC0_PC
Reset:	soft
Address:	785A4h-785A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC1_PC
Reset:	soft
Address:	786A4h-786A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC0_PD
Reset:	soft
Address:	787A4h-787A7h
Name:	DSC_PICTURE_PARAMETER_SET_13
ShortName:	DSC_PICTURE_PARAMETER_SET_13_DSC1_PD

DSC_PICTURE_PARAMETER_SET_13		
Reset: soft		
DWord	**Bit**	**Description**
0	31:0	**Reserved** Access: RO Format: MBZ

DSC_PICTURE_PARAMETER_SET_14

DSC_PICTURE_PARAMETER_SET_14	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	780A8h-780ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC0_PA
Reset:	soft
Address:	781A8h-781ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC1_PA
Reset:	soft
Address:	782A8h-782ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC0_PB
Reset:	soft
Address:	783A8h-783ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC1_PB
Reset:	soft
Address:	784A8h-784ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC0_PC
Reset:	soft
Address:	785A8h-785ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC1_PC
Reset:	soft
Address:	786A8h-786ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC0_PD
Reset:	soft
Address:	787A8h-787ABh
Name:	DSC_PICTURE_PARAMETER_SET_14
ShortName:	DSC_PICTURE_PARAMETER_SET_14_DSC1_PD

DSC_PICTURE_PARAMETER_SET_14		
Reset: soft		
DWord	**Bit**	**Description**
0	31:0	**Reserved** Access: RO Format: MBZ

DSC_PICTURE_PARAMETER_SET_15

DSC_PICTURE_PARAMETER_SET_15	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	780ACh-780AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC0_PA
Reset:	soft
Address:	781ACh-781AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC1_PA
Reset:	soft
Address:	782ACh-782AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC0_PB
Reset:	soft
Address:	783ACh-783AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC1_PB
Reset:	soft
Address:	784ACh-784AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC0_PC
Reset:	soft
Address:	785ACh-785AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC1_PC
Reset:	soft
Address:	786ACh-786AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC0_PD
Reset:	soft
Address:	787ACh-787AFh
Name:	DSC_PICTURE_PARAMETER_SET_15
ShortName:	DSC_PICTURE_PARAMETER_SET_15_DSC1_PD

DSC_PICTURE_PARAMETER_SET_15		
Reset: soft		
DWord	**Bit**	**Description**
0	31:0	**Reserved** Access: RO Format: MBZ

DSC_PICTURE_PARAMETER_SET_16

DSC_PICTURE_PARAMETER_SET_16	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	780B0h-780B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC0_PA
Reset:	soft
Address:	781B0h-781B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC1_PA
Reset:	soft
Address:	782B0h-782B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC0_PB
Reset:	soft
Address:	783B0h-783B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC1_PB
Reset:	soft
Address:	784B0h-784B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC0_PC
Reset:	soft
Address:	785B0h-785B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC1_PC
Reset:	soft
Address:	786B0h-786B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC0_PD
Reset:	soft
Address:	787B0h-787B3h
Name:	DSC_PICTURE_PARAMETER_SET_16
ShortName:	DSC_PICTURE_PARAMETER_SET_16_DSC1_PD

DSC_PICTURE_PARAMETER_SET_16

Reset: soft

DWord	Bit	Description
0	31:20	**slice_row_per_frame** Access: Double Buffered **Description** Double buffer update will happen at the standard pipe double buffer point. This is the field driver will program to indicate slice_row_per_frame for full frame. There is another field in DSC_PICTURE_PARAMETER_SET_1 to indicate slice_row_per_frame based onPSR2 SU region size. This field indicates number of slices stacked in the vertical direction. Example: Input to DSS unit: 3840x2160 to be compressed as 4 slices Input to each VDSC instance: 1920x2160 slice_per_line: 1 slice_row_per_frame: 2
	19	**Reserved** Access: RO Format: MBZ
	18:16	**slice_per_line** Access: R/W Refer to the description under slice_row_per_frame.
	15:0	**slice_chunk_size** Access: R/W

DSC_RC_BUF_THRESH_0

DSC_RC_BUF_THRESH_0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	78054h-7805Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC0_PA
Reset:	soft
Address:	78154h-7815Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC1_PA
Reset:	soft
Address:	78254h-7825Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC0_PB
Reset:	soft
Address:	78354h-7835Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC1_PB
Reset:	soft
Address:	78454h-7845Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC0_PC
Reset:	soft
Address:	78554h-7855Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC1_PC
Reset:	soft
Address:	78654h-7865Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC0_PD
Reset:	soft
Address:	78754h-7875Bh
Name:	DSC_RC_BUF_THRESH_0
ShortName:	DSC_RC_BUF_THRESH_0_DSC1_PD

DSC_RC_BUF_THRESH_0		
Reset: soft		
DWord	**Bit**	**Description**
0	31:24	**rc_buf_thresh_3** Access: R/W
	23:16	**rc_buf_thresh_2** Access: R/W
	15:8	**rc_buf_thresh_1** Access: R/W
	7:0	**rc_buf_thresh_0** Access: R/W
1	31:24	**rc_buf_thresh_7** Access: R/W
	23:16	**rc_buf_thresh_6** Access: R/W
	15:8	**rc_buf_thresh_5** Access: R/W
	7:0	**rc_buf_thresh_4** Access: R/W

DSC_RC_BUF_THRESH_1

DSC_RC_BUF_THRESH_1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	7805Ch-78063h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC0_PA
Reset:	soft
Address:	7815Ch-78163h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC1_PA
Reset:	soft
Address:	7825Ch-78263h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC0_PB
Reset:	soft
Address:	7835Ch-78363h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC1_PB
Reset:	soft
Address:	7845Ch-78463h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC0_PC
Reset:	soft
Address:	7855Ch-78563h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC1_PC
Reset:	soft
Address:	7865Ch-78663h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC0_PD
Reset:	soft
Address:	7875Ch-78763h
Name:	DSC_RC_BUF_THRESH_1
ShortName:	DSC_RC_BUF_THRESH_1_DSC1_PD

DSC_RC_BUF_THRESH_1		
Reset: soft		
DWord	**Bit**	**Description**
0	31:24	**rc_buf_thresh_11** Access: R/W
	23:16	**rc_buf_thresh_10** Access: R/W
	15:8	**rc_buf_thresh_9** Access: R/W
	7:0	**rc_buf_thresh_8** Access: R/W
1	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**rc_buf_thresh_13** Access: R/W
	7:0	**rc_buf_thresh_12** Access: R/W

DSC_RC_RANGE_PARAMETERS_0

DSC_RC_RANGE_PARAMETERS_0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	78008h-7800Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC0_PA
Reset:	soft
Address:	78108h-7810Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC1_PA
Reset:	soft
Address:	78208h-7820Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC0_PB
Reset:	soft
Address:	78308h-7830Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC1_PB
Reset:	soft
Address:	78408h-7840Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC0_PC
Reset:	soft
Address:	78508h-7850Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC1_PC
Reset:	soft
Address:	78608h-7860Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC0_PD
Reset:	soft
Address:	78708h-7870Fh
Name:	DSC_RC_RANGE_PARAMETERS_0
ShortName:	DSC_RC_RANGE_PARAMETERS_0_DSC1_PD

DSC_RC_RANGE_PARAMETERS_0		
Reset: soft		
DWord	**Bit**	**Description**
0	31:26	**rc_bpg_offset_1** Access: R/W
	25:21	**rc_max_qp_1**
	20:16	**rc_min_qp_1**
	15:10	**rc_bpg_offset_0** Access: R/W
	9:5	**rc_max_qp_0**
	4:0	**rc_min_qp_0**
1	31:26	**rc_bpg_offset_3** Access: R/W
	25:21	**rc_max_qp_3**
	20:16	**rc_min_qp_3**
	15:10	**rc_bpg_offset_2** Access: R/W
	9:5	**rc_max_qp_2**
	4:0	**rc_min_qp_2**

DSC_RC_RANGE_PARAMETERS_1

DSC_RC_RANGE_PARAMETERS_1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	78010h-78017h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC0_PA
Reset:	soft
Address:	78110h-78117h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC1_PA
Reset:	soft
Address:	78210h-78217h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC0_PB
Reset:	soft
Address:	78310h-78317h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC1_PB
Reset:	soft
Address:	78410h-78417h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC0_PC
Reset:	soft
Address:	78510h-78517h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC1_PC
Reset:	soft
Address:	78610h-78617h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC0_PD
Reset:	soft
Address:	78710h-78717h
Name:	DSC_RC_RANGE_PARAMETERS_1
ShortName:	DSC_RC_RANGE_PARAMETERS_1_DSC1_PD

DSC_RC_RANGE_PARAMETERS_1		
Reset: soft		
DWord	**Bit**	**Description**
0	31:26	**rc_bpg_offset_5** Access: R/W
	25:21	**rc_max_qp_5**
	20:16	**rc_min_qp_5**
	15:10	**rc_bpg_offset_4** Access: R/W
	9:5	**rc_max_qp_4**
	4:0	**rc_min_qp_4**
1	31:26	**rc_bpg_offset_7** Access: R/W
	25:21	**rc_max_qp_7**
	20:16	**rc_min_qp_7**
	15:10	**rc_bpg_offset_6** Access: R/W
	9:5	**rc_max_qp_6**
	4:0	**rc_min_qp_6**

DSC_RC_RANGE_PARAMETERS_2

DSC_RC_RANGE_PARAMETERS_2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	78018h-7801Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC0_PA
Reset:	soft
Address:	78118h-7811Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC1_PA
Reset:	soft
Address:	78218h-7821Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC0_PB
Reset:	soft
Address:	78318h-7831Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC1_PB
Reset:	soft
Address:	78418h-7841Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC0_PC
Reset:	soft
Address:	78518h-7851Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC1_PC
Reset:	soft
Address:	78618h-7861Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC0_PD
Reset:	soft
Address:	78718h-7871Fh
Name:	DSC_RC_RANGE_PARAMETERS_2
ShortName:	DSC_RC_RANGE_PARAMETERS_2_DSC1_PD

DSC_RC_RANGE_PARAMETERS_2		
Reset: soft		
DWord	**Bit**	**Description**
0	31:26	**rc_bpg_offset_9** Access: R/W
	25:21	**rc_max_qp_9**
	20:16	**rc_min_qp_9**
	15:10	**rc_bpg_offset_8** Access: R/W
	9:5	**rc_max_qp_8**
	4:0	**rc_min_qp_8**
1	31:26	**rc_bpg_offset_11** Access: R/W
	25:21	**rc_max_qp_11**
	20:16	**rc_min_qp_11**
	15:10	**rc_bpg_offset_10** Access: R/W
	9:5	**rc_max_qp_10**
	4:0	**rc_min_qp_10**

DSC_RC_RANGE_PARAMETERS_3

DSC_RC_RANGE_PARAMETERS_3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	78020h-78027h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC0_PA
Reset:	soft
Address:	78120h-78127h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC1_PA
Reset:	soft
Address:	78220h-78227h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC0_PB
Reset:	soft
Address:	78320h-78327h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC1_PB
Reset:	soft
Address:	78420h-78427h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC0_PC
Reset:	soft
Address:	78520h-78527h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC1_PC
Reset:	soft
Address:	78620h-78627h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC0_PD
Reset:	soft
Address:	78720h-78727h
Name:	DSC_RC_RANGE_PARAMETERS_3
ShortName:	DSC_RC_RANGE_PARAMETERS_3_DSC1_PD

DSC_RC_RANGE_PARAMETERS_3		
Reset: soft		
DWord	**Bit**	**Description**
0	31:26	**rc_bpg_offset_13** Access: R/W
	25:21	**rc_max_qp_13**
	20:16	**rc_min_qp_13**
	15:10	**rc_bpg_offset_12** Access: R/W
	9:5	**rc_max_qp_12**
	4:0	**rc_min_qp_12**
1	31:16	**Reserved** Access: RO Format: MBZ
	15:10	**rc_bpg_offset_14** Access: R/W
	9:5	**rc_max_qp_14**
	4:0	**rc_min_qp_14**

DSI_CALIB_TO

DSI_CALIB_TO	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	6B050h-6B053h
Name:	DSI 0 Calibration Timeout
ShortName:	DSI_CALIB_TO_0
Reset:	soft
Address:	6B850h-6B853h
Name:	DSI 1 Calibration Timeout
ShortName:	DSI_CALIB_TO_1
Reset:	soft

This register specifies the amount of time that the Host will drive the Link with the HS calibration sequence. The values are specified in Byte clocks and the values specified should be zero based (i.e. value of 1 = 2 Byte clocks, value of 2 = 3 Byte clocks, etc.)

Restriction: The timeout values should be greater than zero if the respective calibration type is enabled.

DWord	Bit	Description
0	31:20	**Periodic Calibration Timeout** Default Value: 07Fh Access: R/W This field represents the amount of time that the Host will give to transmitting the HS calibration sequence for Periodic Calibrations. The transcoder will ignore this field if Periodic Calibration is not enabled within the TRANS_DSI_FUNC_CONF register. The default value will be set to 128 Byte clocks Restriction: When periodic calibration is enabled in Video Mode, the Horizontal size between synchronous packets must be great enough to support the HS calibration burst without the loss of synchronous packets. Software will need to ensure that the following equation is met to prevent synchronization packet loss: Periodic Calib Duration < (H. Size * Bits per Pixel) / (Link Width * 8) 16*N Notes: 1. The "H. Size" term is dependent on the mode of operation (i.e. Sync Pulse or Sync Event). In Sync Pulse, H. Size = H. Sync Start + (H. Total H. Sync End). In Sync Event, H. Size = H. Total. 2. HS bursts and calibrations cannot be concatenated together on Data Lanes which means the Data Lanes have to enter the LP state on either end of the calibration. The 16*N term within the equation is used to account for the HS to HS latency of transitioning the Data Lanes on either end of the calibration.The variable N is the number of Byte clocks within

DSI_CALIB_TO		
		an Escape clock (N = ceiling(((8X Frequency (in MHz) / 20 MHz) / 8))
	19:16	**Reserved** Access: RO Format: MBZ
	15:0	**Initial Calibration Timeout** Default Value: 0FFFh Access: R/W This field represents the amount of time the Host will give to transmitting the HS calibration sequence for the Initial Calibration, if enabled. The transcoder will ignore this field if Calibration is not enabled within the TRANS_DSI_FUNC_CONF register. The default value will be set to 4096 Byte clocks

DSI_CLK_TIMING_PARAM

DSI_CLK_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B080h-6B083h
Name:	DSI 0 Clock Lane Timing Parameter
ShortName:	DSI_CLK_TIMING_PARAM_0
Reset:	soft
Address:	6B880h-6B883h
Name:	DSI 1 Clock Lane Timing Parameter
ShortName:	DSI_CLK_TIMING_PARAM_1
Reset:	soft

This register specifies the D-PHY timing parameters for the Clock Lane, if SW is overriding the HW defaults.
This register is located within the Core Display and is used by the DSI Controller to calculate Link transition latencies of the Clock Lane. There is an identical register (DPHY_CLK_TIMING_PARAM) located within the combo-PHY that actually applies the overrides to the D-PHY Clock Lane. Both registers should be programmed by Software if an override needs to be applied to the Clock Lane within the D-PHY.
Since this register is being used to calculate the Link transition latencies of the Clock Lane, but does not actually affect the transition times within the D-PHY, this register can be used to add guardbands to the DSI Controller's transition latency calculations.
The lower 12 bits of the offset address for this register should correspond to the lower offset address of its sister D-PHY register within the combo-PHY.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
The programming of this register must be equal to or greater than the programming of its sister register that lives within the combo-PHY (DPHY_CLK_TIMING_PARAM).

DWord	Bit	Description
0	31	**CLK_PREPARE Override** Access: R/W This field controls the override of the CLK-PREPARE timing parameter. 0b: HW maintains **[Default]** 1b: SW overrides
	30:28	**CLK_PREPARE** Access: R/W This parameter defines the time that the Host drives the Clock Lane with the LP-00 Lane state (the Bridge state) immediately before the HS-0 Line state.

DSI_CLK_TIMING_PARAM

This field represents a hexadecimal value with a precision of 1.2 i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this timing parameter at1 Escape clock (minimum50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.00 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 95ns for this parameter.

27 **CLK_ZERO Override**

Access:	R/W

This field controls the override of the CLK-ZERO timing parameter

Value	Name
0	HW Maintains
1	SW overrides

26:24 **Reserved**

Access:	RO
Format:	MBZ

23:20 **CLK_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane.
HW maintains this parameter at 5 Escape clocks (minimum250ns)

19 **CLK_PRE Override**

Access:	R/W

This field controls the override of the CLK-PRE timing parameter.

Value	Name
0	HW Maintains
1	SW overrides

18 **Reserved**

Access:	RO
Format:	MBZ

DSI_CLK_TIMING_PARAM

	17:16	**CLK_PRE** Access: R/W This parameter defines the time that the HS clock shall be driven by the Host prior to any Data Lane beginning its transition from the LP state to the HS state. HW maintains this parameter at 8 UI (1 Byte clock). This field will override the parameter with a value measured in Escape clocks which will be much greater than 8 UI.
	15	**CLK_POST Override** Access: R/W This field controls the override of the CLK-POST timing parameter Value: 0 — Name: HW Maintains Value: 1 — Name: SW overrides
	14:11	**Reserved** Access: RO Format: MBZ
	10:8	**CLK_POST** Access: R/W This parameter defines the time the Host continues to transmit the HS clock after the last Data Lane has transitioned to the LP state. HW maintains this parameter at 1.25 Escape clocks plus 7 Byte clocks (minimum62.5ns + 56 UI)
	7	**CLK_TRAIL Override** Access: R/W This field controls the override of the CLK-TRAIL timing parameter Value: 0 — Name: HW Maintains Value: 1 — Name: SW overrides
	6:3	**Reserved** Access: RO Format: MBZ
	2:0	**CLK_TRAIL** Access: R/W This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane after the CLK-POST time has been achieved. HW maintains this parameter at 1.25 Escape clocks (minimum 62.5ns)

DSI_CMD_FRMCTL

DSI_CMD_FRMCTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B034h-6B037h
Name:	DSI Transcoder 0 Command Mode Frame Control
ShortName:	DSI_CMD_FRMCTL_0
Reset:	soft
Address:	6B834h-6B837h
Name:	DSI Transcoder 1 Command Mode Frame Control
ShortName:	DSI_CMD_FRMCTL_1
Reset:	soft

This register is used to control initiating frame updates to the Peripheral in Command Mode
The fields within this register are only observed by the DSI transcoder when it is in the Command Mode of operation

DWord	Bit	Description
0	31	**Frame Update Request** Access: R/W Set This bit controls when the transcoder will start the next frame when it is in Command Mode. The transcoder will act on this bit only when it is in the Command Mode and the Transcoder is enabled (TRANS_CONF). Software can write to this bit, but Hardware will be responsible for clearing it. 0b – No frame request present 1b – Frame request present
	30	**Reserved** Access: RO Format: MBZ
	29	**Periodic Frame Update Enable** Access: R/W When the Intel graphics driver is not present (e.g. the driver is uninstalled, the OS basic driver is present, or pre-boot time) there will be no frame update requests to the DSI transcoder through the Frame Update Request of this register. Therefore, this field will enable a mechanism that will initiate periodic frame update requests when TE events are received from the Panel. When enabling this feature, the expectation will be that SW has configured the Panel to send TE events to the Host (i.e. set_tear_on, etc.). HW will do the following when this bit is set: 1. It will override the TE Source bit of the TRANS_DSI_FUNC_CONF register to the GPIO setting. The DSI transcoder HW does not have a mechanism to automatically send Bus

Turn-Arounds to the Panel to receive in-band TE events

2. It will override the Mode of Operation of the TRANS_DSI_FUNC_CONF register to a non-gating Command Mode of operation

Value	Name
0b	Periodic Frame Update disabled
1b	Periodic Frame Update Enabled

Programming Notes
Note that when the Takeover MIPI DBI bit is set within the MSG_MEDE_KVMR_SPR_CTL register then HW will do the following if the DSI transcoder is operating in a Command Mode (i.e. DBI): 1. It will enable the Periodic Frame Update mode of operation 2. It will override the TE Source bit of the TRANS_DSI_FUNC_CONF register to the GPIO setting 3. It will override the Mode of Operation of the TRANS_DSI_FUNC_CONF register to a non-gating Command Mode of operation If the DSI transcoder is not operating in a DBI mode, then the transcoder will ignore the Takeover MIPI DBI bit.

28 **Null Packet Enable**

Access:	R/W

This bit controls whether Null Packets will be transmitted between Pixel Packets in Command Mode operation.
If a Pixel Packet ends and the next Pixel Packet is within the transcoders pipeline but not visible to the HS arbiter, then the transcoder will begin transmitting Null Packet bursts to keep the Link in the HS state.
If the current Pixel Packet ends and the next Pixel Packet is not within the transcoders pipeline, then the transcoder will allow the Link to enter the LP state.
This field is ignored when the transcoder is operating in Video Mode.

Value	Name
0b	Null packet injection disabled
1b	Null packet injection enabled

27 **Single Panel Update**

Access:	R/W

This is an attribute applied to the Frame Update Request bit.
When this transcoder is synchronized to another transcoder in Dual Link Dual Pipe Sync mode (i.e. both Port Sync Mode Enable and Dual Pipe Sync Enable are set), then this bit controls whether this transcoder waits for the other port to receive its Frame Update Request and TE event (i.e. both Panels are going to receive a frame), or whether this transcoder just waits for the other transcoders TE event (i.e. just this Panel is going to receive a frame)

Value	Name
0b	Dual Panel update

1b	Single Panel update

Programming Notes

1. HW only acts on this bit if the Port Sync Mode Enable is set for this transcoder. If the transcoders Port Sync Enable is not set, then a Frame Update Request is implicitly a single Panel update. The difference is that a non-synchronized transcoder will not wait for TE events from another port.
2. If this bit is set and the Port Sync Enable bit is set, then it is the responsibility of SW to ensure that the Panel for the other transcoder is generating TE events
3. Setting this bit should be mutually exclusive with the other Frame Update Request attributes Accumulate Frame Update Request and Forward Frame Update Request

26 **Accumulate Frame Update Requests**

Access:	R/W Set

This is an attribute applied to the Frame Update Request bit.
This bit will control whether two synchronized transcoders in a Dual Link - Dual Pipe mode of operation will synchronize the Frame Update Requests to each transcoder (i.e. the Frame Start to the two Pipes will be sent out from each transcoder at the same time)
HW will clear this bit when the V. Blank for this transcoder is observed

Value	Name
0b	No Accumulation
1b	Accumulate

Programming Notes

1. HW only acts on this attribute if:
   a. The Port Sync Enable is set for both transcoders
   b. The transcoders are in a Dual Link Dual Pipe sync mode
2. For Dual Link Single Pipe sync mode (i.e. Port Sync Enable is set and both transcoders are bound to the same Pipe), only DSI 0 sends a Frame Start
3. If SW is going to use this attribute, it must use it one of two ways:
   a. The attribute must be set to the same value for both Frame Update Requests
   b. The attribute must be set to a 1 for the first Frame Update Request and a 0 for the second Frame Update Request
4. HW will not start looking for TE events (if TE gating is enabled) until both Frame Update Requests have been received.
5. Setting this bit should be mutually exclusive with the other Frame Update Request attributes Single Panel Update and Forward Frame Update Request

25 **Forward Frame Update Request**

Access:	R/W

This is an attribute applied to the Frame Update Request bit.

DSI_CMD_FRMCTL

This bit will control whether the transcoder forwards the Frame Update Request received by this transcoder to a synchronized transcoder

Value	Name
0b	Request not forwarded
1b	Request forwarded

Programming Notes

1. HW ignores this bit if the Port Sync Enable bit for the transcoders are not set
2. HW will automatically override the setting of this bit for DSI0 when in Dual Link Single Pipe (DLSP) mode. In DLSP, HW ignores any Frame Update Requests made to DSI1 and automatically forwards DSI0 Frame Update Requests to DSI1.
3. Setting this bit should be mutually exclusive with the other Frame Update Request attributes Accumulate Frame Update Request and Single Panel Update

24:2 **Reserved**

Access:	RO
Format:	MBZ

1 **Reserved**

Access:	RO
Format:	MBZ

0 **Frame in Progress**

Access:	RO

This bit reflects whether the DSI transcoder is currently processing/sending a frame to the Peripheral.

DSI_CMD_RXCTL

DSI_CMD_RXCTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B0D4h-6B0D7h
Name:	DSI Transcoder 0 Command Receive Control
ShortName:	DSI_CMD_RXCTL_0
Reset:	soft
Address:	6B8D4h-6B8D7h
Name:	DSI Transcoder 1 Command Receive Control
ShortName:	DSI_CMD_RXCTL_1
Reset:	soft

This register controls how received DSI packets from the Peripheral are handled.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**Read Unloads DW** Access: R/W This bit controls whether the DSI_RXDATA register read unloads the DW from the transcoders receive queue. If DSI_RXDATA reads do not unload the transcoders receive queue, then the transcoder will continue to return the DW of data at the head of the queue. Otherwise, every read to the DSI_RXDATA will return a new DW of data. Value 0b: DSI_RXDATA reads do not unload DW Value 1b: DSI_RXDATA reads unload DW
	15	**Received Unassigned Trigger** Access: R/WC The unassigned trigger (10100000 [lsb on the left to the msb on the right]) has been received. Value 0b: Trigger message not received Value 1b: Trigger message received
	14	**Received Acknowledge Trigger** Access: R/WC The Acknowledge trigger message (00100001 [lsb to msb]) has been received.

DSI_CMD_RXCTL

Value	Name
0b	Trigger message not received
1b	Trigger message received

13 **Received Tear Effect Trigger**

Access:	R/WC

The Tear Effect (TE) trigger message (01011101 [lsb to msb]) has been received.

Value	Name
0b	Trigger message not received
1b	Trigger message received

12 **Received Reset Trigger**

Access:	R/WC

The Reset trigger message (01100010 [lsb to msb]) has been received.
The Peripheral is not expected to send this trigger message to the Host, but even if it does, the hardware does not take any action on this message

Value	Name
0b	Trigger message not received
1b	Trigger message received

11 **Received Payload was Lost**

Access:	R/WC

This bit indicates if the DSI transcoder had to drop one or more of the payload bytes from a response packet being received from the Peripheral.
Software should check that the "Maximum Return Packet Size" programming is set correctly within the Peripheral

Value	Name
0b	No payload bytes dropped
1b	Payload bytes dropped

10 **Received CRC was Lost**

Access:	R/WC

When set, the DSI transcoder had to drop one or more of the CRC bytes from a response packet being received from the Peripheral.
If the "Received Payload was Lost" bit is set, then this bit will most likely also be set.
It is not imperative that the CRC is captured within the queue, so this is not an error but only a heads up that it may not be present.
If Software wishes the CRC to always be present within the Payload Receive queue, then it should adjust the "Maximum Return Packet Size" programming within the Peripheral to account for the CRC

Value	Name
0b	No CRC bytes dropped
1b	CRC bytes dropped

DSI_CMD_RXCTL		
	9:8	**Reserved** Access: RO Format: MBZ
	7:0	**Number Rx Payload DW** Access: RO This field represents the number of DWs currently within the transcoders Payload Receive queue. Note that the queue will be flushed at the beginning of a Bus Turn-Around (BTA) HW currently maintains an 8 DW queue.

DSI_CMD_RXHDR

DSI_CMD_RXHDR	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	6B0E0h-6B0E3h
Name:	DSI 0 Command Receive Header
ShortName:	DSI_CMD_RXHDR_0
Reset:	soft
Address:	6B8E0h-6B8E3h
Name:	DSI 1 Command Receive Header
ShortName:	DSI_CMD_RXHDR_1
Reset:	soft

This register reads the READ Response packet header received from the Periphery. This register is RO.

DWord	Bit	Description
0	31:0	**Received Header** Access: RO This field contains the READ Response packet header received from the Periphery. Software can read this as many times as it wishes (i.e. the Read Unloads DW bit of the DSI_CMD_RXCTL has no effect on this data).

DSI_CMD_RXPYLD

DSI_CMD_RXPYLD	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	6B0E4h-6B0E7h
Name:	DSI 0 Command Receive Payload
ShortName:	DSI_CMD_RXPYLD_0
Reset:	soft
Address:	6B8E4h-6B8E7h
Name:	DSI 1 Command Receive Payload
ShortName:	DSI_CMD_RXPYLD_1
Reset:	soft

This register reads from the Receive Payload queue within the transcoder which contains the payload data of READ Response packets received from the Periphery. A read to this register will pull a DW of data from a receive queue within the DSI transcoder unless the DSI_CMD_RXCTL is programmed to prevent this. This register is RO.

DWord	Bit	Description
0	31:0	**Received Payload** Access: RO This field contains the READ Response payload data and CRC received from the Periphery. This data is taken from the head of the DSI transcoders receive queue. If the Read Unloads DW bit of the DSI_CMD_RXCTL is set, then multiple reads to this register will return the same data (i.e. the data at the head of the receive queue). If there is a read to this register when the transcoders receive queue is empty (i.e. the Number Rx DW within DSI_CMD_RXDATA is zero), then the data returned will be all zeros. Note that the contents of the Receive Payload queue within the transcoder is flushed for every entry into a Bus Turn-Around state and for every exit from a content protection session.

DSI_CMD_TXCTL

DSI_CMD_TXCTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B0D0h-6B0D3h
Name:	DSI Transcoder 0 Command Transmit Control
ShortName:	DSI_CMD_TXCTL_0
Reset:	soft
Address:	6B8D0h-6B8D3h
Name:	DSI Transcoder 1 Command Transmit Control
ShortName:	DSI_CMD_TXCTL_1
Reset:	soft

This register controls how DSI command packets are built and transmitted over the DSI Link.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24	**Keep Link in HS** Access: R/W This field will keep the Link in the HS state between SW initiated command packets to the Periphery. The transitions between the LP and HS states can result in significant latencies and can have a negative impact on SW performance. If between HS commands there is no other HS traffic to transmit, then the DSI transcoder will begin transmitting Null packets until the next HS packet arrives. **Restriction** Restrictions: 1. HW will only act on this bit when the DSI transcoder is in the Command Mode of operation. 2. SW must clear this bit if it is going to initiate a LP transaction (e.g. a LPDT, BTA, Trigger, etc.). 3. SW should clear this bit when it is finished sending its burst of commands to the Periphery.
	23:13	**Reserved** Access: RO Format: MBZ

DSI_CMD_TXCTL		
	12:8	**Free Header Credits** Access: RO This field represents the number of Header resources that are currently available to SW. SW will need a Header Credit to write to either the Command Tx Header (DSI_CMD_TXHDR) or the LP Message (DSI_LP_MSG) registers. A write to either of these registers will consume a Header Credit. The transcoder will release a Header Credit after it has pulled the command from its internal command header queue. HW currently maintains 16 Header Credits.
	7:0	**Free Payload Credits** Access: RO This field represents the number of Payload resources that are currently available to SW. SW will need a Payload Credit to write to the Command Tx Payload register (DSI_CMD_TXPYLD). A write to the Tx Payload register will consume 1 Payload Credit (i.e., 1 Payload Credit is equal to 1 to 4 bytes of payload). The transcoder will release a Payload Credit after it has pulled a DW of data from its internal command payload queue. HW currently maintains 64 Payload Credits (i.e. HW can accept payloads of up to 256 bytes).

DSI_CMD_TXHDR

DSI_CMD_TXHDR	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B100h-6B103h
Name:	DSI Transcoder 0 Transmit Packet Header
ShortName:	DSI_CMD_TXHDR_0
Reset:	soft
Address:	6B900h-6B903h
Name:	DSI Transcoder 1 Transmit Packet Header
ShortName:	DSI_CMD_TXHDR_1
Reset:	soft

This register is used to write a packet header to the DSI transcoder.

DWord	Bit	Description
0	31	**Payload** Access: R/W When set, the DSI packet carries a payload of data. 0b: Short packet format (no payload) 1b: Long packet format (payload) **Restriction** Restrictions: 1. SW must ensure that the Data Type encoding matches the packet format specified by this attribute. 2. SW must ensure that the payload data is written into the Command Payload queue before writing to this register, if this bit is set.
	30	**LPDT** Access: R/W Low Power Data Transfer. This field will direct the DSI transcoder on what mode (HS or LP) to transmit the packet in. 0b: Cmd transmitted in HS state 1b: Cmd transmitted in LP Escape mode **Restriction** SW must expect synchronization events to be missed, if it sets this attribute when the DSI

DSI_CMD_TXHDR

controller is in the Video Mode of operation and the Timing Generator is enabled.
SW is highly discouraged from setting this bit when in Video Mode.

29 Vertical Blank Fence

Access:	R/W

This field will direct the DSI transcoder to wait until the start of the next V. Blank (in Video Mode) or the end of the frame (in Command Mode) before it executes the Command.
This can be used for Frame Synchronized Commands that have to be fenced after the transmission of an Execute Queue.

Value	Name
0b	Cmd will not be fenced
1b	Cmd will be fenced

28 Reserved

Access:	RO
Format:	MBZ

27:24 Reserved

Access:	RO
Format:	MBZ

23:8 Word Count - Parameters

Access:	R/W

This field specifies either the DSI Word Count (i.e. the length of the payload in bytes), or the two bytes of Parameters.
The interpretation of this field by the DSI transcoder will be based off of the Payload attribute above.
When the Payload bit is '0', then these bytes represent Parameters
When the Payload bit is '1', then these bytes represent the Word Count of the Payload
The interpretation of this field by the Periphery will be based off of the Data Type field below

Restriction
When the command carries a payload, SW must ensure that the value within this field matches the amount of payload data loaded into the Command Payload queue associated with this packet For Short packets, it will be the responsibility of SW to adhere to the DSI protocols if the packet carries only one, or no parameter

7:6 Virtual Channel

Access:	R/W

This field specifies the virtual channel to transmit the command over the DSI Link.

5:0 Data Type

Access:	R/W

This field specifies the DSI command Data Type.

DSI_CMD_TXPYLD

DSI_CMD_TXPYLD	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B104h-6B107h
Name:	DSI Transcoder 0 Transmit Packet Payload
ShortName:	DSI_CMD_TXPYLD_0
Reset:	soft
Address:	6B904h-6B907h
Name:	DSI Transcoder 1 Transmit Packet Payload
ShortName:	DSI_CMD_TXPYLD_1
Reset:	soft

This register is used to write a DW of packet payload to the DSI transcoder.

DWord	Bit	Description
0	31:0	**Payload Data** Access: R/W This register is a proxy into the payload of the command packet to be injected onto the DSI Link. Writes to this register will load the DW of data into a Command Payload queue that will be unloaded by HW after the packet has been validated via a write to the DSI_CMD_TXHDR register. When reading from this register, only the payload data from the last write will be available. **Restriction** Software must have an available Payload credit to write to this register. SW must write the payload in ascending order (i.e. DW 0 is written first, the final DW is written last). SW must load the entire payload within the Command Payload queue before writing to the Command Header register (DSI_CMD_TXHDR). The write to the Command Header register validates the payload written to this queue. SW must ensure that the WC of the Packet Header matches the amount of data written to the Command Payload queue.

DSI_DATA_TIMING_PARAM

DSI_DATA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B084h-6B087h
Name:	DSI 0 Data Lane Timing Parameter
ShortName:	DSI_DATA_TIMING_PARAM_0
Reset:	soft
Address:	6B884h-6B887h
Name:	DSI 1 Data Lane Timing Parameter
ShortName:	DSI_DATA_TIMING_PARAM_1
Reset:	soft

This register specifies the D-PHY timing parameters for the Data Lane, if SW is overriding the HW defaults.
This register is located within the Core Display and is used by the DSI Controller to calculate Link transition latencies of the Data Lanes. There is an identical register (DPHY_DATA_TIMING_PARAM) located within the combo-PHY that actually applies the overrides to the D-PHY Data Lanes. Both registers should be programmed by Software if an override needs to be applied to the Data Lanes within the D-PHY.
Since this register is being used to calculate the Link transition latencies of the Data Lanes, but does not actually affect the transition times within the D-PHY, this register can be used to add guardbands to the DSI Controller's transition latency calculations.
The lower 12 bits of the offset address for this register should correspond to the lower offset address of its sister D-PHY register within the combo-PHY.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
The programming of this register must be equal to or greater than the programming of it's sister register that lives within the combo-PHY (DPHY_DATA_TIMING_PARAM).

DWord	Bit	Description
0	31	**HS_PREPARE Override** Access: R/W This field controls the override of the HS-PREPARE timing parameter. Value 0: HW maintains Value 1: SW overrides
	30:27	**Reserved** Access: RO Format: MBZ

DSI_DATA_TIMING_PARAM

26:24 **HS_PREPARE**

Access:	R/W

This parameter defines the time that the Host drives a Data Lane with the LP-00 Lane state (the Bridge state) immediately before driving the HS-0 Line state.
This field represents a hexadecimal value with a precision of 1.2 i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this parameter at 1 Escape clock (minimum 50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.0 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 85ns + 6UI for this parameter.

23 **HS_ZERO Override**

Access:	R/W

This field controls the override of the HS-ZERO timing parameter

Value	Name
0	HW maintains
1	SW overrides

22:20 **Reserved**

Access:	RO
Format:	MBZ

19:16 **HS_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on a Data Lane.
HW maintains this parameter at 2 Escape clocks plus 1 Byte clock (minimum 100ns + 8UI)

15 **HS_TRAIL Override**

Access:	R/W

This field controls the override of the HS-TRAIL timing parameter

Value	Name
0	HW maintains
1	SW overrides

DSI_DATA_TIMING_PARAM

	14:11	**Reserved** Access: RO Format: MBZ
	10:8	**HS_TRAIL** Access: R/W This parameter defines the time that the Host drives the flipped differential state of the last payload data bit of a HS transmission on a Data Lane. HW maintains this parameter at 1.5 Escape clocks (minimum 75ns)
	7	**HS_EXIT Override** Access: R/W This field controls the override of the HS-EXIT timing parameter Value 0: HW maintains Value 1: SW overrides
	6:3	**Reserved** Access: RO Format: MBZ
	2:0	**HS_EXIT** Access: R/W This parameter defines the time that the Host drives the LP-11 Lane state (i.e. the Stop state) following a HS burst. HW maintains this parameter at 2 Escape clocks (minimum 100ns)

DSI_ESC_CLK_DIV

DSI_ESC_CLK_DIV

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	6B090h-6B093h
Name:	DSI 0 Escape Clock Divider
ShortName:	DSI_ESC_CLK_DIV_0
Reset:	soft
Address:	6B890h-6B893h
Name:	DSI 1 Escape Clock Divider
ShortName:	DSI_ESC_CLK_DIV_1
Reset:	soft

This register defines the clock divider variable M needed to generate an Escape clock from the 8X clock
This register is located within the Core Display. There is an identical register (DPHY_ESC_CLK_DIV) located within the combo-PHY. Both of these registers should be programmed by Software.
The lower 12 bits of the offset address for this register should correspond to the lower offset address of its sister D-PHY register within the combo-PHY.

Restriction : The programming of this register must be identical to the programming of its sister register that lives within the combo-PHY (DPHY_ESC_CLK_DIV)

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:16	**Byte Clocks per Escape Clock** Access: RO This field reports the number of Byte clocks present within a given Escape clock. The DSI transcoder calculates this variable based off of the Escape clock divider M. N = Ceiling(M/8) The DSI complex (transcoder and D-PHY) use this information to emulate an Escape clock using the Byte clock. Note that the value reported here is zero-based (i.e. Ceiling(M/8) - 1)
	15:9	**Reserved** Access: RO Format: MBZ
	8:0	**Escape Clock Divider M** Access: R/W **Description** This field specifies the divider variable (M) needed to derive the Escape clock from the Link

DSI_ESC_CLK_DIV		
		clock (i.e. the 8X frequency) Escape frequency= 8X frequency / M The DSI transcoder does not use a physical Escape clock, so there is no physical divider, but the transcoder needs to know the value of M to emulate the Escape clock in Byte clocks. **Restriction** The Escape clock frequency must be as close to, but not greater than 20MHz. Therefore, the programming of M should be: M = Ceiling(8X Frequency (in MHz) / 20 MHz)

DSI_HTX_TO

DSI_HTX_TO	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B044h-6B047h
Name:	DSI 0 HS Transmit Timeout
ShortName:	DSI_HTX_TO_0
Reset:	soft
Address:	6B844h-6B847h
Name:	DSI 1 HS Transmit Timeout
ShortName:	DSI_HTX_TO_1
Reset:	soft

This register specifies the HS Tx timeout.

DWord	Bit	Description
0	31:16	**HS TX Timeout** Default Value: FFFFh Access: R/W This field represents the upper 16 bits of the HS Transmit Timeout (i.e. the timeout has a granularity of 64K). The time is specified in Byte clocks. This field will default to the maximum possible value. **Programming Notes** This timer is zero-based (i.e. a value of 0 will have a timeout of 64K) If the DSI transcoder is in the Video Mode and is not able to place the Link in the LP state during the H. Blank regions of the V. Active region, then SW must program this to be greater that the amount of time it takes to transmit the full frame (V. Total * H. Total). The value should be set to a value greater than the Peripherals HS RX Timeout.
	15:1	**Reserved** Access: RO Format: MBZ
	0	**HTX_TO** Access: R/WC The HS TX Timer has timed out. HW will set this bit, SW will clear it with a write of 1b.

DSI_INTER_IDENT_REG

DSI_INTER_IDENT_REG	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	6B074h-6B077h
Name:	DSI Transcoder 0 Interrupt Identity Register
ShortName:	DSI_INTER_IDENT_REG_0
Reset:	soft
Address:	6B874h-6B877h
Name:	DSI Transcoder 1 Interrupt Identity Register
ShortName:	DSI_INTER_IDENT_REG_1
Reset:	soft

The DSI Interrupt Identity Register (IIR)logs non-masked DSI interrupts received from the Periphery and Host. The DSI_INTER_MSK_REG (IMR) controls which interrupts will be logged within the IIR.

DWord	Bit	Description
0	31	**TE Event** Access: R/WC A Tear Effect (TE) event was received
	30	**Rx Data / BTA Terminated** Access: R/WC READ response data has been received, or the BTA has been terminated
	29	**Tx Data** Access: R/WC A transmit credit has been freed
	28	**ULPS Entry Done** Access: R/WC A Ultra Low Power State Entry flow has completed
	27	**Non-TE Trigger Received** Access: R/WC A non-TE trigger has been received from the Periphery. The DSI_CMD_RXCTL will indicate the trigger received.
	26	**Host Checksum Error** Access: R/WC Host reported a checksum error
	25	**Host Multi ECC Error** Access: R/WC Host reported a multi-bit ECC error

DSI_INTER_IDENT_REG

	24	**Host Single ECC Error** Access: R/WC Host reported a single-bit ECC
	23	**Host Contention Detected** Access: R/WC Host reported a LP contention
	22	**Host False Control Error** Access: R/WC Host reported a False Control error
	21	**Host Timeout Error** Access: R/WC Host reported a Timeout error
	20	**Host Low Power Transmit Sync Error** Access: R/WC Host reported a LP Transmission byte alignment problem
	19	**Host Escape Mode Entry Command Error** Access: R/WC Host reported an Escape Mode entry command error
	18:17	**Spare 18_17** Access: R/WC Spare R/WC bits for future use
	16	**Frame Update Done** Access: R/WC A frame update is done. This interrupt is only valid when the transcoder is in Command Mode
	15	**Protocol Violation** Access: R/WC Peripheral reported a protocol violation
	14	**Spare 14** Access: R/WC Spare R/WC bit for future use
	13	**Invalid Tx Length** Access: R/WC Peripheral reported an invalid transmission length
	12	**Invalid VC** Access: R/WC Peripheral reported an invalid DSI VC ID
	11	**Invalid Data Type** Access: R/WC

DSI_INTER_IDENT_REG		
		Peripheral reported a non-recognizable DSI Data Type
	10	**Peripheral Checksum Error** Access: R/WC Peripheral reported a checksum error
	9	**Peripheral Multi ECC Error** Access: R/WC Peripheral reported a multi-bit ECC error
	8	**Peripheral Single ECC Error** Access: R/WC Peripheral reported a single-bit ECC error
	7	**Peripheral Contention Detected** Access: R/WC Peripheral reported a LP contention
	6	**Peripheral False Control Error** Access: R/WC Peripheral reported a False Control error
	5	**Peripheral Timeout Error** Access: R/WC Peripheral reported a timeout error
	4	**Peripheral Low Power Transmit Sync Error** Access: R/WC Peripheral reported a LP Transmission byte alignment problem
	3	**Peripheral Escape Mode Entry Command Error** Access: R/WC Peripheral reported an Escape Mode entry command error
	2	**EoT Sync Error** Access: R/WC Peripheral reported an End of Transmission byte alignment problem
	1	**SoT Sync Error** Access: R/WC Peripheral reported a Start of Transmission leader sequence corruption error
	0	**SoT Error** Access: R/WC Peripheral reported a Start of Transmission Error

DSI_INTER_MSK_REG

DSI_INTER_MSK_REG

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B070h-6B073h
Name:	DSI Transcoder 0 Interrupt Mask Register
ShortName:	DSI_INTER_MSK_REG_0
Reset:	soft
Address:	6B870h-6B873h
Name:	DSI Transcoder 1 Interrupt Mask Register
ShortName:	DSI_INTER_MSK_REG_1
Reset:	soft

The DSI Interrupt Mask Register (IMR) provides a filter to the events that can cause interrupts (i.e. the register will determine which events will be logged within the DSI Interrupt Identity Register (IIR))

DWord	Bit	Description
0	31	**TE Event** Access: R/W Tear Effect (TE) interrupt mask Value 0: Event Unmasked Value 1: Event Masked **[Default]**
	30	**Rx Data/BTA Terminated** Access: R/W READ response data received, or the BTA has been terminated interrupt mask Value 0: Event Unmasked Value 1: Event Masked **[Default]**
	29	**Tx Data** Access: R/W Freed transmit credit interrupt mask Value 0: Event Unmasked Value 1: Event Masked **[Default]**
	28	**ULPS Entry Done** Access: R/W Ultra Low Power State Entry flow interrupt mask

DSI_INTER_MSK_REG

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

27 **Non-TE Trigger Received**

Access:	R/W

Non-TE trigger received interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

26 **Host Checksum Error**

Access:	R/W

Host reported a checksum error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

Programming Notes
Masking this event effectively disables the CRC checking for received payloads

25 **Host Multi ECC Error**

Access:	R/W

Host reported a multi-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

Programming Notes
Masking this event along with the Host Single ECC Error mask bit will disable ECC checking for received packet headers

24 **Host Single ECC Error**

Access:	R/W

Host reported a single-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

Programming Notes
Masking this event along with the Host Multi ECC Error mask bit will disable ECC checking for received packet headers

DSI_INTER_MSK_REG

23	**Host Contention Detected** Access: R/W Host reported a LP contention interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
22	**Host False Control Error** Access: R/W Host reported a False Control error interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
21	**Host Timeout Error** Access: R/W Host reported a Timeout error interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
20	**Host Low Power Transmit Sync Error** Access: R/W Host reported a LP Transmission byte alignment problem interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
19	**Host Escape Mode Entry Command Error** Access: R/W Host reported an Escape Mode entry command error interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
18:17	**Spare 18_17** Default Value: 11b Access: R/W Spare R/W bits for future use
16	**Frame Update Done** Frame update finished mask

DSI_INTER_MSK_REG

Value	Name
0b	Event Unmasked
1b	Event Masked **[Default]**

15 — Protocol Violation

Access:	R/W

Peripheral reported a protocol violation interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

14 — Spare 14

Default Value:	1b
Access:	R/W

Spare R/W bit for future use

13 — Invalid Tx Length

Access:	R/W

Peripheral reported an invalid transmission length interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

12 — Invalid VC

Access:	R/W

Peripheral reported an invalid DSI VC ID interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

11 — Invalid Data Type

Access:	R/W

Peripheral reported a non-recognizable DSI Data Type interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

10 — Peripheral Checksum Error

Access:	R/W

Peripheral reported a checksum error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

DSI_INTER_MSK_REG

9 — Peripheral Multi ECC Error

Access:	R/W

Peripheral reported a multi-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

8 — Peripheral Single ECC Error

Access:	R/W

Peripheral reported a single-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

7 — Peripheral Contention Detected

Access:	R/W

Peripheral reported a LP contention interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

6 — Peripheral False Control Error

Access:	R/W

Peripheral reported a False Control error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

5 — Peripheral Timeout Error

Access:	R/W

Peripheral reported a timeout error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

4 — Peripheral Low Power Transmit Sync Error

Access:	R/W

Peripheral reported a LP Transmission byte alignment problem interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

DSI_INTER_MSK_REG

	3	**Peripheral Escape Mode Entry Command Error** Access: R/W Peripheral reported an Escape Mode entry command error interrupt mask **Value** / **Name** 0 – Event Unmasked 1 – Event Masked **[Default]**
	2	**EoT Sync Error** Access: R/W Peripheral reported an End of Transmission byte alignment problem interrupt mask **Value** / **Name** 0 – Event Unmasked 1 – Event Masked **[Default]**
	1	**SoT Sync Error** Access: R/W Peripheral reported a Start of Transmission leader sequence corruption error interrupt mask **Value** / **Name** 0 – Event Unmasked 1 – Event Masked **[Default]**
	0	**SoT Error** Access: R/W Peripheral reported a Start of Transmission Error interrupt mask **Value** / **Name** 0 – Event Unmasked 1 – Event Masked **[Default]**

DSI_IO_MODECTL

DSI_IO_MODECTL

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	6B094h-6B097h
Name:	DSI Transcoder 0 IO Mode Control
ShortName:	DSI_IO_MODECTL_0
Reset:	soft
Address:	6B894h-6B897h
Name:	DSI Transcoder 1 IO Mode Control
ShortName:	DSI_IO_MODECTL_1
Reset:	soft

This register is used to control the mode of operation within the Combo-PHY which is shared between the MIPI DSI transcoder and the eDP/DP DDI.
Each DSI transcoder is attached to the following Combo-PHY:
DSI0: Combo-PHY A
DSI1: Combo-PHY B
Note that the Combo-PHY's are also referred to as DDI A / DDI B

Restriction: If the Combo-PHY is going to be used by the DSI transcoder, then this register must be programmed **before** the power request is sent to the Combo-PHY

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:16	**Reserved** Access: RO Format: MBZ
	15:2	**Reserved** Access: RO Format: MBZ
	1	**Reserved** Access: RO Format: MBZ
	0	**Combo PHY Mode** Access: R/W For products using a Combo-PHY for the DSI port, this bit selects the mode of operation within the Combo-PHY to which the DSI transcoder is attached. For products using a dedicated DSI PHY, this bit controls the clock request to the PHY.

DSI_IO_MODECTL			
		Value	Name
		0b	DDI Mode / No Clock Request
		1b	MIPI DSI Mode / Clock Request

DSI_LP_MSG

DSI_LP_MSG

Register Space:	MMIO: 0/2/0
Access:	R/W Set
Size (in bits):	32
Address:	6B0D8h-6B0DBh
Name:	DSI 0 Low Power Message
ShortName:	DSI_LP_MSG_0
Reset:	soft
Address:	6B8D8h-6B8DBh
Name:	DSI 1 Low Power Message
ShortName:	DSI_LP_MSG_1
Reset:	soft

This register contains the LP messages that can be sent to the Periphery.

Restriction

Software must have a Header credit to write to this register.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18	**Link Direction** Access: RO This field advertises the current state of the Link direction 0b – Link is in the Forward direction 1b – Link is in the Reverse direction
	17	**LP Tx in Progress** Access: RO This status bit indicates whether the DSI transcoder is currently servicing a LP transaction. 0b – Transcoder is not transmitting in the LP Esc mode 1b – Transcoder is transmitting in the LP Esc mode
	16	**In ULPS** Access: RO This status bit indicates whether the DSI Link is in the Ultra-Low Power State (ULPS), or not. This bit should accurately reflect the ultra-low power state of the Link even when the DSI transcoder function is disabled.

DSI_LP_MSG

Value	Name
0b	The DSI Link is not in ULPS
1b	The DSI Link is in ULPS

15:11 **Reserved**

Access:	RO
Format:	MBZ

10:9 **Trigger Type**

Access:	R/W

This field specifies the type of Trigger Message to send the Peripheral. It is only sampled when a Trigger Message is being sent to the Peripheral.

Value	Name	Description
00b	Reset Trigger	Entry Command [lsb:msb]: 01100010
01b	Unknown 3	Entry Command [lsb:msb]: 01011101
10b	Unknown 4	Entry Command [lsb:msb]: 00100001
11b	Unknown 5	Entry Command [lsb:msb]: 10100000

Programming Notes
Note that the Unassigned triggers are not specifically assigned to a given action/function within the DSI spec. Therefore, these can be used as general-purpose trigger messages that the Periphery defines

8 **ULPS Type**

Access:	R/W

This bit specifies the LP state that the Lanes (both Data and Clock) will be left in after entering ULPS

Value	Name	Description
0b	LP-00	Lanes will be left in the LP-00 state
1b	LP-11	Lanes will be left in the LP-11 state

7:3 **Reserved**

Access:	RO
Format:	MBZ

2 **Trigger Message**

Access:	R/W Set

This bit will direct the DSI Transcoder to issue a Trigger Message to the Peripheral. The type of trigger is specified with the Trigger Type field within this register.
Trigger signaling is a mechanism to send a flag to the Protocol Layer of the Periphery using the Escape Mode of transmission.

Programming Notes
The trigger flag, as seen by the Peripheral, can be extended using the Trigger Extension in the DPHY_TRIG_EXT.

DSI_LP_MSG

		The DSI Transcoder will clear this bit when it is finished with the transmission of the message (including the Trigger Extension)
	1	**Bus Turnaround** Access: R/W Set This bit will direct the DSI Transcoder to issue a BTA request to the Periphery. **Programming Notes** When in Video Mode, the DSI transcoder will dispatch a BTA request (by itself) within the next Vertical blank line that it sees. SW must program the Turnaround Timeout (DSI_TA_TO) and the LP Rx (Host) Timeout (DSI_LRX_H_TO) properly to avoid having synchronization events being missed. In other words, the total amount of time it takes to send a BTA and receive a response from the Panel needs to be less than the Vertical blank line time.
	0	**ULPS Entry** Access: R/W Set Ultra-Low Power State Entry. When set, the DSI Transcoder will transmit the ULPS Entry Command on all Data Lanes and it will bring the Clock Lane to the ULPS state. The state of the Lanes at the end of the ULPS flow is dictated by the ULPS Type within this register. When HW has finished the UPLS sequence it will clear this bit. **Restriction** Before setting this bit, Software must disable the DSI's Timing Generator

DSI_LRX_H_TO

DSI_LRX_H_TO

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B048h-6B04Bh
Name:	DSI 0 LP Rx (Host) Timeout
ShortName:	DSI_LRX_H_TO_0
Reset:	soft
Address:	6B848h-6B84Bh
Name:	DSI 1 LP Rx (Host) Timeout
ShortName:	DSI_LRX_H_TO_1
Reset:	soft

This register specifies the LP Rx (Host)timeout.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**LRX_H_TO** Default Value: 0b Access: R/WC The LP RX Timer has timed out. HW will set this bit, SW must clear it with a write of 1b.
	15:0	**LP RX_H Timeout** Access: R/W This field represents the maximum amount of time the DSI transcoder will give to the Peripheral to transmit its response back to the Host. If the timer times out, then the DSI transcoder will set the LRX_H_TO bit in this register and the Host Timeout Error bit within the DSI_INTER_IDENT_REG register, if this interrupt event is unmasked(DSI_INTER_MSK_REG). The time is specified in Escape clocks. **Programming Notes** The LP RX Timer will be disabled if this value is zero

DSI_PWAIT_TO

DSI_PWAIT_TO	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B040h-6B043h
Name:	DSI 0 Peripheral Wait Timeout
ShortName:	DSI_PWAIT_TO_0
Reset:	soft
Address:	6B840h-6B843h
Name:	DSI 1 Peripheral Wait Timeout
ShortName:	DSI_PWAIT_TO_1
Reset:	soft

This register represents a Peripheral wait time used in conjunction with either a BTA or a Trigger LP message.
The times specified within this register are in terms of Escape clocks.
The timers are zero-based (i.e. a value of 0 equals 1 Escape clock)

DWord	Bit	Description
0	31:16	**Peripheral Reset Timeout** Access: R/W This field represents the time to wait after a Reset Trigger has been transmitted to the Peripheral (PR_TO). The timer will start after the Trigger message has been sent and the DSI transcoder will block all other traffic until the timer reaches the timeout value.
	15:0	**Peripheral Response Timeout** Access: R/W This field represents the time to wait before asking the Peripheral for a response (PRESP_TO). The timer will start when the DSI transcoder receives the BTA request from SW and the Link enters the Stop state. When the timer reaches the timeout value, the DSI transcoder will begin the BTA request to the Peripheral.

DSI_T_INIT_PRIMARY

DSI_T_INIT_PRIMARY	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B088h-6B08Bh
Name:	DSI 0 Initialization Primary Time
ShortName:	DSI_T_INIT_PRIMARY_0
Reset:	soft
Address:	6B888h-6B88Bh
Name:	DSI 1 Initialization Primary Time
ShortName:	DSI_T_INIT_PRIMARY_1
Reset:	soft

This register specifies the amount of time (in Escape clocks) to drive the Link in the initialization state.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Primary Initialization Time** Default Value: 07D0h Access: R/W This field specifies the INIT_PRIMARY timing parameter used by the Host to drive the Link initialization. This field is specified in Escape clocks where the Escape clock operates at a maximum frequency of 20MHz. **Programming Notes** The default value of this register will produce an initialization duration of 100us which is the minimum requirement for the INIT timing parameter. The Periphery may require a longer initialization period (INIT + INTERNAL_DELAY), so the value programmed should be greater than the Periphery's initialization requirements.

DSI_T_WAKEUP

DSI_T_WAKEUP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B08Ch-6B08Fh
Name:	DSI 0 Wakeup Timing Parameter
ShortName:	DSI_T_WAKEUP_0
Reset:	soft
Address:	6B88Ch-6B88Fh
Name:	DSI 1 Wakeup Timing Parameter
ShortName:	DSI_T_WAKEUP_1
Reset:	soft

This is the timing parameter T-WAKEUP used to drive the Mark-1 state on the Link when exiting ULPS.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Wakeup Time** Default Value: 4E20h Access: R/W This field represents the T_{WAKEUP} timing parameter used when ULPS is being exited. The time is specified in number of Escape clocks. The default of this field will be set to 1ms (MIPI DSI specification minimum). **Restriction** A value of zero is invalid

DSI_TA_TO

DSI_TA_TO	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B04Ch-6B04Fh
Name:	DSI 0 Turnaround Timeout
ShortName:	DSI_TA_TO_0
Reset:	soft
Address:	6B84Ch-6B84Fh
Name:	DSI 1 Turnaround Timeout
ShortName:	DSI_TA_TO_1
Reset:	soft

This register specifies the Turnaround timeout.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**TA_TO** Access: R/WC The Turnaround Timer has timed out. HW will set this bit, SW must clear it with a write of 1b.
	15:0	**Turnaround Timeout** Access: R/W This field represents the maximum amount of time the Host will give to the Peripheral to acknowledge the Bus Turnaround request. If the timer times out, then the DSI transcoder will set the TA_TO bit in this register and the Host Timeout Error bit within the DSI_INTER_IDENT_REG register, if this interrupt event is unmasked (DSI_INTER_MSK_REG). The time is specified in Escape clocks. **Programming Notes** The TA TO Timer will be disabled if this value is zero

DSI_TRIG_TX_TIME

DSI_TRIG_TX_TIME

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B09Ch-6B09Fh
Name:	DSI 0 Trigger Transmission Time
ShortName:	DSI_TRIG_TX_TIME_0
Reset:	soft
Address:	6B89Ch-6B89Fh
Name:	DSI 1 Trigger Transmission Time
ShortName:	DSI_TRIG_TX_TIME_1
Reset:	soft

This register specifies the amount of time to present a LP Trigger request to the physical layer in Escape clocks When programming this register, SW must consider the following:

1. Escape mode entry and command transmission time: 20 Escape clocks
2. Trigger extension time: Panel specific

Software should not program the value within this register to be less than the time it takes to transmit the Escape mode entry and command. Doing so could pre-empt the transmission of the trigger causing an error at the Panel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Trigger Tx Time** Default Value: 14h This field specifies the number of Escape clocks that the DSI controller should present a trigger message to the physical layer This field is only used if a Trigger Message is initiated from the DSI_LP_MSG register.

DS Invocation Counter

DS_INVOCATION_COUNT - DS Invocation Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02308h
Name:	DS Invocation Counter
ShortName:	DS_INVOCATION_COUNT

This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two. This register is part of the context save and restore.

DWord	Bit	Description
0..1	63:32	**DS Invocation Count UDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS
	31:0	**DS Invocation Count LDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

DSMBASE

DSMBASE - DSMBASE

Register Space:	MMIO: 0/2/0
Size (in bits):	64
SOC_Consumer:	BIOS
Address:	1080C0h

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory. BIOS is now able to allocate Gfx Stolen Memory above the 4GB.

DWord	Bit	Description
0..1	63:20	**BDSM** Default Value: 000h Access: R/W _Custom_GTIReset: BUS This BitField contains bits 63 to 20 of the base address of stolen DRAM memory.
	19:1	**Reserved** Access: RO Format: MBZ
	0	**SPARE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This was a lock bit prior.

DSSM

DSSM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	51004h-51007h
Name:	Display Strap State
ShortName:	DSSM
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31:29	**Reference Frequency** Access: RO This field indicates the reference clock frequency. Software should use this value when programming the display clocks. 000b: 24 MHz 001b: 19.2 MHz 010b: 38.4 MHz
	28	**Spare 28**
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Spare 17**
	16	**Spare 16**
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**Spare 11**

DSSM

	10	**Spare 10**
	9	**Spare 9**
	8	**Spare 8**
	7	**Spare 7**
	6	**DE 8k Dis** DE_8K_DIS 8k capability fuse. This bit indicates whether hardware supports screens with widths greater than 5120 pixels. For tiled or joined displays, this is the total width after combining the widths of both pipes. Software must not enable these resolutions when the fuse is configured to disable 8k.

Value	Name	Description
0b	Enable	8k Capability Enabled
1b	Disable	8k Capability Disabled

	5	**Audio IO Flop Bypass** This field specifies whether the audio IO flop should be bypassed for dies with a long path to IO.

Value	Name
0b	Don't Bypass
1b	Bypass

	4	**Audio IO Select** This field specifies which audio IO location to use. It has to match where the PCH audio is connecting to the die.

Value	Name
0b	South
1b	North

	3	**WD Video Fault Continue** This field specifies whether WD video should continue data writes after a fault or stop the writes.

Value	Name
0b	Stop Writes
1b	Continue Writes

	2	**Reserved**
	1	**Part Is SOC**

Description
This field specifies whether this part is a SoC or not.

Value	Name
0b	Not SoC
1b	SoC

	0	**DisplayPort A Present** This bit specifies whether the port was present during initialization. This strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0.

DSSM				
		Value	Name	Description
		0b	Not Present	Port not present
		1b	Present	Port present

Dummy Context Save Register

UNUTILIZED_DUMMY_CTXSAVE - Dummy Context Save Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	080FCh	
DWord	**Bit**	**Description**
0	31:0	**Context Save Register** Access: R/W _Custom_GTIReset: DEV This register is purely used as a dummy register when do context save of non-unslice clients. This is the last register saved as part of all other context saves and used as indication that restore is complete

EDRAMCAP

EDRAMCAP - EDRAMCAP		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	120010h	
Describes the presence and capabilities of the eDRAM cache.		
DWord	**Bit**	**Description**
0	31:0	**EDRAMCAP_VALUE** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS **Bits[31:22] - Reserved** **Bits[21:16] - CURRENT_ETAG_WAYS,** Default Value: 11b The total number of ways in each ETAG slice. This field is updated by PCODE after every ETAG shrink or ETAG expand. 0 if 4 ways 1 if 8 ways 2 if 12 ways 3 if 16 ways. **Bits[15:10] - Reserved** **Bits[9:8] - SETS_CONFIGURATION,** Default Value: 10b 1K or 2K sets, to support 64MB and 128MB EDRAM size configurations accordingly. 00 = Reserved. 01 if 1K sets 10 if 2K sets 11 reserved. **Bits[7:5] - WAYS_CONFIGURATION,** Default Value: 011b This field defines the total number of ETAG ways. 000 if 4 ways 001 if 8 ways 010 if 12 ways 011 if 16 ways 1xx reserved. **Bits[4:1] - Super Queue Internal Register Count,** Default Value: 0100b Number of EDRAM TAG banks should be always 4, meaning 4 banks. **Bit[0] - FUSE_EDRAM_ENABLE,** Default Value: 0b PCODE will update this field based on FUSE_EDRAM_ENABLE.

EMRR Mask LSB

EMRRMASK_LSB - EMRR Mask LSB		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 09208h		
EMRR Mask Value		
DWord	**Bit**	**Description**
0	31:12	**EMRR MASK LSB BITS** Access: RO _Custom_GTIReset: BUS EMRR MASK VALUE.
	11	**EMRR ENABLE** Access: RO _Custom_GTIReset: BUS EMRR Enable.
	10	**EMRR LOCK** Access: RO _Custom_GTIReset: BUS EMRR LOCK bit.
	9:0	**Spares** Access: RO _Custom_GTIReset: BUS

EMRR Mask MSB

EMRRMASK_MSB - EMRR Mask MSB		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 0920Ch		
EMRR Mask Value		
DWord	**Bit**	**Description**
0	31:0	**EMRR MASK MSB BITS** Access: RO _Custom_GTIReset: BUS EMRR MASK VALUE.

Encoded row max QP vector

ENC_ROW_MAX_QP_VEC - Encoded row max QP vector	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	1024
_Custom_GTIReset:	BUS
Address:	1C2D00h-1C2D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG0
Address:	1C6D00h-1C6D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG1
Address:	1D2D00h-1D2D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG2
Address:	1D6D00h-1D6D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG3
Address:	1E2D00h-1E2D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG4
Address:	1E6D00h-1E6D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG5
Address:	1F2D00h-1F2D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG6
Address:	1F6D00h-1F6D7Fh
Name:	Max QP for each Tile row
ShortName:	ENC_ROW_MAX_QP_VEC_VDENC_REG7

This register holds the Max QP of the encoded bitstream for four consecutive LCU rows. Each, LCU row uses 8 bits.

DWord	Bit	Description
0	31:24	**MAX_QP_LCU_ROW_3** This Byte holds the maximum qp value of any CU coded in the row 3. The value could be used to determine the quality of encoded bitstream for row 3.

ENC_ROW_MAX_QP_VEC - Encoded row max QP vector		
	23:16	**MAX_QP_LCU_ROW_2** This Byte holds the maximum qp value of any CU coded in the row 2. The value could be used to determine the quality of encoded bitstream for row 2.
	15:8	**MAX_QP_LCU_ROW_1** This Byte holds the maximum qp value of any CU coded in the row 1. The value could be used to determine the quality of encoded bitstream for row 1.
	7:0	**MAX_QP_LCU_ROW_0** This Byte holds the maximum qp value of any CU coded in the row 0. The value could be used to determine the quality of encoded bitstream for row 0.
1	31:24	**MAX_QP_LCU_ROW_7**
	23:16	**MAX_QP_LCU_ROW_6**
	15:8	**MAX_QP_LCU_ROW_5**
	7:0	**MAX_QP_LCU_ROW_4**
2	31:24	**MAX_QP_LCU_ROW_11**
	23:16	**MAX_QP_LCU_ROW_10**
	15:8	**MAX_QP_LCU_ROW_9**
	7:0	**MAX_QP_LCU_ROW_8**
3	31:24	**MAX_QP_LCU_ROW_15**
	23:16	**MAX_QP_LCU_ROW_14**
	15:8	**MAX_QP_LCU_ROW_13**
	7:0	**MAX_QP_LCU_ROW_12**
4	31:24	**MAX_QP_LCU_ROW_19**
	23:16	**MAX_QP_LCU_ROW_18**
	15:8	**MAX_QP_LCU_ROW_17**
	7:0	**MAX_QP_LCU_ROW_16**
5	31:24	**MAX_QP_LCU_ROW_23**
	23:16	**MAX_QP_LCU_ROW_22**
	15:8	**MAX_QP_LCU_ROW_21**
	7:0	**MAX_QP_LCU_ROW_20**
6	31:24	**MAX_QP_LCU_ROW_27**
	23:16	**MAX_QP_LCU_ROW_26**
	15:8	**MAX_QP_LCU_ROW_25**
	7:0	**MAX_QP_LCU_ROW_24**
7	31:24	**MAX_QP_LCU_ROW_31**
	23:16	**MAX_QP_LCU_ROW_30**
	15:8	**MAX_QP_LCU_ROW_29**
	7:0	**MAX_QP_LCU_ROW_28**
8	31:24	**MAX_QP_LCU_ROW_35**

ENC_ROW_MAX_QP_VEC - Encoded row max QP vector		
	23:16	**MAX_QP_LCU_ROW_34**
	15:8	**MAX_QP_LCU_ROW_33**
	7:0	**MAX_QP_LCU_ROW_32**
9	31:24	**MAX_QP_LCU_ROW_39**
	23:16	**MAX_QP_LCU_ROW_38**
	15:8	**MAX_QP_LCU_ROW_37**
	7:0	**MAX_QP_LCU_ROW_36**
10	31:24	**MAX_QP_LCU_ROW_43**
	23:16	**MAX_QP_LCU_ROW_42**
	15:8	**MAX_QP_LCU_ROW_41**
	7:0	**MAX_QP_LCU_ROW_40**
11	31:24	**MAX_QP_LCU_ROW_47**
	23:16	**MAX_QP_LCU_ROW_46**
	15:8	**MAX_QP_LCU_ROW_45**
	7:0	**MAX_QP_LCU_ROW_44**
12	31:24	**MAX_QP_LCU_ROW_51**
	23:16	**MAX_QP_LCU_ROW_50**
	15:8	**MAX_QP_LCU_ROW_49**
	7:0	**MAX_QP_LCU_ROW_48**
13	31:24	**MAX_QP_LCU_ROW_55**
	23:16	**MAX_QP_LCU_ROW_54**
	15:8	**MAX_QP_LCU_ROW_53**
	7:0	**MAX_QP_LCU_ROW_52**
14	31:24	**MAX_QP_LCU_ROW_59**
	23:16	**MAX_QP_LCU_ROW_58**
	15:8	**MAX_QP_LCU_ROW_57**
	7:0	**MAX_QP_LCU_ROW_56**
15	31:24	**MAX_QP_LCU_ROW_63**
	23:16	**MAX_QP_LCU_ROW_62**
	15:8	**MAX_QP_LCU_ROW_61**
	7:0	**MAX_QP_LCU_ROW_60**
16	31:24	**MAX_QP_LCU_ROW_67**
	23:16	**MAX_QP_LCU_ROW_66**
	15:8	**MAX_QP_LCU_ROW_65**
	7:0	**MAX_QP_LCU_ROW_64**
17	31:24	**MAX_QP_LCU_ROW_71**

ENC_ROW_MAX_QP_VEC - Encoded row max QP vector		
	23:16	**MAX_QP_LCU_ROW_70**
	15:8	**MAX_QP_LCU_ROW_69**
	7:0	**MAX_QP_LCU_ROW_68**
18	31:24	**MAX_QP_LCU_ROW_75**
	23:16	**MAX_QP_LCU_ROW_74**
	15:8	**MAX_QP_LCU_ROW_73**
	7:0	**MAX_QP_LCU_ROW_72**
19	31:24	**MAX_QP_LCU_ROW_79**
	23:16	**MAX_QP_LCU_ROW_78**
	15:8	**MAX_QP_LCU_ROW_77**
	7:0	**MAX_QP_LCU_ROW_76**
20	31:24	**MAX_QP_LCU_ROW_83**
	23:16	**MAX_QP_LCU_ROW_82**
	15:8	**MAX_QP_LCU_ROW_81**
	7:0	**MAX_QP_LCU_ROW_80**
21	31:24	**MAX_QP_LCU_ROW_87**
	23:16	**MAX_QP_LCU_ROW_86**
	15:8	**MAX_QP_LCU_ROW_85**
	7:0	**MAX_QP_LCU_ROW_84**
22	31:24	**MAX_QP_LCU_ROW_91**
	23:16	**MAX_QP_LCU_ROW_90**
	15:8	**MAX_QP_LCU_ROW_89**
	7:0	**MAX_QP_LCU_ROW_88**
23	31:24	**MAX_QP_LCU_ROW_95**
	23:16	**MAX_QP_LCU_ROW_94**
	15:8	**MAX_QP_LCU_ROW_93**
	7:0	**MAX_QP_LCU_ROW_92**
24	31:24	**MAX_QP_LCU_ROW_99**
	23:16	**MAX_QP_LCU_ROW_98**
	15:8	**MAX_QP_LCU_ROW_97**
	7:0	**MAX_QP_LCU_ROW_96**
25	31:24	**MAX_QP_LCU_ROW_103**
	23:16	**MAX_QP_LCU_ROW_102**
	15:8	**MAX_QP_LCU_ROW_101**
	7:0	**MAX_QP_LCU_ROW_100**
26	31:24	**MAX_QP_LCU_ROW_107**

ENC_ROW_MAX_QP_VEC - Encoded row max QP vector		
	23:16	**MAX_QP_LCU_ROW_106**
	15:8	**MAX_QP_LCU_ROW_105**
	7:0	**MAX_QP_LCU_ROW_104**
27	31:24	**MAX_QP_LCU_ROW_111**
	23:16	**MAX_QP_LCU_ROW_110**
	15:8	**MAX_QP_LCU_ROW_109**
	7:0	**MAX_QP_LCU_ROW_108**
28	31:24	**MAX_QP_LCU_ROW_115**
	23:16	**MAX_QP_LCU_ROW_114**
	15:8	**MAX_QP_LCU_ROW_113**
	7:0	**MAX_QP_LCU_ROW_112**
29	31:24	**MAX_QP_LCU_ROW_119**
	23:16	**MAX_QP_LCU_ROW_118**
	15:8	**MAX_QP_LCU_ROW_117**
	7:0	**MAX_QP_LCU_ROW_116**
30	31:24	**MAX_QP_LCU_ROW_123**
	23:16	**MAX_QP_LCU_ROW_122**
	15:8	**MAX_QP_LCU_ROW_121**
	7:0	**MAX_QP_LCU_ROW_120**
31	31:24	**MAX_QP_LCU_ROW_127**
	23:16	**MAX_QP_LCU_ROW_126**
	15:8	**MAX_QP_LCU_ROW_125**
	7:0	**MAX_QP_LCU_ROW_124**

Error Identity Register

EIR - Error Identity Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020B0h-020B3h
Name:	Error Identity Register
ShortName:	EIR_RCSUNIT
Address:	180B0h-180B3h
Name:	Error Identity Register
ShortName:	EIR_POCSUNIT
Address:	220B0h-220B3h
Name:	Error Identity Register
ShortName:	EIR_BCSUNIT
Address:	1C00B0h-1C00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT0
Address:	1C40B0h-1C40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT1
Address:	1C80B0h-1C80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT0
Address:	1D00B0h-1D00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT2
Address:	1D40B0h-1D40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT3
Address:	1D80B0h-1D80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT1
Address:	1E00B0h-1E00B3h
Name:	Error Identity Register

EIR - Error Identity Register

ShortName:	EIR_VCSUNIT4
Address:	1E40B0h-1E40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT5
Address:	1E80B0h-1E80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT2
Address:	1F00B0h-1F00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT6
Address:	1F40B0h-1F40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT7
Address:	1F80B0h-1F80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT3
Address:	1A0B0h-1A0B3h
Name:	Error Identity Register
ShortName:	EIR_CCSUNIT0

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.)

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:0	**Error Identity Bits** This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the error bit of the IIR. Reserved bits are RO. Refer the table titled "Hardware-Detected Error Bits" for independent bit definitions. Value: 1h — Name: Error occurred

EIR - Error Identity Register

		Programming Notes
		Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).

Error Mask Register

EMR - Error Mask Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020B4h-020B7h
Name:	Error Mask Register
ShortName:	EMR_RCSUNIT
Address:	180B4h-180B7h
Name:	Error Mask Register
ShortName:	EMR_POCSUNIT
Address:	220B4h-220B7h
Name:	Error Mask Register
ShortName:	EMR_BCSUNIT
Address:	1C00B4h-1C00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT0
Address:	1C40B4h-1C40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT1
Address:	1C80B4h-1C80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT0
Address:	1D00B4h-1D00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT2
Address:	1D40B4h-1D40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT3
Address:	1D80B4h-1D80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT1
Address:	1E00B4h-1E00B7h
Name:	Error Mask Register

EMR - Error Mask Register

ShortName:	EMR_VCSUNIT4
Address:	1E40B4h-1E40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT5
Address:	1E80B4h-1E80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT2
Address:	1F00B4h-1F00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT6
Address:	1F40B4h-1F40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT7
Address:	1F80B4h-1F80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT3
Address:	1A0B4h-1A0B7h
Name:	Error Mask Register
ShortName:	EMR_CCSUNIT0

The EMR register is used by software to control which Error Status Register bits are masked or unmasked. Unmasked bits will be reported in the EIR, thus setting the error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. Masked bits will not be reported in the EIR and therefore cannot generate error conditions or CPU interrupts. Reserved bits are RO.

DWord	Bit	Description
0	31:8	**Reserved** Default Value: FFFFFFh Format: PBC **Programming Notes** These bits are not implemented in HW and must be set to '1'
	7:0	**Error Mask Bits** This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR. Refer the table titled "Hardware-Detected Error Bits" for independent bit definitions.

EMR - Error Mask Register

Value	Name	Description
FFh	**[Default]**	
0h	Not Masked	Will be reported in the EIR
1h	Masked	Will not be reported in the EIR

Error Status Register

ESR - Error Status Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020B8h-020BBh
Name:	Error Status Register
ShortName:	ESR_RCSUNIT
Address:	180B8h-180BBh
Name:	Error Status Register
ShortName:	ESR_POCSUNIT
Address:	220B8h-220BBh
Name:	Error Status Register
ShortName:	ESR_BCSUNIT
Address:	1C00B8h-1C00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT0
Address:	1C40B8h-1C40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT1
Address:	1C80B8h-1C80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT0
Address:	1D00B8h-1D00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT2
Address:	1D40B8h-1D40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT3
Address:	1D80B8h-1D80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT1
Address:	1E00B8h-1E00BBh
Name:	Error Status Register

ESR - Error Status Register

ShortName:	ESR_VCSUNIT4
Address:	1E40B8h-1E40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT5
Address:	1E80B8h-1E80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT2
Address:	1F00B8h-1F00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT6
Address:	1F40B8h-1F40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT7
Address:	1F80B8h-1F80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT3
Address:	1A0B8h-1A0BBh
Name:	Error Status Register
ShortName:	ESR_CCSUNIT0

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing an error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Error Status Bits** This register contains the non-persistent values of all hardware-detected error condition bits. Refer the table titled "Hardware-Detected Error Bits" for independent bit definitions. Value: 1h — Name: Error Condition Detected

EU_GRF_CLEAR

EU_GRF_CLEAR - EU_GRF_CLEAR		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0E550h	
Name:	EU_GRF_CLEAR	
ShortName:	EU_GRF_CLEAR	
This is a basic register template		
DWord	**Bit**	**Description**
0	31:0	**GRF_CLEAR** Default Value: 0000000000000000b Access: RO

EUP1 BONUS2 Reg

EUP1SPCBONUS2 - EUP1 BONUS2 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24698h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT:

EUP1SPCBONUS2 - EUP1 BONUS2 Reg

		'0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP1 BONUS11 Reg

EUP1SPCBONUS1 - EUP1 BONUS11 Reg		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24694h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT:

EUP1SPCBONUS1 - EUP1 BONUS11 Reg

		'0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP2 BONUS1 Reg

EUP2SPCBONUS1 - EUP2 BONUS1 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24714h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT:

EUP2SPCBONUS1 - EUP2 BONUS1 Reg

		'0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP2 BONUS2 Reg

EUP2SPCBONUS2 - EUP2 BONUS2 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24718h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT:

EUP2SPCBONUS2 - EUP2 BONUS2 Reg

		'0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP 2 Power Down FSM control register with lock

EUP2SPCPOWERDNFSMCTL - EUP 2 Power Down FSM control register with lock		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24710h	
DWord	**Bit**	**Description**
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM

EUP2SPCPOWERDNFSMCTL - EUP 2 Power Down FSM control register with lock

		Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks

EUP2SPCPOWERDNFSMCTL - EUP 2 Power Down FSM control register with lock		
		1xx = Rsvd for future Default : Assert Reset

EUP 2 Power on FSM control register with lock

EUP2SPCPOWERUPFSMCTL - EUP 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2470Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

EUP2SPCPOWERUPFSMCTL - EUP 2 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EUP3 BONUS1 Reg

EUP3SPCBONUS1 - EUP3 BONUS1 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24794h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe)

EUP3SPCBONUS1 - EUP3 BONUS1 Reg

		'1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP3 BONUS2 Reg

EUP3SPCBONUS2 - EUP3 BONUS2 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24798h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe)

EUP3SPCBONUS2 - EUP3 BONUS2 Reg

		'1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 1 PFET control register with lock

EUP1SPCPFETCTL - EU PAIR 1 PFET control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24688h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 1 PGFETCTL register are R/W 1 = All bits of EU PAIR 1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns

EUP1SPCPFETCTL - EU PAIR 1 PFET control register with lock

		3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) **Value**: 001b — **Name**: **[Default]**
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

EU PAIR 1 Power Context Save request

EUP1PGCTXREQ - EU PAIR 1 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24684h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 1 Power Down FSM control register with lock

EUP1SPCPOWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24690h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:

EUP1SPCPOWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

	0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
8:6	**Power Down state 3** Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Default : Gate Clocks

Value	Name
000b	Assert Reset
1xxb	Reserved
001b	Firewall ON
010b	Gate clocks **[Default]**

5:3	**Power Down state 2** Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Default: Firewall ON

Value	Name
1xxb	Reserved
010b	Gate clocks
000b	Assert Reset
001b	Firewall ON **[Default]**

2:0	**Power Down state 1** Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Default: Assert Reset

Value	Name
001b	Firewall ON
010b	Gate clocks

EUP1SPCPOWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

		1xxb	Reserved
		000b	Assert Reset **[Default]**

EU PAIR 1 Power Gate Control Request

EUP1PGCTLREQ - EU PAIR 1 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24680h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS EU PAIR 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 1 Power on FSM control register with lock

EUP1SPCPOWERUPFSMCTL - EU PAIR 1 Power on FSM control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 2468Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

EUP1SPCPOWERUPFSMCTL - EU PAIR 1 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EU PAIR 2 PGFET control register with lock

EUP2SPCPFETCTL - EU PAIR 2 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24708h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 PGFETCTL register are R/W 1 = All bits of EU PAIR 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns

EUP2SPCPFETCTL - EU PAIR 2 PGFET control register with lock

		3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Stroble pulse period** Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) **Value** / **Name** 001b / **[Default]**
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

EU PAIR 2 Power Context Save request

EUP2PGCTXREQ - EU PAIR 2 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24704h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 2 Power Gate Control Request

EUP2PGCTLREQ - EU PAIR 2 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24700h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS EU PAIR 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 3 PGFET control register with lock

EUP3SPCPFETCTL - EU PAIR 3 PGFET control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24788h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 PGFETCTL register are R/W 1 = All bits of EU PAIR 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns

EUP3SPCPFETCTL - EU PAIR 3 PGFET control register with lock

3'b101: 480ns
3'b110: 640ns
3'b111: 1280ns

18:16 **Time period last primay pfet strobe to secondary pfet strobe**

Access:	R/W Lock
_Custom_GTIReset:	BUS

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

Value	Name
001b	**[Default]**

15:0 **PFET Ladder Step Sequence**

Default Value:	1111111111111111b
Access:	R/W Lock
_Custom_GTIReset:	BUS

PFET Ladder STEP sequence
The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage.
The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0]
Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal.
15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.
15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

EU PAIR 3 Power Context Save request

EUP3PGCTXREQ - EU PAIR 3 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24784h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 3 Power Down FSM control register with lock

EUP3SPCPOWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24790h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:

EUP3SPCPOWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

		0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

EUP3SPCPOWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 3 Power Gate Control Request

EUP3PGCTLREQ - EU PAIR 3 Power Gate Control Request

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24780h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS EU PAIR 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 3 Power on FSM control register with lock

EUP3SPCPOWERUPFSMCTL - EU PAIR 3 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2478Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

EUP3SPCPOWERUPFSMCTL - EU PAIR 3 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Eviction counter status register

L3EVICTCNTR - Eviction counter status register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B12Ch	
DWord	**Bit**	**Description**
0	31:16	**Eviction Counter** Counter indicating total number of eviction in multiple of 64 events
	15:0	**C/Z Eviction Counter** Counter indicating total number of eviction (in multiple of 64 events) from C/Z (or unified tile cache) ways

Exec-List Context Offset

CXT_EL_OFFSET - Exec-List Context Offset	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	021ACh-021AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_RCSUNIT
Address:	181ACh-181AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_POCSUNIT
Address:	221ACh-221AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_BCSUNIT
Address:	1C01ACh-1C01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT0
Address:	1C41ACh-1C41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT1
Address:	1C81ACh-1C81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT0
Address:	1D01ACh-1D01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT2
Address:	1D41ACh-1D41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT3
Address:	1D81ACh-1D81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT1
Address:	1E01ACh-1E01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT4

CXT_EL_OFFSET - Exec-List Context Offset

Address:	1E41ACh-1E41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT5

Address:	1E81ACh-1E81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT2

Address:	1F01ACh-1F01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT6

Address:	1F41ACh-1F41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT7

Address:	1F81ACh-1F81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT3

Address:	1A1ACh-1A1AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_CCSUNIT0

This register provides the layout format of LRCA in Exec-List mode of scheduling. Each field represents its location in 4KB offset from LRCA base address. Register gets initialized to default value coming out of reset. SW must not program this register.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:20	**CSFE Engine Context Size** Value: 8h — Name: **[Default]**
	19:16	**Ring Context Offset** Default Value: 1h
	15:13	**Ring Context Size** Value: 5h — Name: **[Default]**
	12:4	**Reserved** Access: RO Format: MBZ

CXT_EL_OFFSET - Exec-List Context Offset			
	3:0	**PerProcess HW Status Page Offset**	
		Default Value:	0h

Execlist Control Register

EXECLIST_CONTROL - Execlist Control Register	
Register Space:	MMIO: 0/2/0
Access:	WO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02550h-02553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_RCSUNIT
Address:	18550h-18553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_POCSUNIT
Address:	22550h-22553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_BCSUNIT
Address:	1C0550h-1C0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT0
Address:	1C4550h-1C4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT1
Address:	1C8550h-1C8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT0
Address:	1D0550h-1D0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT2
Address:	1D4550h-1D4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT3
Address:	1D8550h-1D8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT1
Address:	1E0550h-1E0553h
Name:	EXECLIST CONTROL

EXECLIST_CONTROL - Execlist Control Register

ShortName:	EXECLIST_CONTROL_VCSUNIT4
Address:	1E4550h-1E4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT5
Address:	1E8550h-1E8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT2
Address:	1F0550h-1F0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT6
Address:	1F4550h-1F4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT7
Address:	1F8550h-1F8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT3
Address:	1A550h-1A553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_CCSUNIT0

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2	**Use HW Element Pointer** HW element pointer gets saved on a context getting preempted due to Preempt to Idle(indicates the element number of the preempted context in the EQ). On a load following Preempt to Idle SW can set "Use Element Pointer" to indicate HW to resume from the element on which preemption has occurred due to Preempt to Idle, not setting Use Element Pointer will result in HW executing from Element-0. o UseHWElementPointer = 1 : HW saves its position in the N deep execution Q across any C6 events. When HW sees Load + UseHWElementPointer, HW will restart execution at the element pointed to by the Element Pointer. • This usage is only expected post a PreemptToIdle message, and is independent of C6 entry-exit in between PreemptToIdle and Load. • Load+UseHWElementPointer on the first load (out of reset) will cause execution to begin at the first valid element in the Q • Load+UseHWElementPointer without a preceding PreemptToIdle (i.e. when trying to Preempt a currently running Q) will cause undefined behavior.

EXECLIST_CONTROL - Execlist Control Register		
		○ UseHWElementPointer = 0 : HW begins execution at the first valid element in the Q.
	1	**Preempt to Idle** When SW writes a 1 to this bit, HW will immediately copy the contents of the Execution queue into the Submission queue. HW will preempt the executing context on appropriate preemption boundary, saves state and invalidates all the pending elements of the execution queue to be executed. HW saves the element pointer of the EQ on which it got preempted (indicates the element number of the preempted context in the EQ), element pointer is power context save/restored by HW. This forces HW to go idle triggering idle sequence for power management. A Preempt-to-idle message must be followed by a Load message to resume operation. This Load message may occur before or after a power gating/C6 sequence
	0	**Load** Writing to the Load bit triggers HW to sample Submission Queue (SQ) to Execution Queue (EQ) and start executing from Element-0 of Execution Queue. Doing a Load during an ongoing execution of an context will result in preemption and the new submission queue gets sampled to Execution Queue, however HW will not start executing from the newly updated Execution Queue until the preempted context is completely saved. Multiple loads occurring during the preemption of an executing context will result in EQ getting updated multiple times with the SQ and engine will only execute the most up to date EQ available upon completion of the preemption.

Execlist Status

EXECLIST_STATUS - Execlist Status	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02234h-0223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_RCSUNIT
Address:	18234h-1823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_POCSUNIT
Address:	22234h-2223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_BCSUNIT
Address:	1C0234h-1C023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT0
Address:	1C4234h-1C423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT1
Address:	1C8234h-1C823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT0
Address:	1D0234h-1D023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT2
Address:	1D4234h-1D423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT3
Address:	1D8234h-1D823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT1
Address:	1E0234h-1E023Bh
Name:	RCS Execlist Status

EXECLIST_STATUS - Execlist Status

ShortName:	EXECLIST_STATUS_VCSUNIT4
Address:	1E4234h-1E423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT5
Address:	1E8234h-1E823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT2
Address:	1F0234h-1F023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT6
Address:	1F4234h-1F423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT7
Address:	1F8234h-1F823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT3
Address:	1A234h-1A23Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_CCSUNIT0

This register contains the pointers and full indicator for the Execlist Queue and the context ID of the currently running context.DefaultValue = UUUU UUU1h (4:0 default to 00001b, others UNDEFINED).

Programming Notes

This register functionality is not supported and must not be programmed for Position command streamer.

DWord	Bit	Description
0	63:32	**Current Context ID** Format: U32 Contains the context ID of the currently running context.
	31	**Reserved** Access: RO Format: MBZ
	30	**Pending Load** Format: U1 When set indicates the Load of SQ to EQ is complete. Hardware is in the process of making the first valid element of the EQ to be active (executing).

EXECLIST_STATUS - Execlist Status

29:28	**Reserved** Access: RO Format: MBZ
27	**Arbitration Enable** Format: U1 This field reflects the Arbitration Flag set by the MI_ARB_ON_OFF command in Command Streamer.
26:12	**Last Context Switch Reason** Access: R/W Format: U15

Description

This field contains the switch reason for the last context to switch away.

Bit	Defintion
12	Idle to Active (special case of Switch to New Queue)
13	Switch To New Queue
14	Element Switch
15	Active to Idle (special case of Element Switch)
16	Context Complete
17	Wait on Sync Flip
18	Wait on V-Blank
19	Wait on Semaphore
20	Wait on Scan Line
26:21	Reserved

Programming Notes

This field should not written by SW.

11:8	**Active Context Offset** When Active Context field is set, this field indicates the active context offset within the execution queue.
7	**Active Context** When set indicates there is an active context being executed in hardware.
6:5	**Reserved** Access: RO Format: MBZ
4	**Valid Execution Queue Duplicate** Indicates there is an active context or a pending context or a pending load in progress.

EXECLIST_STATUS - Execlist Status		
	3	**Valid Execution Queue** Indicates there is an active context or a pending context or a pending load in progress.
	2	**Preempt to Idle Pending** Preempt to Idle Pending: HW has received Preempt to Idle load request from the scheduler and hardware is in the process of switching out the active context if any to force HW go IDLE.
	1	**Two Pending Load's** Indicates there are two pending loads in HW, (n-1)th load's first valid element is being pursued by HW to be made active and the Nth loads first valid element will be considered once (N-1)th is active. This situation will arise when Nth load happens while (N-1)th load is pending in hardware. Any further Load (N+1) occurring while this bit is set will result in overwriting the Nth SQ load, that is Nth SQ load contents will never be seen by hardware.
	0	**Execution Queue Invalid** Default Value: 1h There are no contexts available in Execution Queue to be executed. There are no pending loads (including Preempt To Idle) to be processed by the hardware. Scheduler can look for this bit to be set before doing a load of SQ to avoid preemption of any active contexts in hardware.

Execlist Submission Queue Contents

EXECLIST_SQ_CONTENTS - Execlist Submission Queue Contents	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	512
_Custom_GTIReset:	DEV
Address:	02510h-0254Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_RCSUNIT
Address:	18510h-1854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_POCSUNIT
Address:	22510h-2254Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_BCSUNIT
Address:	1C0510h-1C054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT0
Address:	1C4510h-1C454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT1
Address:	1C8510h-1C854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT0
Address:	1D0510h-1D054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT2
Address:	1D4510h-1D454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT3
Address:	1D8510h-1D854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT1
Address:	1E0510h-1E054Fh
Name:	EXECLIST SQ CONTENTS

EXECLIST_SQ_CONTENTS - Execlist Submission Queue Contents

ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT4
Address:	1E4510h-1E454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT5
Address:	1E8510h-1E854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT2
Address:	1F0510h-1F054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT6
Address:	1F4510h-1F454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT7
Address:	1F8510h-1F854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT3
Address:	1A510h-1A54Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_CCSUNIT0

Contents of submission queue from Element-0 to Element-7.

All "Element* Low Dword" have the format of the Bits[31:0] of the "Context Descriptor" definition.
All "Element* HighDword" have the format of the Bits[63:32] of the "Context Descriptor" definition.

DWord	Bit	Description
0	31:0	**Element 0 Low DWord** Format: U32
1	31:0	**Element 0 High DWord** Format: U32
2	31:0	**Element 1 Low DWord** Format: U32
3	31:0	**Element 1 High DWord** Format: U32
4	31:0	**Element 2 Low DWord** Format: U32
5	31:0	**Element 2 High DWord** Format: U32

EXECLIST_SQ_CONTENTS - Execlist Submission Queue Contents		
6	31:0	**Element 3 Low DWord** Format: U32
7	31:0	**Element 3 High DWord** Format: U32
8	31:0	**Element 4 Low DWord** Format: U32
9	31:0	**Element 4 High DWord** Format: U32
10	31:0	**Element 5 Low DWord** Format: U32
11	31:0	**Element 5 High DWord** Format: U32
12	31:0	**Element 6 Low DWord** Format: U32
13	31:0	**Element 6 High DWord** Format: U32
14	31:0	**Element 7 Low DWord** Format: U32
15	31:0	**Element 7 High DWord** Format: U32

Execlist Submit Port Register

EXECLIST_SUBMITPORT - Execlist Submit Port Register	
Register Space:	MMIO: 0/2/0
Access:	WO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02230h-02233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_RCSUNIT
Address:	18230h-18233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_POCSUNIT
Address:	22230h-22233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_BCSUNIT
Address:	1C0230h-1C0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT0
Address:	1C4230h-1C4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT1
Address:	1C8230h-1C8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT0
Address:	1D0230h-1D0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT2
Address:	1D4230h-1D4233h
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT3
Address:	1D8230h-1D8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT1
Address:	1E0230h-1E0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT4

EXECLIST_SUBMITPORT - Execlist Submit Port Register

Address:	1E4230h-1E4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT5

Address:	1E8230h-1E8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT2

Address:	1F0230h-1F0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT6

Address:	1F4230h-1F4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT7

Address:	1F8230h-1F8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT3

Address:	1A230h-1A233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_CCSUNIT0

ELSP provides a mechanism to load the elements of the Submission Queue in a cyclic order starting from Element-0 to Element-7. Consecutive writes to ELSP results in progressively updating lower dword followed by upper dword of successive elements starting from Element-0 to Element7. On reaching upper dword of Element-7 it wraps back to lower dword of Element-0.
Example: The first dword write to ELSP results in updating the lower dword of Element-0 and the following write updates the upper dword of Element-0 and the following write updates the lower dword of Element-1 and so on, on updating upper dword of Element-7 it wraps back to lower dword of Element-0.

DWord	Bit	Description
0	31:0	**Context Descriptor DW** Format: U32 See "Context Descriptor Format" for format. The element that this DW is submitted as and whether it is the high DW or the low DW is determined by order. This register must be written to 16 times in order to write to all the eight elements of an Submission Queue. .

Execute Condition Code Register

EXCC - Execute Condition Code Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02028h-0202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_RCSUNIT
Address:	18028h-1802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_POCSUNIT
Address:	22028h-2202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_BCSUNIT
Address:	1C0028h-1C002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT0
Address:	1C4028h-1C402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT1
Address:	1C8028h-1C802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT0
Address:	1D0028h-1D002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT2
Address:	1D4028h-1D402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT3
Address:	1D8028h-1D802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT1
Address:	1E0028h-1E002Bh
Name:	Execute Condition Code Register

EXCC - Execute Condition Code Register

ShortName:	EXCC_VCSUNIT4
Address:	1E4028h-1E402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT5
Address:	1E8028h-1E802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT2
Address:	1F0028h-1F002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT6
Address:	1F4028h-1F402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT7
Address:	1F8028h-1F802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT3
Address:	1A028h-1A02Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_CCSUNIT0

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Context Wait for V-blank on Pipe-D** This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.

EXCC - Execute Condition Code Register

	14	**Context Wait for V-blank on Pipe-C** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	13	**Context Wait for V-blank on Pipe-B** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	12	**Context Wait for V-blank on Pipe-A** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	11:5	**Reserved** Access: RO Format: MBZ
	4:0	**User Defined Condition Codes** Source: RenderCS The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

Execution Queue Element Mask

EQ_ELEMENT_MASK - Execution Queue Element Mask	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0256Ch-0256Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_RCSUNIT
Address:	1856Ch-1856Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_POCSUNIT
Address:	2256Ch-2256Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_BCSUNIT
Address:	1C056Ch-1C056Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT0
Address:	1C456Ch-1C456Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT1
Address:	1C856Ch-1C856Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VECSUNIT0
Address:	1D056Ch-1D056Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT2
Address:	1D456Ch-1D456Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT3
Address:	1D856Ch-1D856Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VECSUNIT1
Address:	1E056Ch-1E056Fh
Name:	EQ_ELEMENT_MASK

EQ_ELEMENT_MASK - Execution Queue Element Mask

ShortName:	EQ_ELEMENT_MASK_VCSUNIT4
Address:	1E456Ch-1E456Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT5
Address:	1E856Ch-1E856Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VECSUNIT2
Address:	1F056Ch-1F056Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT6
Address:	1F456Ch-1F456Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VCSUNIT7
Address:	1F856Ch-1F856Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_VECSUNIT3
Address:	1A56Ch-1A56Fh
Name:	EQ_ELEMENT_MASK
ShortName:	EQ_ELEMENT_MASK_CCSUNIT0

This register captures the status of the elements executed from an Execution Queue on Preempt to Idle. HW looks at this register on Load with Use HW Element Pointer to pick the right element (instead of default Element-0) to execute in order to resume from where it got preempted on Preempt To Idle. This register must not be programmed by SW. This register is power context save/restored by HW.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:0	**Load** Each bit in the mask corresponds to an element in the execution queue. Bit[0] corresponds to Element-0 and Bit[7] corresponds to Element-7 of the EQ. Bit set for an element indicates the element is executed. Bit Reset for an element indicates either the element is invalid or pending execution (a preempted context is treated as pending execution).

FAULT_TLB_RD_DATA1 Register

FAULT_TLB_RD_DATA1 - FAULT_TLB_RD_DATA1 Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CEBCh

DWord	Bit	Description
0	31:9	**Reserved** Access: RO Format: MBZ
	8:7	**TLB Entry Page Size** Default Value: 00b Access: RO 2'b00 - 4k, 2'b01 - 64k, 2'b10 - 2M, 2'b11 - 1G
	6	**TLB Entry Present** Default Value: 0h Access: RO 1'b1 - Present, 1'b0 - Not Present
	5	**TLB Entry Valid** Default Value: 0h Access: RO 1'b1 - Valid, 1'b0 - Not Valid
	4	**Cycle GTT Sel** Default Value: 0h Access: RO Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle)
	3:0	**Address** Default Value: 0000b Access: RO Bit[3:0] Fault cycle Virtual address [47:44]

FBC_CFB_BASE

FBC_CFB_BASE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	43200h-43203h
Name:	FBC Compressed Buffer Address
ShortName:	FBC_CFB_BASE_A
Reset:	soft

Restriction
The contents of this register must not be changed while compression is enabled.

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27:12	**CFB Offset Address** This register specifies bits 27:12 of the offset of the Compressed Frame Buffer from the base of stolen memory. A programmed value of 0x0001 in this field corresponds to an offset of 0x1000 (4K) bytes. **Restriction** The buffer must be 4K byte aligned, which is enforced by reserving bits 11:0. The offset must be greater than 4K bytes, avoiding the first 4KB of stolen memory.
	11:0	**Reserved** Access: RO Format: MBZ

FBC_CTL

FBC_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	43208h-4320Bh
Name:	FBC Control
ShortName:	FBC_CTL_A
Reset:	soft

Description
FBC is tied to Plane 1 A.

Programming Notes
Frame Buffer Compression is not supported with per-pixel alpha. Software must disable FBC for per-pixel alpha formats.
Frame Buffer Compression is supported with surfaces of up to 8192 pixels x 4096 lines and plane sizes up to 5120 pixels x 4096 lines.
The FBC compressed vertical limit is 2560 lines, after which the remaining lines will be displayed correctly, but will not be compressed.
Compression ratios cannot be changed dynamically. FBC must be disabled and reenabled when changing compression ratios.

Restriction
The contents of this register must not be changed, except the enable bit, while compression is enabled.
Frame Buffer Compression is only supported with 16bpp and 32bpp 8:8:8 RGB plane source pixel formats. It is not supported with any other format. The 16bpp format requires the compression ratio to be set to 2:1 or 4:1. FBC is not supported with RGB 16bpp plane formats when plane 90/270 rotation is enabled. Frame Buffer Compression is only supported while the plane it is tied to has a source size of at least 200 pixels x 32 lines. Software must disable FBC for the non-supported pixel formats and sizes.
Frame Buffer Compression is not supported with interlaced fetch. With plane 90/270 rotation, all frame buffer modifications will result in full frame invalidation and recompression.

DWord	Bit	Description
0	31	**Enable FBC** This bit is used to globally enable FBC function at the next Vertical Blank start. FBC should not be enabled when the pipe is disabled.

Value	Name
0b	Disable

FBC_CTL

	1b	Enable

30	**Reserved** Access: RO Format: MBZ
29	**Reserved** Access: RO Format: MBZ
28	**Reserved**
27:19	**Reserved** Access: RO Format: MBZ
18	**Reserved**
17	**Reserved**
16	**Reserved**
15	**Reserved**
14:13	**Reserved** Access: RO Format: MBZ
12:11	**Reserved** Access: RO Format: MBZ
10	**Reserved**
9:8	**Reserved**
7:6	**Compression Limit** This register sets a minimum limit on compression. This determines the maximum size of the compressed frame buffer. Display lines that do not meet the compression limit will not be compressed, so the best compression will be achieved with a 1:1 ratio. FBC processes received pixels as 32bpp irrespective of pixel format, so that CFB buffer sizing for 16bpp is indicated below: Compression Ratio 1, Pixel Format 16 bpp - Not Supported Compression Ratio 1, Pixel Format 32 bpp - Supported (CFB=FB) Compression Ratio 1/2, Pixel Format 16 bpp - Supported (CFB=FB) Compression Ratio 1/2, Pixel Format 32 bpp - Supported (CFB=1/2 FB) Compression Ratio 1/4, Pixel Format 16 bpp - Supported (CFB=1/2 FB) Compression Ratio 1/4, Pixel Format 32 bpp - Supported (CFB=1/4 FB) FB = Frame Buffer Size CFB = Compressed Frame Buffer Size

Value	Name	Description
00b	1:1	Compressed buffer is the same size as the uncompressed buffer.

01b	2:1	Compressed buffer is one half the size of the uncompressed buffer.
10b	4:1	Compressed buffer is one quarter the size of the uncompressed buffer.
11b	Reserved	Reserved

5:4 Write Back Watermark

The compressed data write back engine waits for this number of entries to be ready before writing the data out to memory.

Value	Name	Description
00b	4	4 entries
01b	8	8 entries
10b	16	16 entries
11b	32	32 entries

3:0 Reserved

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	07020h

This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:12	**FBC RT Base Address** Access: R/W Format: GraphicsAddress[31:12] _Custom_GTIReset: DEV 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.
	11:2	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	1	**FBC Front Buffer Target** Access: R/W _Custom_GTIReset: DEV Value / Name / Description: 0h / **[Default]** / FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression. 1h / / FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.
	0	**PPGTT Render Target Base Address Valid for FBC** Access: R/W _Custom_GTIReset: DEV Value / Name / Description: 0h / **[Default]** / Base address in this register [31:12] is not valid and therefore FBC will not get any modifications from rendering. 1h / / Base address in this register [31:12] is valid and HW needs to compare the

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER				
				current render target base address with this base address to provide modifications to FBC.

FBC_RT_BASE_ADDR_REGISTER_UPPER

FBC_RT_BASE_ADDR_REGISTER_UPPER - FBC_RT_BASE_ADDR_REGISTER_UPPER

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	07024h

This Register is saved and restored as part of Context.

Programming Notes

"Render Tracking with Nuke" is the only FBC functional mode supported by render engine. SW must always program the FBC_RT_BASE_ADDR_REGISTER_* register in Render Engine to a reserved value (0xFFFF_FFFF) such that the programmed value doesn't match the render target surface address programmed. This would disable render engine from generating modify messages to FBC unit in display. Refer "Frame Buffer Compression" section for more details related to FBC functionality and programming.

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	15:0	**FBC RT Base Address Upper DWORD** Access: R/W Format: GraphicsAddress[47:32] _Custom_GTIReset: DEV Must be set to modify corresponding data bit. Reads to this field returns zero.Upper 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It can be only programmed once per context. **Programming Notes** It must be programmed before any draw call binding that render target base address.

FBC LLC Config Read Control Register

FBC_LLC_READ_CTRL - FBC LLC Config Read Control Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09044h

FBC LLC Config Read Control Register

DWord	Bit	Description
0	31	**FBC LLC Config Read Control Register Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of FBC_CTRL Register are R/W. 1 = All bits of FBC_CTRL Register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 does not clear the lock). These bits are not reset on FLR.
	30	**FBC LLC Config Start Value** Default Value: 1b Access: R/W Lock _Custom_GTIReset: BUS PCU_CR_LLC_CONFIG Read Cycle Interval in microseconds (1333ns normal). 1'b0 - Treat LLC as partially open on reset (boot or C6 exit) (Default). 1'b1 - Treat LLC as fully open on reset (boot or C6 exit). This must not be set unless coordinated with Uncore.
	29:16	**Reserved** Access: RO Format: MBZ
	15:0	**FBC LLC Config Read Interval** Default Value: 00FFh Access: R/W Lock _Custom_GTIReset: BUS PCU_CR_LLC_CONFIG Read Cycle Interval in microseconds (1333ns normal). 0x0000: Do not read PCU_CR_LLC_CONFIG (use Start Value only). 0x0001-0xFFFF : Read PCU_CR_LLC_CONFIG at the specified interval, until LLC_FULLY_OPEN=1. Default: 0xFF (approx 170us).

FENCE_LSB

FENCE_LSB	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100020h
Name:	FENCE4_LSB
ShortName:	FENCE4_LSB
Address:	100028h
Name:	FENCE5_LSB
ShortName:	FENCE5_LSB
Address:	100030h
Name:	FENCE6_LSB
ShortName:	FENCE6_LSB
Address:	100038h
Name:	FENCE7_LSB
ShortName:	FENCE7_LSB
Address:	100040h
Name:	FENCE8_LSB
ShortName:	FENCE8_LSB
Address:	100048h
Name:	FENCE9_LSB
ShortName:	FENCE9_LSB
Address:	100050h
Name:	FENCE10_LSB
ShortName:	FENCE10_LSB
Address:	100058h
Name:	FENCE11_LSB
ShortName:	FENCE11_LSB
Address:	100060h
Name:	FENCE12_LSB
ShortName:	FENCE12_LSB
Address:	100068h
Name:	FENCE13_LSB
ShortName:	FENCE13_LSB

FENCE_LSB	
Address:	100070h
Name:	FENCE14_LSB
ShortName:	FENCE14_LSB
Address:	100078h
Name:	FENCE15_LSB
ShortName:	FENCE15_LSB
Address:	100080h
Name:	FENCE16_LSB
ShortName:	FENCE16_LSB
Address:	100088h
Name:	FENCE17_LSB
ShortName:	FENCE17_LSB
Address:	100090h
Name:	FENCE18_LSB
ShortName:	FENCE18_LSB
Address:	100098h
Name:	FENCE19_LSB
ShortName:	FENCE19_LSB
Address:	1000A0h
Name:	FENCE20_LSB
ShortName:	FENCE20_LSB
Address:	1000A8h
Name:	FENCE21_LSB
ShortName:	FENCE21_LSB
Address:	1000B0h
Name:	FENCE22_LSB
ShortName:	FENCE22_LSB
Address:	1000B8h
Name:	FENCE23_LSB
ShortName:	FENCE23_LSB
Address:	1000C0h
Name:	FENCE24_LSB
ShortName:	FENCE24_LSB
Address:	1000C8h
Name:	FENCE25_LSB

FENCE_LSB

ShortName:	FENCE25_LSB
Address:	1000D0h
Name:	FENCE26_LSB
ShortName:	FENCE26_LSB
Address:	1000D8h
Name:	FENCE27_LSB
ShortName:	FENCE27_LSB
Address:	1000E0h
Name:	FENCE28_LSB
ShortName:	FENCE28_LSB
Address:	1000E8h
Name:	FENCE29_LSB
ShortName:	FENCE29_LSB
Address:	1000F0h
Name:	FENCE30_LSB
ShortName:	FENCE30_LSB
Address:	1000F8h
Name:	FENCE31_LSB
ShortName:	FENCE31_LSB

Fence Registers LSBs

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="3">0</td><td>31:12</td><td>FENCELO<table><tr><td>Default Value:</td><td>000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td>_Custom_GTIReset:</td><td>BUS</td></tr></table>Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page.
This address represents the last 4KB page of the fence region (Lower Bound is included in the fence region).
Graphics Address is the offset within GMADR space.</td></tr>
<tr><td>11:2</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>1</td><td>TILE<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table></td></tr>
</table>

FENCE_LSB

		_Custom_GTIReset: BUS This field specifies the spatial ordering of QW within tiles. 0b - Consecutive SWords (32B) sequenced in the X direction 1b - Consecutive OWords (16B) sequenced in the Y direction
	0	**FENCEVAL** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This field specifies whether or not this fence register defines a fence region. 0b - FENCE INVALID 1b - FENCE VALID

FENCE_MSB

FENCE_MSB	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100024h
Name:	FENCE4_MSB
ShortName:	FENCE4_MSB
Address:	10002Ch
Name:	FENCE5_MSB
ShortName:	FENCE5_MSB
Address:	100034h
Name:	FENCE6_MSB
ShortName:	FENCE6_MSB
Address:	10003Ch
Name:	FENCE7_MSB
ShortName:	FENCE7_MSB
Address:	100044h
Name:	FENCE8_MSB
ShortName:	FENCE8_MSB
Address:	10004Ch
Name:	FENCE9_MSB
ShortName:	FENCE9_MSB
Address:	100054h
Name:	FENCE10_MSB
ShortName:	FENCE10_MSB
Address:	10005Ch
Name:	FENCE11_MSB
ShortName:	FENCE11_MSB
Address:	100064h
Name:	FENCE12_MSB
ShortName:	FENCE12_MSB
Address:	10006Ch
Name:	FENCE13_MSB
ShortName:	FENCE13_MSB

FENCE_MSB	
Address:	100074h
Name:	FENCE14_MSB
ShortName:	FENCE14_MSB
Address:	10007Ch
Name:	FENCE15_MSB
ShortName:	FENCE15_MSB
Address:	100084h
Name:	FENCE16_MSB
ShortName:	FENCE16_MSB
Address:	10008Ch
Name:	FENCE17_MSB
ShortName:	FENCE17_MSB
Address:	100094h
Name:	FENCE18_MSB
ShortName:	FENCE18_MSB
Address:	10009Ch
Name:	FENCE19_MSB
ShortName:	FENCE19_MSB
Address:	1000A4h
Name:	FENCE20_MSB
ShortName:	FENCE20_MSB
Address:	1000ACh
Name:	FENCE21_MSB
ShortName:	FENCE21_MSB
Address:	1000B4h
Name:	FENCE22_MSB
ShortName:	FENCE22_MSB
Address:	1000BCh
Name:	FENCE23_MSB
ShortName:	FENCE23_MSB
Address:	1000C4h
Name:	FENCE24_MSB
ShortName:	FENCE24_MSB
Address:	1000CCh
Name:	FENCE25_MSB

FENCE_MSB

ShortName:	FENCE25_MSB
Address:	1000D4h
Name:	FENCE26_MSB
ShortName:	FENCE26_MSB
Address:	1000DCh
Name:	FENCE27_MSB
ShortName:	FENCE27_MSB
Address:	1000E4h
Name:	FENCE28_MSB
ShortName:	FENCE28_MSB
Address:	1000ECh
Name:	FENCE29_MSB
ShortName:	FENCE29_MSB
Address:	1000F4h
Name:	FENCE30_MSB
ShortName:	FENCE30_MSB
Address:	1000FCh
Name:	FENCE31_MSB
ShortName:	FENCE31_MSB

Fence Registers MSBs

DWord	Bit	Description
0	31:12	**FENCEUP** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11	**Reserved** Access: RO Format: MBZ

FENCE_MSB

	10:0	**Pitch** Default Value: 000h Access: R/W _Custom_GTIReset: BUS This field specifies the width (pitch) of the fence region in multiple of tile widths. For Tile X this field must be programmed to a multiple of 512B (003 is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B (000 is the minimum value). 000h = 128B 001h = 256B 002h = 384B 003h = 512B 004h = 640B 005h = 768B 006h = 896B 007h = 1024B ... 3FFh = 128KB 4FFh = 160KB 5FFh = 192KB 6FFh = 224KB 7FFh = 256KB

Fence Control Register

MFCR - Fence Control Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09070h

Fence Control Register

DWord	Bit	Description
0	31	**Fuse Override Lock** Access: R/W Lock _Custom_GTIReset: BUS SW Fuse Override Lock Bit
	30:28	**ECORSVD** Access: R/W _Custom_GTIReset: BUS ECO purposes Reserved
	27:26	**GT VBOX DISABLE FUSE OVERRIDE** Access: R/W Lock _Custom_GTIReset: BUS S/W GT Vbox Disable Fuse Override Bits
	25:22	**GT SUBSLICE DISABLE FUSE OVERRIDE** Access: R/W Lock _Custom_GTIReset: BUS SW GT SubSlice Disable Fuse Override Bits
	21:16	**GT SLICE ENABLE FUSE OVERRIDE** Default Value: 111111b Access: R/W Lock _Custom_GTIReset: BUS SW GT Slice Enable Fuse Override Bits
	15:5	**Reserved** Access: RO Format: MBZ
	4	**Reserved**
	3	**Reserved**

MFCR - Fence Control Register

	2	**Write/Read Port Block** Access: R/W _Custom_GTIReset: BUS 0 - Dont Block the R/W port when Query is started. 1 - Block the R/W port until the Memory Fence is completed. This is applicable for only Memory Fence.
	1	**LLC Query Enable** Access: R/W _Custom_GTIReset: BUS 0 - Query for 16 Ways. 1 - Query for 32 Ways. No Flexing.
	0	**Fence Controller GFDT Mode** Access: R/W _Custom_GTIReset: BUS Fence Controller GFDT Mode. 0 - Single bit GFDT mode. 1 - Two bit GFDT mode.

FF Performance

FF_PERF - FF Performance

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	06B1Ch
Name:	Render CS FF Performance
ShortName:	RCS_FF_PERF
Address:	17B1Ch
Name:	Position CS POSH Pipeline FF Performance
ShortName:	PCS_FF_PERF

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	10:8	**Throttle counter value** Access: R/W _Custom_GTIReset: DEV Counter value defining how many clocks the interface needs to be slowed down. Value: 0h — Name: **[Default]** — Description: Masked by default.
	7:3	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	2	**Enable throttling for SF-WM interface** Access: R/W _Custom_GTIReset: DEV

FF_PERF - FF Performance

Value	Name	Description
0h	Disable_2	No throttling
1h	Enable_2	Enable throttling in all SF-WM interfaces

Programming Notes
This field must not be programmed for SVGR unit.

1 **Enable throttling for SF-SBE interface**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Disable_1	No throttling
1h	Enable_1	Enable throttling in all SF-SBE interfaces

Programming Notes
This field must not be programmed for SVGR unit.

0 **Enable throttling for CL-SF interface**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Disable_0	No throttling
1h	Enable_0	Enable throttling in all CL-SF interfaces

Restriction
This bit must not be set. SW may choose to use SF-SBE throttle interface(bit 1) to achieve the same effect.

First MGSR read done

FIRST_MGSR_READ_DONE - First MGSR read done	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1C2DA4h-1C2DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG0
Address:	1C6DA4h-1C6DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG1
Address:	1D2DA4h-1D2DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG2
Address:	1D6DA4h-1D6DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG3
Address:	1E2DA4h-1E2DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG4
Address:	1E6DA4h-1E6DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG5
Address:	1F2DA4h-1F2DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG6
Address:	1F6DA4h-1F6DA7h
Name:	First MGSR read done
ShortName:	FIRST_MGSR_READ_DONE_VDENC_REG7
This register is used to enable wrap around cases in the current testbench. There is not good way to identify the delay that should be introduced in Primary.bfl file before the wrapped around value is written to MGSR register. RTL will write 1 to this register when the first value is read by ECP and reset at frame_flop_reset. This will indicate that the read has happened and the wrap around can happen. this is introduced, because in real life it should never happen that the tailptr value read by ECP is of the next frame before reading at least one tailptr value of this frame.	

DWord	Bit	Description

FIRST_MGSR_READ_DONE - First MGSR read done		
0	31:16	**mgsr_return_value_zero** Access: RO This field is cleared when a WL is submitted to VDENC and set if the tail pointer value received by VDENC is zero..
	15:8	**VDENC_End_of_frame_processed** Access: RO This field is cleared when a WL is submitted to VDENC and set after VDENC process entire frame.
	7:0	**First_MGSR_read_done** Access: RO This field is cleared when a WL is submitted to VDENC and set after reading first tail pointer from MGSR.

First VF Offset

FIRST_VF_OFFSET_0_2_0_PCI - First VF Offset		
Register Space: PCI: 0/2/0 Size (in bits): 16		
Address: 00334h		
Defines the offset of the function number from the PF to the first VF.		
DWord	**Bit**	**Description**
0	15:0	**FIRST VF OFFSET VALUE** Default Value: 0000000000000001b Access: RO _Custom_GTIReset: BUS Defines the routing ID offset of the first VF that is associated with the PF that contains this Capability structure. The first VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the PF containing this field ignoring any carry, using unsigned, 16-bit arithmetic. The value of this field is hardwired to 0001h.

FIX BONUS1 Reg

FIXSPCBONUS1 - FIX BONUS1 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24314h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIXSPCBONUS1 - FIX BONUS1 Reg

	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIX BONUS2 Reg

FIXSPCBONUS2 - FIX BONUS2 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24318h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIXSPCBONUS2 - FIX BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIX PGFET control register with lock

FIXSPCPFETCTL - FIX PGFET control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24308h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns

FIXSPCPFETCTL - FIX PGFET control register with lock

3'b011: 240ns
3'b100: 320ns
3'b101: 480ns
3'b110: 640ns
3'b111: 1280ns

Value	Name
101b	**[Default]**

18:16 **Strobe pulse period**

Default Value:	010b
Access:	R/W Lock
_Custom_GTIReset:	BUS

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

15:0 **PFET Ladder Step Sequence**

Default Value:	1111111111111111b
Access:	R/W Lock
_Custom_GTIReset:	BUS

PFET Ladder STEP sequence
The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage.
The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0]
Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal.
15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.
15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Fix Power Context Save request

FIXPGCTXREQ - Fix Power Context Save request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24304h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

FIX Power Down FSM control register with lock

FIXSPCPOWERDNFSMCTL - FIX Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24310h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

FIXSPCPOWERDNFSMCTL - FIX Power Down FSM control register with lock

10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

FIXSPCPOWERDNFSMCTL - FIX Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Fix Power Gate Control Request

FIXPGCTLREQ - Fix Power Gate Control Request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24300h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIX Power on FSM control register with lock

FIXSPCPOWERUPFSMCTL - FIX Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2430Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

FIXSPCPOWERUPFSMCTL - FIX Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Flexible EU Event Control 0

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E458h

This register configures flexible EU event 0/1. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 1. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 1. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 1. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 0. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 **Coarse Event Filter Select EU event 0**

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 0. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 **Increment Event for EU event 0**

This field controls which increment event provides the basis for flexible EU event 0.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

Flexible EU Event Control 1

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E558h

This register configures flexible EU event 2/3. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 3** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 3. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 3** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 3. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 3** This field controls which increment event provides the basis for flexible EU event 3. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	11:8	**Fine Event Filter Select EU event 2** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 2. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 **Coarse Event Filter Select EU event 2**

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 2. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 **Increment Event for EU event 2**

This field controls which increment event provides the basis for flexible EU event 2.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

Flexible EU Event Control 2

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E658h

This register configures flexible EU event 4/5. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 5** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 5. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA]
	19:16	**Coarse Event Filter Select EU event 5** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 5. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]
	15:12	**Increment Event for EU event 5** This field controls which increment event provides the basis for flexible EU event 5. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]
	11:8	**Fine Event Filter Select EU event 4** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 4. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 Coarse Event Filter Select EU event 4

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 4. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 Increment Event for EU event 4

This field controls which increment event provides the basis for flexible EU event 4.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

Flexible EU Event Control 3

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E758h

This register configures flexible EU event 6/7. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 7** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 7. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 7** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 7. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 7** This field controls which increment event provides the basis for flexible EU event 7. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	11:8	**Fine Event Filter Select EU event 6** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 6. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 **Coarse Event Filter Select EU event 6**

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 6. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 **Increment Event for EU event 6**

This field controls which increment event provides the basis for flexible EU event 6.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

Flexible EU Event Control 4

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E45Ch

This register configures flexible EU event 8/9. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 9** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 9. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 9** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 9. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 9** This field controls which increment event provides the basis for flexible EU event 9. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	11:8	**Fine Event Filter Select EU event 8** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 8. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 **Coarse Event Filter Select EU event 8**

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 8. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 **Increment Event for EU event 8**

This field controls which increment event provides the basis for flexible EU event 8.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

Flexible EU Event Control 5

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E55Ch

This register configures flexible EU event 10/11. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 11** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 11. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 11** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 11. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 11** This field controls which increment event provides the basis for flexible EU event 11. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	11:8	**Fine Event Filter Select EU event 10** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 10. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 **Coarse Event Filter Select EU event 10**

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 10. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 **Increment Event for EU event 10**

This field controls which increment event provides the basis for flexible EU event 10.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

Flexible EU Event Control 6

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E65Ch

This register configures flexible EU event 12/13. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:20	**Fine Event Filter Select EU event 13** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 13. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 13** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 13. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 13** This field controls which increment event provides the basis for flexible EU event 13. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	11:8	**Fine Event Filter Select EU event 12** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 12. Note that the fine event filter is logically applied after the coarse

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6

event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0xA]	

7:4 **Coarse Event Filter Select EU event 12**

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 12. Note that the coarse event filter is logically applied before the fine event filter.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

3:0 **Increment Event for EU event 12**

This field controls which increment event provides the basis for flexible EU event 12.

Value	Name
0xf	Default **[Default]**
[0x0-0x8]	

FLT_RPT0

FLT_RPT0 - FLT_RPT0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	124810h

GT uses this register to post VT-d faults

DWord	Bit	Description
0	31:12	**FI** Default Value: 00000h Access: R/W _Custom_GTIReset: BUS Fault Info.
	11:0	**Reserved** Access: RO Format: MBZ

FLT_RPT1

FLT_RPT1 - FLT_RPT1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	124814h	
GT uses this register to post VT-d faults		
DWord	**Bit**	**Description**
0	31:0	**FI** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS Fault Info.

FLT_RPT2

FLT_RPT2 - FLT_RPT2

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	124818h

GT uses this register to post VT-d faults

DWord	Bit	Description
0	31	**PP** Default Value: 0h Access: R/W _Custom_GTIReset: BUS PASID Present.
	30	**EXE** Default Value: 0h Access: R/W _Custom_GTIReset: BUS Execute Permission Requested.
	29	**PRIV** Default Value: 0h Access: R/W _Custom_GTIReset: BUS Privilege Mode Requested .
	28:16	**Reserved** Access: RO Format: MBZ
	15:0	**Source ID** Default Value: 0010h Access: RO _Custom_GTIReset: BUS Source ID.

FLT_RPT3

FLT_RPT3 - FLT_RPT3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	12481Ch

GT uses this register to post VT-d faults

DWord	Bit	Description
0	31	**F** Default Value: 0h Access: R/W _Custom_GTIReset: BUS Fault
	30	**T** Default Value: 0h Access: R/W _Custom_GTIReset: BUS Type
	29:28	**AT** Default Value: 0h Access: R/W _Custom_GTIReset: BUS Address Type
	27:8	**PN** Default Value: 00000h Access: R/W _Custom_GTIReset: BUS PASID Number
	7:0	**FR** Default Value: 0h Access: R/W _Custom_GTIReset: BUS Fault Reason

FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	024D0h-024D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_RCSUNIT
Address:	024D4h-024D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_RCSUNIT
Address:	024D8h-024DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_RCSUNIT
Address:	024DCh-024DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_RCSUNIT
Address:	024E0h-024E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_RCSUNIT
Address:	024E4h-024E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_RCSUNIT
Address:	024E8h-024EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_RCSUNIT
Address:	024ECh-024EFh
Name:	FORCE_TO_NONPRIV
Address:	024F0h-024F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_RCSUNIT
Address:	024F4h-024F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_RCSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	024F8h-024FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_RCSUNIT
Address:	024FCh-024FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_RCSUNIT
Address:	02010h-02013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_RCSUNIT
Address:	02014h-02017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_RCSUNIT
Address:	02018h-0201Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_RCSUNIT
Address:	0201Ch-0201Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_RCSUNIT
Address:	021E0h-021E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_RCSUNIT
Address:	021E4h-021E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_RCSUNIT
Address:	021E8h-021EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_RCSUNIT
Address:	021ECh-021EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_RCSUNIT
Address:	184D0h-184D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_POCSUNIT
Address:	184D4h-184D7h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_1_POCSUNIT
Address:	184D8h-184DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_POCSUNIT
Address:	184DCh-184DFh
Name:	FORCE_TO_NONPRIV
Address:	184E0h-184E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_POCSUNIT
Address:	184E4h-184E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_POCSUNIT
Address:	184E8h-184EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_POCSUNIT
Address:	184ECh-184EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_POCSUNIT
Address:	184F0h-184F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_POCSUNIT
Address:	184F4h-184F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_POCSUNIT
Address:	184F8h-184FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_POCSUNIT
Address:	184FCh-184FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_POCSUNIT
Address:	18010h-18013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_POCSUNIT
Address:	18014h-18017h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_13_POCSUNIT
Address:	18018h-1801Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_POCSUNIT
Address:	1801Ch-1801Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_POCSUNIT
Address:	181E0h-181E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_POCSUNIT
Address:	181E4h-181E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_POCSUNIT
Address:	181E8h-181EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_POCSUNIT
Address:	181ECh-181EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_POCSUNIT
Address:	224D0h-224D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_BCSUNIT
Address:	224D4h-224D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_BCSUNIT
Address:	224D8h-224DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_BCSUNIT
Address:	224DCh-224DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_BCSUNIT
Address:	224E0h-224E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_BCSUNIT
Address:	224E4h-224E7h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_BCSUNIT
Address:	224E8h-224EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_BCSUNIT
Address:	224ECh-224EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_BCSUNIT
Address:	224F0h-224F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_BCSUNIT
Address:	224F4h-224F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_BCSUNIT
Address:	224F8h-224FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_BCSUNIT
Address:	224FCh-224FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_BCSUNIT
Address:	22010h-22013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_BCSUNIT
Address:	22014h-22017h
Name:	FORCE_TO_NONPRIV
Address:	22018h-2201Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_BCSUNIT
Address:	2201Ch-2201Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_BCSUNIT
Address:	221E0h-221E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_BCSUNIT
Address:	221E4h-221E7h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_BCSUNIT
Address:	221E8h-221EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_BCSUNIT
Address:	221ECh-221EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_BCSUNIT
Address:	1C04D0h-1C04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT0
Address:	1C04D4h-1C04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT0
Address:	1C04D8h-1C04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT0
Address:	1C04DCh-1C04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT0
Address:	1C04E0h-1C04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT0
Address:	1C04E4h-1C04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT0
Address:	1C04E8h-1C04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT0
Address:	1C04ECh-1C04EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT0
Address:	1C04F0h-1C04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT0

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1C04F4h-1C04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT0
Address:	1C04F8h-1C04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT0
Address:	1C04FCh-1C04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT0
Address:	1C0010h-1C0013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT0
Address:	1C0014h-1C0017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT0
Address:	1C0018h-1C001Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT0
Address:	1C001Ch-1C001Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT0
Address:	1C01E0h-1C01E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT0
Address:	1C01E4h-1C01E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT0
Address:	1C01E8h-1C01EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT0
Address:	1C01ECh-1C01EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT0
Address:	1C44D0h-1C44D3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT1
Address:	1C44D4h-1C44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT1
Address:	1C44D8h-1C44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT1
Address:	1C44DCh-1C44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT1
Address:	1C44E0h-1C44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT1
Address:	1C44E4h-1C44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT1
Address:	1C44E8h-1C44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT1
Address:	1C44ECh-1C44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT1
Address:	1C44F0h-1C44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT1
Address:	1C44F4h-1C44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT1
Address:	1C44F8h-1C44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT1
Address:	1C44FCh-1C44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT1
Address:	1C4010h-1C4013h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT1
Address:	1C4014h-1C4017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT1
Address:	1C4018h-1C401Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT1
Address:	1C401Ch-1C401Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT1
Address:	1C41E0h-1C41E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT1
Address:	1C41E4h-1C41E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT1
Address:	1C41E8h-1C41EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT1
Address:	1C41ECh-1C41EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT1
Address:	1C84D0h-1C84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT0
Address:	1C84D4h-1C84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT0
Address:	1C84D8h-1C84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT0
Address:	1C84DCh-1C84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT0

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1C84E0h-1C84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT0
Address:	1C84E4h-1C84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT0
Address:	1C84E8h-1C84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT0
Address:	1C84ECh-1C84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT0
Address:	1C84F0h-1C84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT0
Address:	1C84F4h-1C84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT0
Address:	1C84F8h-1C84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT0
Address:	1C84FCh-1C84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT0
Address:	1C8010h-1C8013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VECSUNIT0
Address:	1C8014h-1C8017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VECSUNIT0
Address:	1C8018h-1C801Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VECSUNIT0
Address:	1C801Ch-1C801Fh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_15_VECSUNIT0
Address:	1C81E0h-1C81E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VECSUNIT0
Address:	1C81E4h-1C81E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VECSUNIT0
Address:	1C81E8h-1C81EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VECSUNIT0
Address:	1C81ECh-1C81EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VECSUNIT0
Address:	1D04D0h-1D04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT2
Address:	1D04D4h-1D04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT2
Address:	1D04D8h-1D04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT2
Address:	1D04DCh-1D04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT2
Address:	1D04E0h-1D04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT2
Address:	1D04E4h-1D04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT2
Address:	1D04E8h-1D04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT2
Address:	1D04ECh-1D04EFh

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT2
Address:	1D04F0h-1D04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT2
Address:	1D04F4h-1D04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT2
Address:	1D04F8h-1D04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT2
Address:	1D04FCh-1D04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT2
Address:	1D0010h-1D0013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT2
Address:	1D0014h-1D0017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT2
Address:	1D0018h-1D001Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT2
Address:	1D001Ch-1D001Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT2
Address:	1D01E0h-1D01E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT2
Address:	1D01E4h-1D01E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT2
Address:	1D01E8h-1D01EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT2

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1D01ECh-1D01EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT2
Address:	1D44D0h-1D44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT3
Address:	1D44D4h-1D44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT3
Address:	1D44D8h-1D44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT3
Address:	1D44DCh-1D44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT3
Address:	1D44E0h-1D44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT3
Address:	1D44E4h-1D44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT3
Address:	1D44E8h-1D44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT3
Address:	1D44ECh-1D44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT3
Address:	1D44F0h-1D44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT3
Address:	1D44F4h-1D44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT3
Address:	1D44F8h-1D44FBh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT3
Address:	1D44FCh-1D44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT3
Address:	1D4010h-1D4013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT3
Address:	1D4014h-1D4017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT3
Address:	1D4018h-1D401Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT3
Address:	1D401Ch-1D401Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT3
Address:	1D41E0h-1D41E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT3
Address:	1D41E4h-1D41E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT3
Address:	1D41E8h-1D41EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT3
Address:	1D41ECh-1D41EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT3
Address:	1D84D0h-1D84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT1
Address:	1D84D4h-1D84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT1
Address:	1D84D8h-1D84DBh

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT1
Address:	1D84DCh-1D84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT1
Address:	1D84E0h-1D84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT1
Address:	1D84E4h-1D84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT1
Address:	1D84E8h-1D84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT1
Address:	1D84ECh-1D84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT1
Address:	1D84F0h-1D84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT1
Address:	1D84F4h-1D84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT1
Address:	1D84F8h-1D84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT1
Address:	1D84FCh-1D84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT1
Address:	1D8010h-1D8013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VECSUNIT1
Address:	1D8014h-1D8017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VECSUNIT1

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1D8018h-1D801Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VECSUNIT1
Address:	1D801Ch-1D801Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VECSUNIT1
Address:	1D81E0h-1D81E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VECSUNIT1
Address:	1D81E4h-1D81E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VECSUNIT1
Address:	1D81E8h-1D81EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VECSUNIT1
Address:	1D81ECh-1D81EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VECSUNIT1
Address:	1E04D0h-1E04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT4
Address:	1E04D4h-1E04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT4
Address:	1E04D8h-1E04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT4
Address:	1E04DCh-1E04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT4
Address:	1E04E0h-1E04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT4
Address:	1E04E4h-1E04E7h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT4
Address:	1E04E8h-1E04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT4
Address:	1E04ECh-1E04EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT4
Address:	1E04F0h-1E04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT4
Address:	1E04F4h-1E04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT4
Address:	1E04F8h-1E04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT4
Address:	1E04FCh-1E04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT4
Address:	1E0010h-1E0013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT4
Address:	1E0014h-1E0017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT4
Address:	1E0018h-1E001Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT4
Address:	1E001Ch-1E001Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT4
Address:	1E01E0h-1E01E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT4
Address:	1E01E4h-1E01E7h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT4
Address:	1E01E8h-1E01EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT4
Address:	1E01ECh-1E01EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT4
Address:	1E44D0h-1E44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT5
Address:	1E44D4h-1E44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT5
Address:	1E44D8h-1E44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT5
Address:	1E44DCh-1E44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT5
Address:	1E44E0h-1E44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT5
Address:	1E44E4h-1E44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT5
Address:	1E44E8h-1E44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT5
Address:	1E44ECh-1E44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT5
Address:	1E44F0h-1E44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT5

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1E44F4h-1E44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT5
Address:	1E44F8h-1E44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT5
Address:	1E44FCh-1E44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT5
Address:	1E4010h-1E4013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT5
Address:	1E4014h-1E4017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT5
Address:	1E4018h-1E401Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT5
Address:	1E401Ch-1E401Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT5
Address:	1E41E0h-1E41E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT5
Address:	1E41E4h-1E41E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT5
Address:	1E41E8h-1E41EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT5
Address:	1E41ECh-1E41EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT5
Address:	1E84D0h-1E84D3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT2
Address:	1E84D4h-1E84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT2
Address:	1E84D8h-1E84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT2
Address:	1E84DCh-1E84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT2
Address:	1E84E0h-1E84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT2
Address:	1E84E4h-1E84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT2
Address:	1E84E8h-1E84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT2
Address:	1E84ECh-1E84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT2
Address:	1E84F0h-1E84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT2
Address:	1E84F4h-1E84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT2
Address:	1E84F8h-1E84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT2
Address:	1E84FCh-1E84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT2
Address:	1E8010h-1E8013h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VECSUNIT2
Address:	1E8014h-1E8017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VECSUNIT2
Address:	1E8018h-1E801Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VECSUNIT2
Address:	1E801Ch-1E801Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VECSUNIT2
Address:	1E81E0h-1E81E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VECSUNIT2
Address:	1E81E4h-1E81E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VECSUNIT2
Address:	1E81E8h-1E81EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VECSUNIT2
Address:	1E81ECh-1E81EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VECSUNIT2
Address:	1F04D0h-1F04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT6
Address:	1F04D4h-1F04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT6
Address:	1F04D8h-1F04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT6
Address:	1F04DCh-1F04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT6

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1F04E0h-1F04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT6
Address:	1F04E4h-1F04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT6
Address:	1F04E8h-1F04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT6
Address:	1F04ECh-1F04EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT6
Address:	1F04F0h-1F04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT6
Address:	1F04F4h-1F04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT6
Address:	1F04F8h-1F04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT6
Address:	1F04FCh-1F04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT6
Address:	1F0010h-1F0013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT6
Address:	1F0014h-1F0017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT6
Address:	1F0018h-1F001Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT6
Address:	1F001Ch-1F001Fh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT6
Address:	1F01E0h-1F01E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT6
Address:	1F01E4h-1F01E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT6
Address:	1F01E8h-1F01EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT6
Address:	1F01ECh-1F01EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT6
Address:	1F44D0h-1F44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT7
Address:	1F44D4h-1F44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT7
Address:	1F44D8h-1F44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT7
Address:	1F44DCh-1F44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT7
Address:	1F44E0h-1F44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT7
Address:	1F44E4h-1F44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT7
Address:	1F44E8h-1F44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT7
Address:	1F44ECh-1F44EFh

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT7
Address:	1F44F0h-1F44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT7
Address:	1F44F4h-1F44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT7
Address:	1F44F8h-1F44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT7
Address:	1F44FCh-1F44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT7
Address:	1F4010h-1F4013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VCSUNIT7
Address:	1F4014h-1F4017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VCSUNIT7
Address:	1F4018h-1F401Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VCSUNIT7
Address:	1F401Ch-1F401Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VCSUNIT7
Address:	1F41E0h-1F41E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VCSUNIT7
Address:	1F41E4h-1F41E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VCSUNIT7
Address:	1F41E8h-1F41EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VCSUNIT7

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1F41ECh-1F41EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VCSUNIT7
Address:	1F84D0h-1F84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT3
Address:	1F84D4h-1F84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT3
Address:	1F84D8h-1F84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT3
Address:	1F84DCh-1F84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT3
Address:	1F84E0h-1F84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT3
Address:	1F84E4h-1F84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT3
Address:	1F84E8h-1F84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT3
Address:	1F84ECh-1F84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT3
Address:	1F84F0h-1F84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT3
Address:	1F84F4h-1F84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT3
Address:	1F84F8h-1F84FBh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT3
Address:	1F84FCh-1F84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT3
Address:	1F8010h-1F8013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_VECSUNIT3
Address:	1F8014h-1F8017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_VECSUNIT3
Address:	1F8018h-1F801Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_VECSUNIT3
Address:	1F801Ch-1F801Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_VECSUNIT3
Address:	1F81E0h-1F81E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_VECSUNIT3
Address:	1F81E4h-1F81E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_VECSUNIT3
Address:	1F81E8h-1F81EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_VECSUNIT3
Address:	1F81ECh-1F81EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_VECSUNIT3
Address:	1A4D0h-1A4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_CCSUNIT0
Address:	1A4D4h-1A4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_CCSUNIT0
Address:	1A4D8h-1A4DBh

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_CCSUNIT0
Address:	1A4DCh-1A4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_CCSUNIT0
Address:	1A4E0h-1A4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_CCSUNIT0
Address:	1A4E4h-1A4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_CCSUNIT0
Address:	1A4E8h-1A4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_CCSUNIT0
Address:	1A4ECh-1A4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_CCSUNIT0
Address:	1A4F0h-1A4F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_CCSUNIT0
Address:	1A4F4h-1A4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_CCSUNIT0
Address:	1A4F8h-1A4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_CCSUNIT0
Address:	1A4FCh-1A4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_CCSUNIT0
Address:	1A010h-1A013h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_12_CCSUNIT0
Address:	1A014h-1A017h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_13_CCSUNIT0

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

Address:	1A018h-1A01Bh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_14_CCSUNIT0

Address:	1A01Ch-1A01Fh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_15_CCSUNIT0

Address:	1A1E0h-1A1E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_16_CCSUNIT0

Address:	1A1E4h-1A1E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_17_CCSUNIT0

Address:	1A1E8h-1A1EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_18_CCSUNIT0

Address:	1A1ECh-1A1EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_19_CCSUNIT0

These registers are privilege registers and are not allowed to be written from non-privilege batch buffer. These are global registers and power context save/restored.

Workaround

This register must be programmed as non-privileged to give PPGTT batch buffer access: 3DPRIM_XP0(0x2690), 3DPRIM_XP1(0x2694) and 3DPRIM_XP2(0x2698).

DWord	Bit	Description
0	31	**Virtual Function Privilege Control** Value / Name / Description 0 / **Default]** / MMIO offset programmed in Non Privileged Register Address field will be treated as a non-privilege register by the commands executed from a non-privilege batch buffer. This register provides programmability to add new entries to the User Mode Non-Privileged Registers table mentioned in User Mode Privileged Commands section. 1 / / MMIO offset programmed in Non Privileged Register Address field will be treated as a non-privilege register by the commands executed from a privilege batch buffer or ring buffer of an virtual function. Not that this will not make the register offset as non-privileged for the commands executed from non-privileged batch buffer.
	30	**Denylist Enable**

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

If this bit is set, then the command stream will not allow access for a PPGTT batch buffer to this register or range. This takes the highest precedence so in the case the register is allow listed in a separate FORCE_TO_NONPRIV register, it will still be deny listed.

Value	Name
0	Allowlist **[Default]**
1	Denylist

29:28 **Access Selection**

This field allows the selection of whether read or write access are impacted. This allows for any permutation to deny list or allow list any combination of reads/writes. For Example, if Deny list Enable is set and the Access if for Reads only, then only Read access will be disallowed based on the Address in this register.

Value	Name
0h	Impacts both Read and Write Access **[Default]**
1h	Impacts only Read Access
2h	Impacts only Write Access
3h	Reserved

27:26 **Reserved**

Access:	RO
Format:	MBZ

25:2 **Non Privilege Register Address**

Format:	MmioAddress[25:2]

This field contains the MMIO offset of a register. MMIO offset programmed in this field will be treated as a non-privilege register by render command streamer while processing register writes from a non-privilege batch buffer. This register provides programmability is to extend the non-privilege register table mentioned in MI_BATCH_BUFFER_START command in render command streamer.

Value	Name
3800h	**[Default]**

1:0 **Offset Range**

This field specifies the range of registers to either be deny listed or allow listed. Note the Non-Privilege Register Address value should be at the same granularity of the Offset Range. The lower bits of the address will be ignored in the comparison as the definition only support base 2 address for range comparison.

Value	Name	Description
0h	Single Register **[Default]**	Offset for allowlist or denylist compare will be 25:2.
1h	Four Registers	Offset for allowlist or denylist compare will be 25:4.
2h	Sixteen Registers	Offset for allowlist or denylist compare will be 25:6.
3h	Sixty Four Registers	Offset for allowlist or denylist compare will be 25:8.

FUSE_STATUS

FUSE_STATUS

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	42000h-42003h
Name:	Fuse Status
ShortName:	FUSE_STATUS
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31	**Fuse Download Status** Access: RO This field indicates the status of fuse and strap download to the Display Engine. After fuse and strap download, fuses will be distributed within the Display Engine. Value: 0b – Not Done Value: 1b – Done
	30:28	**Reserved** Access: RO Format: MBZ
	27	**Fuse PG0 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #0. Value: 0b – Not Done Value: 1b – Done
	26	**Fuse PG1 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #1. Value: 0b – Not Done Value: 1b – Done
	25	**Fuse PG2 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #2. Value / Name

FUSE_STATUS

	0b	Not Done
	1b	Done

24 Fuse PG3 Distribution Status

Access:	RO

This field indicates the status of fuse distribution to power well #3.

Value	Name
0b	Not Done
1b	Done

23 Fuse PG4 Distribution Status

Access:	RO

This field indicates the status of fuse distribution to power well #4.

Value	Name
0b	Not Done
1b	Done

22 Fuse PG5 Distribution Status

Access:	RO

This field indicates the status of fuse distribution to power well #5.

Value	Name
0b	Not Done
1b	Done

21:16 Reserved

Access:	RO
Format:	MBZ

15:0 Reserved

Access:	RO
Format:	MBZ

GAC_GAM Arbitration Counters Register 0

ARB_GAC_GAM_REQCNTS0 - GAC_GAM Arbitration Counters Register 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	043A8h

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

GAC_GAM Arbitration Counters Register 1

ARB_GAC_GAM_REQCNTS1 - GAC_GAM Arbitration Counters Register 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	043ACh

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

GAC_GAM RO Arbitration Register 0

ARB_RO_GAC_GAM0 - GAC_GAM RO Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	043D0h	
DWord	**Bit**	**Description**
0	31:28	**Reserved** Access: RO Format: MBZ
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved** Access: RO Format: MBZ
	12	**Priority for entry 01**
	11:9	**Goto field for entry 01 when request vector is 11b**
	8:6	**Goto field for entry 01 when request vector is 10b**
	5:3	**Goto field for entry 01 when request vector is 01b**
	2:0	**Goto field for entry 01 when request vector is 00b**

GAC_GAM RO Arbitration Register 1

ARB_RO_GAC_GAM1 - GAC_GAM RO Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	043D4h	

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved** Access: RO Format: MBZ
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM RO Arbitration Register 2

ARB_RO_GAC_GAM2 - GAC_GAM RO Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	043D8h	

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved** Access: RO Format: MBZ
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM RO Arbitration Register 3

ARB_RO_GAC_GAM3 - GAC_GAM RO Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	043DCh	

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved** Access: RO Format: MBZ
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAF Config Register 0

GAFCFG0 - GAF Config Register 0

Register Space:	MMIO: 0/2/0
Access:	R/W Lock
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0D800h

DWord	Bit	Description
0	31	**gafsrdunit reserved** Default Value: 0b
	30	**Extra 4 slots addition to stopping distance** 0b **[Default]** 1b
	29	**Multi Slice Fuse enable** 0b **[Default]** 1b
	28	**TSG Double min alloc** 0b **[Default]** 1b
	27	**SF Double min alloc** 0b **[Default]** 1b
	26	**CL2 Double min alloc** 0b **[Default]** 1b
	25	**CL1 Double min alloc** 0b **[Default]** 1b

GAFCFG0 - GAF Config Register 0

24 **CL Double min alloc**

Value	Name
0b	**[Default]**
1b	

23 **SOL Double min alloc**

Value	Name
0b	**[Default]**
1b	

22 **GS Double min alloc**

Value	Name
0b	**[Default]**
1b	

21 **TE Double min alloc**

Value	Name
0b	**[Default]**
1b	

20:18 **CL max alloc programming**

Value	Name	Description
000b		Default(64)
001b		56
010b	**[Default]**	48
011b		40
100b		32
101b		24
110b		16
111b		Reserved

17:15 **SOL max alloc programming**

Value	Name	Description
000b		Default(64)
001b		56
010b	**[Default]**	48
011b		40
100b		32
101b		24
110b		16
111b		Reserved

GAFCFG0 - GAF Config Register 0

14:12 **GS max alloc programming**

Value	Name	Description
000b		Default(64)
001b		56
010b	**[Default]**	48
011b		40
100b		32
101b		24
110b		16
111b		Reserved

11:9 **TE max alloc programming**

Value	Name	Description
000b		Default(64)
001b		56
010b	**[Default]**	48
011b		40
100b		32
101b		24
110b		16
111b		Reserved

8:7 **TSG Low priority threshold programming**

Value	Name	Description
00b	**[Default]**	Default Low Priority Threshold
01b		Max Alloc/4
10b		Max Alloc/2
11b		Max Alloc

6:5 **SOL Low priority threshold programming**

Value	Name	Description
00b	**[Default]**	Default Low Priority Threshold
01b		Max Alloc/4
10b		Max Alloc/2
11b		Max Alloc

4:3 **GS Low priority threshold programming**

Value	Name	Description
00b	**[Default]**	Default Low Priority Threshold
01b		Max Alloc/4

GAFCFG0 - GAF Config Register 0

	10b	Max Alloc/2
	11b	Max Alloc

2:1 TE Low priority threshold programming

Value	Name	Description
00b	**[Default]**	Default Low Priority Threshold
01b		Max Alloc/4
10b		Max Alloc/2
11b		Max Alloc

0 GAFS data return policy

Value	Name
0b	**[Default]**
1b	

GAF Config Register 1

GAFCFG1 - GAF Config Register 1

Register Space: MMIO: 0/2/0
Access: R/W Lock
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0D804h

DWord	Bit	Description
0	31:26	**gafarbunit reserved** Value: 000000b **[Default]**; [0,63]
	25:13	**gafswrunit reserved** Value: 0000h **[Default]**; [0,8191]
	12:11	**sarbunit reserved** Value: 0h **[Default]**; [0,3]
	10	**sarb overfetch cache disable** Value: 0b **[Default]**; 1b
	9:7	**gafdunit reserved** Value: 000b **[Default]**; [0,7]
	6	**ebb signal bypass control** Used to control the bypass ebb signal in gafdunit Value: 0b **[Default]**; 1b
	5:2	**gafmunit reserved** Value: 0000b **[Default]**

GAFCFG1 - GAF Config Register 1

		[0,15]
	1	**POSH nonPOSH priority** Value: 0b — **[Default]** Value: 1b
	0	**VF SOL priority** Value: 0b — **[Default]** Value: 1b

GAMMA_MODE

GAMMA_MODE

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank

Address:	4A480h-4A483h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_A
Reset:	soft

Address:	4AC80h-4AC83h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_B
Reset:	soft

Address:	4B480h-4B483h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_C
Reset:	soft

Address:	4BC80h-4BC83h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_D
Reset:	soft

DWord	Bit	Description
0	31	**Pre CSC Gamma Enable** This bit enables the pipe pre color space conversion gamma. Restriction : This bit must not be set when any of the individual plane 'Pipe CSC Enable' bit is set in PLANE_COLOR_CTL register. Value / Name: 1b – Enable 0b – Disable
	30	**Post CSC Gamma Enable** This bit enables the pipe post color space conversion gamma. Restriction : This bit must not be set when any of the individual plane 'Pipe Gamma Enable' bit is set in PLANE_COLOR_CTL register.

GAMMA_MODE

Value	Name
1b	Enable
0b	Disable

29	**Allow Double Buffer Update Disable**
	Access: R/W
	This field controls whether double buffer updates are allowed to be disabled for the Gamma registers that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled.

Value	Name
0b	Not Allowed
1b	Allowed **[Default]**

28:25	**Reserved**
	Access: RO
	Format: MBZ
24:16	**Reserved**
	Access: RO
	Format: MBZ
15	**Reserved**
14:5	**Reserved**
	Access: RO
	Format: MBZ
4:3	**Reserved**
	Access: RO
	Format: MBZ
2	**Reserved**
	Access: RO
	Format: MBZ
1:0	**Gamma Mode**
	This field selects which mode the pipe palette/gamma correction logic works in. Other gamma units, such as in the planes, are unaffected by these bits.
	This field applies to post csc gamma. Pre csc gamma mode is fixed and not configurable.

Value	Name	Description
00b	8 bit	8-bit Legacy Palette Mode
01b	10 bit	10-bit Precision Palette Mode
10b	12 bit	12-bit Interpolated Gamma Mode
11b	12 bit Multi Segment	12-bit Multi-segmented Gamma Mode

Gang Timer Register

FF_MODE2 - Gang Timer Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	06604h-06607h
Name:	Ganged Timer Register
ShortName:	FF_MODE2_SVGUNIT
Address:	17604h-17607h
Name:	Ganged Timer Register
ShortName:	FF_MODE2_SVGRUNIT

This register is used to program the FF shader timers.

DWord	Bit	Description
0	31:24	**GS timer value** Format: U8 The GS timer value will be a multiple of 32 clocks. The GS timer value of 0 disables the GS timer. If the number of clocks between ganged threads reaches the GS timer value, the GS will dispatch however many threads it currently has ganged.
	23:16	**TDS timer value** Format: U8 The TDS timer value will be a multiple of 32 clocks. The TDS timer value of 0 disables the TDS timer. If the number of clocks between ganged threads reaches the TDS timer value, the TDS will dispatch however many threads it currently has ganged. **Programming Notes** For best performance, a value of 4 should be programmed.
	15:8	**HS timer value** Format: U8 The HS timer value will be a multiple of 32 clocks. The HS timer value of 0 disables the HS timer. If the number of clocks between ganged threads reaches the HS timer value, the HS will dispatch however many threads it currently has ganged.

FF_MODE2 - Gang Timer Register		
	7:0	**VS timer value** Format: U8 The VS timer value will be a multiple of 32 clocks. The VS timer value of 0 disables the VS timer. If the number of clocks between ganged threads reaches the VS timer value, the VS will dispatch however many threads it currently has ganged.

Gated Clock Counter for DFR Testability

SAMPLER_DFR_GATED_COUNT - Gated Clock Counter for DFR Testability

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E14Ch

For testability of DFR feature

DWord	Bit	Description
0	31:0	**Counter Bits** Format: U32 Count of edge-skipped sampler clocks

General Purpose Register

CS_GPR - General Purpose Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	1024
_Custom_GTIReset:	DEV
Address:	02600h-0267Fh
Name:	General Purpose Register
ShortName:	CS_GPR_RCSUNIT
Address:	18600h-1867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_POCSUNIT
Address:	22600h-2267Fh
Name:	General Purpose Register
ShortName:	CS_GPR_BCSUNIT
Address:	1C0600h-1C067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT0
Address:	1C4600h-1C467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT1
Address:	1C8600h-1C867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT0
Address:	1D0600h-1D067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT2
Address:	1D4600h-1D467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT3
Address:	1D8600h-1D867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT1
Address:	1E0600h-1E067Fh
Name:	General Purpose Register

CS_GPR - General Purpose Register

ShortName:	CS_GPR_VCSUNIT4
Address:	1E4600h-1E467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT5
Address:	1E8600h-1E867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT2
Address:	1F0600h-1F067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT6
Address:	1F4600h-1F467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT7
Address:	1F8600h-1F867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT3
Address:	1A600h-1A67Fh
Name:	General Purpose Register
ShortName:	CS_GPR_CCSUNIT0

This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.

GPR Index	MMIO Offset
R_0	0x2600
R_1	0x2608
R_2	0x2610
R_3	0x2618
R_4	0x2620
R_5	0x2628
R_6	0x2630
R_7	0x2638
R_8	0x2640
R_9	0x2648
R_10	0x2650
R_11	0x2658
R_12	0x2660

CS_GPR - General Purpose Register

R_13	0x2668
R_14	0x2670
R_15	0x2678

DWord	Bit	Description
0..1	63:32	**CS_GPR_DATA1** Source: CommandStreamer
	31:0	**CS_GPR_DATA0** Source: CommandStreamer
2..3	63:32	**CS_GPR_DATA3** Source: CommandStreamer
	31:0	**CS_GPR_DATA2** Source: CommandStreamer
4..5	63:32	**CS_GPR_DATA5** Source: CommandStreamer
	31:0	**CS_GPR_DATA4** Source: CommandStreamer
6..7	63:32	**CS_GPR_DATA7** Source: CommandStreamer
	31:0	**CS_GPR_DATA6** Source: CommandStreamer
8..9	63:32	**CS_GPR_DATA9** Source: CommandStreamer
	31:0	**CS_GPR_DATA8** Source: CommandStreamer
10..11	63:32	**CS_GPR_DATA11** Source: CommandStreamer
	31:0	**CS_GPR_DATA10** Source: CommandStreamer
12..13	63:32	**CS_GPR_DATA13** Source: CommandStreamer
	31:0	**CS_GPR_DATA12** Source: CommandStreamer
14..15	63:32	**CS_GPR_DATA15** Source: CommandStreamer
	31:0	**CS_GPR_DATA14**

CS_GPR - General Purpose Register		
		Source: CommandStreamer
16..17	63:32	**CS_GPR_DATA17** Source: CommandStreamer
	31:0	**CS_GPR_DATA16** Source: CommandStreamer
18..19	63:32	**CS_GPR_DATA19** Source: CommandStreamer
	31:0	**CS_GPR_DATA18** Source: CommandStreamer
20..21	63:32	**CS_GPR_DATA21** Source: CommandStreamer
	31:0	**CS_GPR_DATA20** Source: CommandStreamer
22..23	63:32	**CS_GPR_DATA23** Source: CommandStreamer
	31:0	**CS_GPR_DATA22** Source: CommandStreamer
24..25	63:32	**CS_GPR_DATA25** Source: CommandStreamer
	31:0	**CS_GPR_DATA24** Source: CommandStreamer
26..27	63:32	**CS_GPR_DATA27** Source: CommandStreamer
	31:0	**CS_GPR_DATA26** Source: CommandStreamer
28..29	63:32	**CS_GPR_DATA29** Source: CommandStreamer
	31:0	**CS_GPR_DATA28** Source: CommandStreamer
30..31	63:32	**CS_GPR_DATA31** Source: CommandStreamer
	31:0	**CS_GPR_DATA30** Source: CommandStreamer

GFX_FLSH_CNT

GFX_FLSH_CNT - GFX_FLSH_CNT

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	101008h

Used to flush Gunit TLB

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**GfxFlshCntl** Default Value: 0b Access: WO _Custom_GTIReset: BUS Access type of this register is WO. A write to this bit flushes the Gfx TLB in GUNIT. The data associated with the write is discarded and a read return all 0s.

GFX_VTDBAR_LSB

GFXVTDBAR_LSB_0_2_0_PCI - GFX_VTDBAR_LSB

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	000C8h

This is the base address for the Graphics VTD configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN.
None of the bits in this register are writeable in Intel TXT mode. This enforcement is based on SAI policy registers.
BIOS programs this register, after which the register cannot be altered.

DWord	Bit	Description
0	31:12	**GFXVTDBAR** Default Value: 000000h Access: R/W _Custom_GTIReset: BUS This field corresponds to bits 31 to 12 of the base address GFX-VTD configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set. All the Bits in this register are included in an SAI policy group for Intel TXT mode purposes.
	11:2	**Reserved** Access: RO Format: MBZ
	1	**SPARE** Default Value: 000h Access: R/W _Custom_GTIReset: BUS This was a lock bit prior.
	0	**GFXVTDBAREN** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0: GFX-VTBAR is disabled and does not claim any memory. 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled.

GFXBDF

GFXBDF - GFXBDF

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	10107Ch

If the associated hardware strap is enabled, hardware will update this register based on the received IOSF P Bus / Device value from Type 0 configuration cycles (per PCIe spec). Also hardware will be updating this register, Punit needs the ability to save/restore the register contents for relevant PKGC state flows and/or S0i3 flows. Therefore, this register will be a RW-able by software and write-able by hardware.

DWord	Bit	Description
0	31:24	**BUS** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS This field specifies the PCI bus number of theGfx device.
	23:19	**DEVICE** Access: R/W _Custom_GTIReset: BUS This field specifies the PCI device number of theGfx device. Value: 00010b — Name: **[Default]**
	18:16	**FUNCTION** Default Value: 000b Access: RO _Custom_GTIReset: BUS This field specifies the PCI function number of theGfx device.
	15:1	**Reserved** Access: RO Format: MBZ
	0	**HWUPDATEDISABLE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0 : Hardware updates Bus/Device value based on received Type 0 configuration cycles. 1 : Disable hardware updates based on received hardware cycles (even if strapped to allow updates).

GGTT Pinned Range Base Register

GGTT_PINNED_BASE - GGTT Pinned Range Base Register

Register Space: MMIO: 0/2/0

Size (in bits): 32

GGTT Pinned Range Base register

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**Pinned Range Base** Default Value: 00000h Access: R/W _Custom_GTIReset: DEV GGTT Entry that represents the base of the Pinned Range. This corresponds to bits 31:12 of the Global Virtual address of the memory page that corresponds to that entry. This register is a shadow of the primary register in Gunit, and is updated automatically by Gunit HW via IOSF-SB.

GGTT Pinned Range Limit Register

GGTT_PINNED_LIMIT - GGTT Pinned Range Limit Register

Register Space: MMIO: 0/2/0

Size (in bits): 32

GGTT Pinned Range Limit register

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**Pinned Range Limit** Default Value: 00000h Access: R/W _Custom_GTIReset: DEV GGTT Entry that represents the limit(last entry) of the Pinned Range. This corresponds to bits 31:12 of the Global Virtual address of the memory page that corresponds to that entry. This register is a shadow of the primary register in Gunit, and is updated automatically by Gunit HW via IOSF-SB.

Global MicroController Status

GUC_STATUS - Global MicroController Status

Register Space: MMIO: 0/2/0
Access: RO
Size (in bits): 32

Programming Notes
This register is saved in the power context.
Only write by MinuteIA is allowed to this register.
Host writes to this register have no effect (they are dropped).

DWord	Bit	Description
0	31:30	**Authentication Status** BootROM code shall write a 1 to bit 31, if the uOS was authenticated successfully. BootROM code shall write a 1 to bit 30, if the uOS authentication failed. **Value / Name / Description** 1h / Fail / The uOS authentication failed. 2h / Success / The uOS was authenticated successfully. **Programming Notes** Set Once Bits (Once written, they cannot be overwritten) If bit 30 is set, DMA HW will skip trying to load a uOS into the SRAM thereby preventing the MinuteIA from execution.
	29:24	**uApp Status** This field is software-defined.
	23:16	**Reserved**
	15:8	**uKernel/uOS Status** This field is software-defined.
	7:1	**Boot ROM Code Status** This field is software-defined.
	0	**MinIA Is In Reset** '1' indicates that MinIA is in reset.

Global System Interrupt Routine

EU_GLOBAL_SIP - Global System Interrupt Routine		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0E42Ch	

DWord	Bit	Description
0	31:3	**Global SIP** Format: GraphicsAddress[31:3] Specifies the base address for System Interrupt Routine that over-rides the SIP set by the state (STATE_SIP).
	2:1	**Reserved** Format: PBC
	0	**Global SIP Enable** The bit specifies if the System Routine starts from the Global SIP provided by the DW OR the SIP provided by the state (STATE_SIP) Value: 0 — SIP used is from STATE_EIP Value: 1 — SIP used is from MMIO register

GMCH Graphics Control

GGC - GMCH Graphics Control

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	108040h

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**GMS** Default Value: 05h Access: R/W _Custom_GTIReset: BUS This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB

21h - 2Fh: Reserved
30h:1536MB
31h - 3Fh: Reserved
40h: 2048MB
41h - EFh: Reserved
F0h: 4MB
F1h: 8MB
F2h: 12MB
F3h: 16MB
F4h: 20MB
F5h: 24MB
F6h: 28MB
F7h: 32MB
F8h: 36MB
F9h: 40MB
FAh: 44MB
FBh: 48MB
FCh: 52MB
FDh: 56MB
FEh: 60MB
FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.

7:6 **GGMS**

Access:	R/W
_Custom_GTIReset:	BUS

This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
Hardware functionality in case of programming this value to Reserved is not guaranteed.
0x0:No Preallocated Memory
0x1:2MB of Preallocated Memory
0x2:4MB of Preallocated Memory
0x3:8MB of Preallocated Memory

Value	Name
00b	**[Default]**

5:3 **Reserved**

Access:	RO
Format:	MBZ

2 **VAMEN**

Default Value:	0b
Access:	R/W
_Custom_GTIReset:	BUS

GGC - GMCH Graphics Control

	1	**IVD** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory.
	0	**SPARE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Note: This bit was maintained as a placeholder for compatibility. Prior, it locked the register.

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	02500h-02503h
Name:	GPGPU Dispatch Dimension X
ShortName:	GPGPU_DISPATCHDIMX_RCSUNIT_BE_COMPUTE

Address:	1A500h-1A503h
Name:	GPGPU Dispatch Dimension X
ShortName:	GPGPU_DISPATCHDIMX_CCSUNIT_BE_COMPUTE0

DWord	Bit	Description
0	31:0	**Dispatch Dimension X** Format: U32 The number of thread groups to be dispatched in the X dimension (max x + 1). Value: 0, FFFFFFFFh; Name:

GPGPU Dispatch Dimension Y

GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	02504h-02507h
Name:	GPGPU Dispatch Dimension Y
ShortName:	GPGPU_DISPATCHDIMY_RCSUNIT_BE_COMPUTE

Address:	1A504h-1A507h
Name:	GPGPU Dispatch Dimension Y
ShortName:	GPGPU_DISPATCHDIMY_CCSUNIT_BE_COMPUTE0

DWord	Bit	Description
0	31:0	**Dispatch Dimension Y** Format: U32 The number of thread groups to be dispatched in the Y dimension (max y + 1 Value: 0, FFFFFFFFh; Name:

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch Dimension Z	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02508h-0250Bh
Name:	GPGPU Dispatch Dimension Z
ShortName:	GPGPU_DISPATCHDIMZ_RCSUNIT_BE_COMPUTE
Address:	1A508h-1A50Bh
Name:	GPGPU Dispatch Dimension Z
ShortName:	GPGPU_DISPATCHDIMZ_CCSUNIT_BE_COMPUTE0

DWord	Bit	Description
0	31:0	**Dispatch Dimension Z** Format: U32 The number of thread groups to be dispatched in the Zdimension (max Z + 1) Value: 0, FFFFFFFFh; Name:

GP Thread Time

GP_THREAD_TIME - GP Thread Time	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	053C4h

Reading this register returns the cumulative GP context execution time. This register uses the same clock frequency as CTX_TIMESTAMP, but differs from CTX_TIMESTAMP because it excludes the execution time during preemption save or restore. This register gets context save/restored on a context switch.
The granularity of this toggle is at the rate of the bit 3 in the "Reported Timestamp Count" register(0x2358). The toggle will be 8 times slower that "Reported Timestamp Count". The granularity of the time stamp base unit for "Reported Timestamp Count" is defined in the Timestamp Bases subsection in Power Management chapter.

DWord	Bit	Description
0	31:0	**Timestamp Value** Access: RO Number of clock ticks that the context has run.

Graphics Device Reset Control

GDRST - Graphics Device Reset Control

Register Space:	MMIO: 0/2/0
Size (in bits):	32
CrashLogSaved:	true
CrashLogVisibility:	cspec
Address:	0941Ch

Graphics Device Reset Control Registers

DWord	Bit	Description
0	31:24	**Reserved**
	23:22	**Reserved**
	21	**Reserved**
	20	**Initiate Graphics SFC3 soft reset** Access: R/W Set _Custom_GTIReset: BUS Graphics SFC 3 Soft-Reset Control: '1' : Initiate a graphics SFC1 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP hardware can reset this bit. Note: This is a non-posted register.
	19	**Initiate Graphics SFC2 soft reset** Access: R/W Set _Custom_GTIReset: BUS Graphics SFC 1 Soft-Reset Control: '1' : Initiate a graphics SFC1 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP hardware can reset this bit. Note: This is a non-posted register.
	18	**Initiate Graphics SFC1 soft reset** Access: R/W Set _Custom_GTIReset: BUS Graphics SFC 1 Soft-Reset Control: '1' : Initiate a graphics SFC1 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP hardware can reset this bit. Note: This is a non-posted register.

GDRST - Graphics Device Reset Control

	17	**Initiate Graphics SFC0 soft reset** Access: R/W Set _Custom_GTIReset: BUS Graphics SFC 0 Soft-Reset Control: '1' : Initiate a graphics SFC0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP hardware can reset this bit. Note: This is a non-posted register.
	16	**Initiate Graphics Vebox3 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	15	**Initiate Graphics Vebox2 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	14	**Initiate Graphics Vebox1 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	13	**Initiate Graphics Vebox0 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete

		'0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	12	**Initiate Graphics Media 7 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	11	**Initiate Graphics Media 6 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	10	**Initiate Graphics Media 5 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	9	**Initiate Graphics Media 4 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	8	**Initiate Graphics Media 3 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS

GDRST - Graphics Device Reset Control

		Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	7	**Initiate Graphics Media 2 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	6	**Initiate Graphics Media 1 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	5	**Initiate Graphics Media 0 Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	4	**Reserved** Access: RO Format: MBZ
	3	**Initiate Graphics GUC soft reset** Access: R/W Set _Custom_GTIReset: BUS Graphics GUC Soft-Reset Control: '1' : Initiate a graphics GUC domain reset(cgucrst_b). - Cleared by CP once the reset is complete

GDRST - Graphics Device Reset Control

		'0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	2	**Initiate Graphics Blitter Soft Reset** Access: R/W Set _Custom_GTIReset: BUS **Description** Graphics Blitter Soft-Reset Control: '1' : Initiate a graphics blitter domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	1	**Initiate Graphics Render Soft Reset** Access: R/W Set _Custom_GTIReset: BUS **Description** Graphics Render Soft-Reset Control: '1' : Initiate a graphics render domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register. Note that both RenderEngine (hedaed by RenderCS) and ComputeEngine (headed by ComputeCS) are in Graphics Render Reset domain.
	0	**Initiate Graphics Full Soft Reset** Access: R/W Set _Custom_GTIReset: BUS Graphics Full Soft-Reset Control: '1' : Initiate a full graphics reset (i.e., graphics render, media, and blitter reset). - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.

Graphics Memory Range Address

GMADR_0_2_0_PCI - Graphics Memory Range Address

Register Space:	PCI: 0/2/0
Size (in bits):	64
Address:	00018h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

DWord	Bit	Description
0	63:32	**Memory Base Address** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [63:32].
	31	**4096 MB Address Mask** Default Value: 0b Access: R/W Lock _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1)
	30	**2048 MB Address Mask** Default Value: 0b Access: R/W Lock _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1)
	29	**1024 MB Address Mask** Default Value: 0b Access: R/W Lock _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1)
	28	**512MB Address Mask** Default Value: 0b Access: R/W Lock _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e.

GMADR_0_2_0_PCI - Graphics Memory Range Address

		MSAC.APSZ[1]=1)
	27	**256 MB Address Mask** Default Value: 0b Access: R/W Lock _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1)
	26:4	**Address Mask** Default Value: 00000000000000000000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s to indicate at least 128MB address range.
	3	**Prefetchable Memory** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1 to enable prefetching.
	2:1	**Memory Type** Default Value: 10b Access: RO _Custom_GTIReset: BUS Hardwired to 2h to indicate 64 bit base address.
	0	**Memory/IO Space** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate memory space.

Graphics Mode Register

GFX_MODE - Graphics Mode Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0229Ch-0229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_RCSUNIT
Address:	1829Ch-1829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_POCSUNIT
Address:	2229Ch-2229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_BCSUNIT
Address:	1C029Ch-1C029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT0
Address:	1C429Ch-1C429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT1
Address:	1C829Ch-1C829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT0
Address:	1D029Ch-1D029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT2
Address:	1D429Ch-1D429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT3
Address:	1D829Ch-1D829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT1
Address:	1E029Ch-1E029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT4

GFX_MODE - Graphics Mode Register

Address:	1E429Ch-1E429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT5

Address:	1E829Ch-1E829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT2

Address:	1F029Ch-1F029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT6

Address:	1F429Ch-1F429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT7

Address:	1F829Ch-1F829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT3

Address:	1A29Ch-1A29Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_CCSUNIT0

This register contains a control bit for the new execlist and 2-level PPGTT functions.

Programming Notes

"Privilege Check Disable" are the only programmable bits in GFX_MODE register for PositionCS, functionality for the rest of the bits is not supported by Position command streamer.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Reserved** Format: PBC
	14	**Reserved** Format: PBC
	13	**Reserved** Format: PBC
	12	**Reserved**

12 **Reserved**

Source:	RenderCS, BlitterCS, ComputeCS
Format:	PBC

11 **Virtual Function MMIO Read Access Control**

This bit controls the disabling and enabling of MMIO read access of an virtual function context running on an engine.

Value	Name	Description
1		A VF context running on an engine can do MMIO read access to other engines. Ex: VF context running on RenderCS can do MMIO read access to VideoCS.
0	**Default]**	A VF context running on an engine cant do MMIO read access to other engines. Ex: VF context running on RenderCS can't do MMIO read access to VideoCS.

10 **Prefetch Disable**

This field allows software to enable or disable pre-fetch mechanism for command buffers in hardware.

Value	Name	Description
0	**[Default]**	When reset pre-fetch of command buffers is enabled in hardware. However software can enable/disable pre-fetch functionality locally from within a command sequence using MI_ARB_CHK command on per context basis.
1		When set pre-fetch of command buffers is disabled in hardware.

9 **Per-Process GTT Enable**

Per-Process GTT Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes

This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.
Programming this bit doesn't enable or disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming this bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access.

GFX_MODE - Graphics Mode Register

8 — Reserved

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Format:	PBC

8 — Reserved

7 — 64Bit Virtual Addressing Enable

64Bit Virtual Addressing Enable

Value	Name	Description
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.

Programming Notes

This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Whether this field is set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.

6:5 — Reserved

4 — Reserved

3 — Disable Legacy Mode

This bit must be set to disable Legacy behavior to support features added for the current project.

When set the size of the CSB status FIFO is 12 deep.

Value	Name	Description
0h	Enable Legacy **[Default]**	Any features using this bit will be compatible with legacy drivers.
1h	Disable Legacy	HW will not be compatible with legacy drivers.

Programming Notes

A graphics reset is required prior to changing the value of this bit.

2 — Reserved

Format:	PBC

1 — MMIO Read Privilege Check Disable

Format:	Enable

This field when set, disables MMIO Read Privilege Violation checks on non-privileged batch buffers. When set Privileged MMIO read requests are allowed to be executed from non-privileged batch buffers.

GFX_MODE - Graphics Mode Register		
	0	**Privilege Check Disable** This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.

Graphics Primary Interrupt

GFX_MSTR_INTR - Graphics Primary Interrupt

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 190010h

Top level register that indicates interrupt from hardware.
Bits in this register are set interrupts are pending in the underlying PCU, display or GT interrupts

DWord	Bit	Description
0	31	**Primary Interrupt** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This is the primary control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device interrupt .
	30	**PCU** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS
	29	**GU_MISC** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS
	28:26	**Reserved** Access: RO Format: MBZ
	25:17	**Reserved** Access: RO Format: MBZ
	16	**Display** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS
	15:2	**Reserved** Access: RO Format: MBZ

GFX_MSTR_INTR - Graphics Primary Interrupt

	1	**GT DW1**
		Default Value: 0b
		Access: RO Variant
		_Custom_GTIReset: BUS
	0	**GT DW0**
		Default Value: 0b
		Access: RO Variant
		_Custom_GTIReset: BUS

Graphics System Event

GSE_0_2_0_PCI - Graphics System Event		
Register Space:	PCI: 0/2/0	
Size (in bits):	32	
Address:	000E4h	
This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.		
DWord	**Bit**	**Description**
0	31:24	**GSE Scratch Trigger 3** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS
	23:16	**GSE Scratch Trigger 2** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS
	15:8	**GSE Scratch Trigger 1** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS
	7:0	**GSE Scratch Trigger 0** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS

Graphics Translation Table Memory Mapped Range Address

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

Register Space:	PCI: 0/2/0
Size (in bits):	64
Address:	00010h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

DWord	Bit	Description
0	63:24	**Memory Base Address** Default Value: 0000000000h Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [63:24].
	23:4	**Address Mask** Default Value: 00000000000000000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s to indicate at least 16MB address range.
	3	**Prefetchable Memory** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to prevent prefetching.
	2:1	**Memory Type** Default Value: 10b Access: RO _Custom_GTIReset: BUS Hardwired to 2h to indicate 64 bit base address.

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

	0	**Memory/IO Space** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate memory space.

Graphics Virtual Primary Interrupt

GFX_VIRT_MSTR_INTR - Graphics Virtual Primary Interrupt

Register Space:	MMIO: 0/2/0
Size (in bits):	32

Address:	191010h
Name:	VF1_GFX_MSTR_INTR
ShortName:	VF1_GFX_MSTR_INTR

Address:	192010h
Name:	VF2_GFX_MSTR_INTR
ShortName:	VF2_GFX_MSTR_INTR

Address:	193010h
Name:	VF3_GFX_MSTR_INTR
ShortName:	VF3_GFX_MSTR_INTR

Address:	194010h
Name:	VF4_GFX_MSTR_INTR
ShortName:	VF4_GFX_MSTR_INTR

Address:	195010h
Name:	VF5_GFX_MSTR_INTR
ShortName:	VF5_GFX_MSTR_INTR

Address:	196010h
Name:	VF6_GFX_MSTR_INTR
ShortName:	VF6_GFX_MSTR_INTR

Address:	197010h
Name:	VF7_GFX_MSTR_INTR
ShortName:	VF7_GFX_MSTR_INTR

Top level register that indicates interrupt from hardware.
Bits in this register are set interrupts are pending in the underlying PCU, display or GT interrupts

DWord	Bit	Description
0	31	**Primary Interrupt** Access: R/W
	30	**PCU** Access: RO
	29:17	**Reserved** Access: RO Format: MBZ

GFX_VIRT_MSTR_INTR - Graphics Virtual Primary Interrupt

	16	**Display** Access: RO
	15:6	**Reserved** Access: RO Format: MBZ
	5:4	**Reserved** Access: RO Format: MBZ
	3:2	**Reserved** Access: RO Format: MBZ
	1	**GT DW1** Access: R/W
	0	**GT DW0** Access: R/W

GSCPowerGoodDelay

GSC_PG_DLY - GSCPowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	**Bit**	**Description**
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value

GS Invocation Counter

GS_INVOCATION_COUNT - GS Invocation Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02328h
Name:	GS Invocation Counter
ShortName:	GS_INVOCATION_COUNT

This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**GS Invocation Count UDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Invocation Count LDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GSI Power Good Delay

GSI_PG_DLY - GSI Power Good Delay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	**Bit**	**Description**
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value

GSMBASE

GSMBASE - GSMBASE

Register Space:	MMIO: 0/2/0
Size (in bits):	64
SOC_Consumer:	BIOS
Address:	108100h

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory. BIOS is now able to allocate Gfx Stolen Memory above the 4GB.

DWord	Bit	Description
0..1	63:32	**BGSM_MSB** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS This BitField contains bits 63 to 32 of the base address of stolen DRAM memory.
	31:20	**BGSM_LSB** Default Value: 001h Access: R/W _Custom_GTIReset: BUS This BitField contains bits 31 to 20 of the base address of stolen DRAM memory.
	19:1	**Reserved** Access: RO Format: MBZ
	0	**SPARE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This was a lock bit prior.

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02330h
Name:	GS Primitives Counter
ShortName:	GS_PRIMITIVES_COUNT

This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**GS Primitives Count UDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Primitives Count LDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GT_FLUSH_BCLD_ACK

GT_FLUSH_BCLD_ACK - GT_FLUSH_BCLD_ACK

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	030C0h

GT writes a '1 to this bit to acknowledge PRMRR range registers are loaded into GT.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**ACK** Default Value: 0b Access: R/W _Custom_GTIReset: BUS GT Boot Context Load Ack

GT_RELOAD_FLUSH

GT_RELOAD_FLUSH - GT_RELOAD_FLUSH

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	030B0h

Ucode writes a '1 to bits 0 which triggers GT to flush and re-load PRMRR range registers.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**BCLD_REQ** Default Value: 0b Access: R/W _Custom_GTIReset: BUS GT Boot Context Load Request. Write to this bit will initiate Mcheck Complete Routine (PPPE flow).

GTACK

GTACK - GTACK

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	120004h

This register is written to by GT for various device 2 sequencer flows.

DWord	Bit	Description
0	31:5	**Reserved** Access: RO Format: MBZ
	4	**RTPACK** Default Value: 0h Access: R/W _Custom_GTIReset: BUS GT indicates that the set root table pointer flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	3	**DESCRACK** Default Value: 0h Access: R/W _Custom_GTIReset: BUS GT indicates that the generic descriptor flow is complete from its point of view by writing a 1b to this field Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	2	**VTDACK** Default Value: 0h Access: R/W _Custom_GTIReset: BUS GT indicates that the Translation Enable/Disable or IOTLB Invalidation flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	1	**DPRACK** Default Value: 0h Access: R/W _Custom_GTIReset: BUS GT indicates that DPR Update flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.

GTACK - GTACK

	0	**PMRACK** Default Value: 0h Access: R/W _Custom_GTIReset: BUS GT indicates that PMR Enable/Disable flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.

GTC_CTL

GTC_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	67000h-67003h
Name:	Global Time Code Control
ShortName:	GTC_CTL
Reset:	soft

DWord	Bit	Description
0	31	**GTC Function Enable** This bit enables the GTC counter. Value: 0b = Disable; 1b = Enable Restriction: Enable this bit before enabling GTC controller operation on a port with a GTC capable device.
	30:29	**Reserved** Access: RO Format: MBZ
	28:13	**Reserved**
	12:1	**Reserved** Access: RO Format: MBZ
	0	**Reserved**

GTC_DDA_M

GTC_DDA_M		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	67010h-67013h	
Name:	Global Time Code DDA M	
ShortName:	GTC_DDA_M	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
	23:0	**GTC DDA M** This field is used to program the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: 1/(accumulator increment) = Reference Clock * DDA_M / DDA_N

GTC_DDA_N

GTC_DDA_N		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	67014h-67017h	
Name:	Global Time Code DDA N	
ShortName:	GTC_DDA_N	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:24	**GTC Accum Inc** Format: U7.1 This field is the GTC accumulator increment value in nanoseconds each time the DDA trips. It is programmed in 7.1 fixed point binary format where the LSB represents 0.5ns increment.
	23:0	**GTC DDA N** This field is used to program the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: 1/(accumulator increment) = Reference Clock * DDA_M / DDA_N

GTC_IIR

GTC_IIR	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	67058h-6705Bh
Name:	Global Time Code Interrupt Identity
ShortName:	GTC_IIR
Reset:	soft

See the GTC interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the GTC interrupt bits which are unmasked by the GTC_IMR.Bits set in this register will propagate to the GTC interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

GTC_IMR

GTC_IMR	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	67054h-67057h
Name:	Global Time Code Interrupt Mask
ShortName:	GTC_IMR
Reset:	soft

See the GTC interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which GTC events are reported int the GTC IIR.

Value	Name
0b	Not Masked
1b	Masked
FFFFFFFFh	All interrupts masked **[Default]**

GTC_LIVE

GTC_LIVE		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	67020h-67023h	
Name:	Global Time Code Live	
ShortName:	GTC_LIVE	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GTC Live Value** This field contains the live current value of the GTC. It is inactive when the GTC controller function is disabled. This register also samples and holds the live GTC value following a Audio Time Capture (ATC) event until software reads this register. A subsequent read of this register will reflect the live value.

GTC_PORT_CTL

GTC_PORT_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64370h-64373h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_USBC1
Reset:	soft
Address:	64470h-64473h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_USBC2
Reset:	soft
Address:	64570h-64573h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_USBC3
Reset:	soft
Address:	64670h-64673h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_USBC4
Reset:	soft
Address:	64770h-64773h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_USBC5
Reset:	soft
Address:	64870h-64873h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_USBC6
Reset:	soft
Address:	64070h-64073h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_A
Reset:	soft
Address:	64170h-64173h
Name:	DDI GTC Port Control
ShortName:	GTC_PORT_CTL_B

GTC_PORT_CTL

Reset: soft

Address: 64270h-64273h
Name: DDI GTC Port Control
ShortName: GTC_PORT_CTL_C
Reset: soft

DWord	Bit	Description
0	31	**Port Global Time Code Enable** This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. This bit has no effect if the GTC controller is disabled. **Value** / **Name** 0b – Disable 1b – Enable **Restriction** The Maintenance Phase Enable bit must be initially written as '0' when this bit is set.
	30:25	**Reserved**
	24	**Maintenance Phase Enable** This bit is used by software to transition from lock acquisition to lock maintenance phase. The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field. Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'. **Value** / **Name** / **Description** 0b – Lock – Lock acquisition phase. The controller writes or reads GTC every 1ms. 1b – Maintain – Lock maintenance phase. The controller writes or reads GTC every 10ms.
	23:1	**Reserved**
	0	**Port RX Lock Done** This bit indicates the remote GTC sink has achieved lock. This bit shall be written by software after reading remote GTC sink DPCD register. This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled. **Value** / **Name** 0b – Not Locked 1b – Locked

GTC_PORT_MISC

GTC_PORT_MISC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64394h-64397h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_USBC1
Reset:	soft
Address:	64494h-64497h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_USBC2
Reset:	soft
Address:	64594h-64597h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_USBC3
Reset:	soft
Address:	64694h-64697h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_USBC4
Reset:	soft
Address:	64794h-64797h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_USBC5
Reset:	soft
Address:	64894h-64897h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_USBC6
Reset:	soft
Address:	64094h-64097h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_A
Reset:	soft
Address:	64194h-64197h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_B

GTC_PORT_MISC

Reset:	soft
Address:	64294h-64297h
Name:	DDI GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_C
Reset:	soft

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21:12	**GTC Update Message Delay** Default Value: 00110100b 52 nanoseconds This field programs the absolute delay in nanoseconds between the GTC at the aux sync point event and the corresponding GTC value at the capture point. It represents the delay between the GTC values at the aux sync point and capture point introduced due to synchronization and glitch suppression.
	11:8	**Min Lock Duration** Default Value: 1010b 10ms This field determines the minimum duration in milliseconds of lock acquisition and maintenance phase after which software is notified through interrupt. The GTC interrupt enable and mask register must be enabled beforehand. Software may also poll the interrupt identity bit in IIR.
	7:0	**Reserved** Access: RO Format: MBZ

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	64378h-6437Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_USBC1
Reset:	soft
Address:	64478h-6447Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_USBC2
Reset:	soft
Address:	64578h-6457Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_USBC3
Reset:	soft
Address:	64678h-6467Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_USBC4
Reset:	soft
Address:	64778h-6477Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_USBC5
Reset:	soft
Address:	64878h-6487Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_USBC6
Reset:	soft
Address:	64078h-6407Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_A
Reset:	soft
Address:	64178h-6417Bh
Name:	DDI GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_B

GTC_PORT_TX_CURR		
Reset:	soft	
Address:	64278h-6427Bh	
Name:	DDI GTC Port TX Current	
ShortName:	GTC_PORT_TX_CURR_C	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**Global Time Code Port TX Current** This field contains the local GTC value sampled at the Aux sync point of the response message from the remote GTC sink following software read of the remote sink GTC DPCD register.

GTC_PORT_TX_PREV

GTC_PORT_TX_PREV	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	64380h-64383h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_USBC1
Reset:	soft
Address:	64480h-64483h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_USBC2
Reset:	soft
Address:	64580h-64583h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_USBC3
Reset:	soft
Address:	64680h-64683h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_USBC4
Reset:	soft
Address:	64780h-64783h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_USBC5
Reset:	soft
Address:	64880h-64883h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_USBC6
Reset:	soft
Address:	64080h-64083h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_A
Reset:	soft
Address:	64180h-64183h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_B

GTC_PORT_TX_PREV

Reset:	soft
Address:	64280h-64283h
Name:	DDI GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_C
Reset:	soft

DWord	Bit	Description
0	31:0	**Global Time Code Port TX Previous** This field contains the previous local GTC value sampled at Aux sync point. It is transferred from the GTC_PORT_TX_CURR register when the current value is updated.

GT C6 Entry TSC LSB

GTC6_ENTRY_TSC_LSB - GT C6 Entry TSC LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00C28h	
C6 Entry TSC LSB		
DWord	**Bit**	**Description**
0	31:0	**Count for C6 entry TSC LSB** Access: RO _Custom_GTIReset: BUS C6 Entry TSC LSB

GT C6 Entry TSC MSB

GTC6_ENTRY_TSC_MSB - GT C6 Entry TSC MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00C2Ch	
C6 Entry TSC MSB		
DWord	**Bit**	**Description**
0	31:24	**RSVD** Access: RO _Custom_GTIReset: BUS RSVD
	23:0	**Count GT C6 Entry TSC MSB** Access: RO _Custom_GTIReset: BUS C6 Entry TSC MSB

GT C6 Residency LSB

GTC6_RESIDENCY_LSB - GT C6 Residency LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00C20h	
C6 Residency LSB		
DWord	**Bit**	**Description**
0	31:0	**Count for C6 Residency** Access: RO _Custom_GTIReset: BUS C6 Resindency LSB

GT C6 Residency MSB

GTC6_RESIDENCY_MSB - GT C6 Residency MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00C24h	
C6 Residency MSB		
DWord	**Bit**	**Description**
0	31:24	**RSVD** Access: RO _Custom_GTIReset: BUS RSVD
	23:0	**Count for C6 Residency** Access: RO _Custom_GTIReset: BUS C6 Residency MSB

GT Correctable Err Status Register

ERR_STAT_FUSA_GT_COR - GT Correctable Err Status Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100160h

This register captures GT Correctable Errors for FuSa functionality.

DWord	Bit	Description
0	31:16	**Error Mask** Default Value: ffffh Access: R/W _Custom_GTIReset: BUS Bits for masking errors defined on bits 15:0 of ERR_STAT_FUSA_GT_COR. These bits are independent of the lower 16 bits -i.e a write to one of these bits is not required to set/clear the lower 16.
	15:1	**Reserved**
	0	**L3 Single Error Corrected** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS L3 single error corrected

GTDRIVER_MAILBOX_DATA1

GTDRIVER_MAILBOX_DATA1 - GTDRIVER_MAILBOX_DATA1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	13812Ch	
Data register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU I/O SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES.		
DWord	**Bit**	**Description**
0	31:0	**Considerations**

GTDRIVER_MAILBOX_INTERFACE

GTDRIVER_MAILBOX_INTERFACE - GTDRIVER_MAILBOX_INTERFACE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	138124h

Control and Status register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_DATA. THIS REGISTER IS DUPLICATED IN THE PCU.

DWord	Bit	Description
0	31:0	**Considerations**

GTDRIVER_P2G_EVENTS

GTDRIVER_P2G_EVENTS - GTDRIVER_P2G_EVENTS	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	138160h

This extended capability allows PCODE to send an interrupt notification upon completion of a mailbox command. It is enabled via the GFX Driver Mailbox. PCODE will set the appropriate bit in this register to 1b, and will then write to 0.2.0.GTTMMADR.PIM[PCU_MBOXE]. The GFX Driver will clear the appropriate bit in this register by writing a 1 to the bit. THIS REGISTER IS DUPLICATED IN THE PCU I/O SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES.

DWord	Bit	Description
0	31:0	**Considerations**

GT Engine Interrupt Enable

GT_ENG_INTR_ENABLE - GT Engine Interrupt Enable

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	190030h
ShortName:	RENDER_COPY_INTR_ENABLE
Address:	190034h
ShortName:	VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	190038h
ShortName:	GUC_SCATTERGATHER_INTR_ENABLE
Address:	19003Ch
ShortName:	GPM_WGBOXPERF_INTR_ENABLE
Address:	190044h
ShortName:	GUNIT_CSME_INTR_ENABLE
Address:	190048h
ShortName:	CCS_RSVD_INTR_ENABLE

SW/FW programs this register to control interrupt events that are to be ignored (dropped).
Register content is saved/restored during RC6.
Bits in the registers described above are in the order: Engine1_Engine0_INTR_ENABLE.

Register Address	Engine 1	Engine 0	Structure defining bits
190030	Render	Copy	Render: Render Engine Interrupt Vector Copy: Blitter Interrupt Vector
190034	Vide Decode	Video Enhace	Video Decode: VideoDecoder Interrupt Vector Video Enhance: VideEnhancement Interupt Vector
190038	GuC	Scatter Gather	GuC: GUC Interrupt Vector Scatter Gather: Scatter Gather Interrupt Vector
19003C	GPM	WGBoxPerf	GPM: GTPM Interrupt Vector WGBoxPerf: WDBoxOAInterrupt Vector
190040	Reserved	Reserved	Reserved:
190044	GUnit	CSME	GUnit: G-Unit Interrupt Vector CSME: Manageability Engine Interrupt Vector
190048	CCS	Reserved	CCS: Compute CS Reserved

DWord	Bit	Description
0	31:16	**Engine1 Interrupt Enable** Default Value: 0000h Access: R/W

GT_ENG_INTR_ENABLE - GT Engine Interrupt Enable			
		_Custom_GTIReset:	BUS
	15:0	**Engine0 Interrupt Enable**	
		Default Value:	0000h
		Access:	R/W
		_Custom_GTIReset:	BUS

GT Engine Interrupt Mask

GT_ENG_INTR_MASK - GT Engine Interrupt Mask			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	190090h		
ShortName:	RCS0_RSVD_INTR_MASK		
Address:	1900A0h		
ShortName:	BCS_RSVD_INTR_MASK		
Address:	1900A8h		
ShortName:	VCS0_VCS1_INTR_MASK		
Address:	1900ACh		
ShortName:	VCS2_VCS3_INTR_MASK		
Address:	1900B0h		
ShortName:	VCS4_VCS5_INTR_MASK		
Address:	1900B4h		
ShortName:	VCS6_VCS7_INTR_MASK		
Address:	1900D0h		
ShortName:	VECS0_VECS1_INTR_MASK		
Address:	1900D4h		
ShortName:	VECS2_VECS3_INTR_MASK		
Address:	1900E8h		
ShortName:	GUC_SCATTERGATHER_INTR_MASK		
Address:	1900ECh		
ShortName:	GPM_WGBOXPERF_INTR_MASK		
Address:	1900F4h		
ShortName:	GUNIT_CSME_INTR_MASK		
Address:	190100h		
ShortName:	CCS0_CCS1_INTR_MASK		
DWord	**Bit**	**Description**	
0	31:16	**Engine1 Interrupt Mask**	
		Default Value:	0000h
		Access:	R/W
		_Custom_GTIReset:	BUS

GT_ENG_INTR_MASK - GT Engine Interrupt Mask		
	15:0	**Engine0 Interrupt Mask** Default Value: 0000h Access: R/W _Custom_GTIReset: BUS

GT Fatal Err Status Register

ERR_STAT_FUSA_GT_FATAL - GT Fatal Err Status Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100168h

This register captures GT Fatal Errors for FuSa functionality.

DWord	Bit	Description
0	31:16	**Error Mask** Default Value: ffffh Access: R/W _Custom_GTIReset: BUS Bits for masking errors defined on bits 15:0 of ERR_STAT_FUSA_GT_FATAL. These bits are independent of the lower 16 bits -i.e a write to one of these bits is not required to set/clear the lower 16.
	15:9	**Reserved**
	8	**IDI Parity Error** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS IDI Parity Error
	7:6	**Reserved HW Error2** Access: R/WC _Custom_GTIReset: BUS
	5	**L3 ECC Checker Error** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS L3 ECC Checker Error
	4	**L3 Double Error** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS L3 double error
	3:2	**Reserved HW Error1** Access: R/WC _Custom_GTIReset: BUS

ERR_STAT_FUSA_GT_FATAL - GT Fatal Err Status Register

	1	**Array Bist Error** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS Array BIST Error
	0	**Reserved HW Error0** Access: R/WC _Custom_GTIReset: BUS

GT Function Level Reset Control Message

FLRCTLMSG - GT Function Level Reset Control Message

Register Space:	MMIO: 0/2/0
Size (in bits):	32
CrashLogSaved:	true
CrashLogVisibility:	cspec
Address:	08100h

GT Reset Control Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**Reserved** Access: RO Format: MBZ
	0	**Initiate GT Function Level Reset Message** Access: R/W Set _Custom_GTIReset: BUS GT Function Level Reset (FLR) 1: Initiate GT FLR - This is a Non-Posted message to reset Render, Media, Blitter and GTI-Device domains. - This bit is cleared by the CPunit upon completion of the reset.

GTICP BONUS1 Reg

GTICPBONUS1 - GTICP BONUS1 Reg

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24014h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request

GTICPBONUS1 - GTICP BONUS1 Reg

		'1' : Initiate Power UP req
	3	**BONUS BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

GTICP BONUS2 Reg

GTICPBONUS2 - GTICP BONUS2 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24018h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)

GTICPBONUS2 - GTICP BONUS2 Reg

	4	**BONUS BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

GT Interrupt DW0

GT_INTR_DW0 - GT Interrupt DW0

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 190018h

Engine bits in this register are set if any of the unmasked bits in the underlying engine 16b interrupt vector is non-zero

DWord	Bit	Description
0	31	**CSME** Access: R/W One Clear
	30	**Reserved** Access: RO Format: MBZ
	29	**Reserved** Access: RO Format: MBZ
	28	**GUNIT** Access: R/W One Clear
	27:26	**Reserved** Access: RO Format: MBZ
	25	**GUC** Access: R/W One Clear
	24	**Reserved** Access: RO Format: MBZ
	23	**SCTRGTHR** Access: R/W One Clear
	22	**Reserved** Access: RO Format: MBZ
	21	**Reserved** Access: RO Format: MBZ

GT_INTR_DW0 - GT Interrupt DW0

	20	**WDPERF** Access: R/W One Clear
	19	**KCR** Access: R/W One Clear
	18	**Reserved** Access: RO Format: MBZ
	17	**Reserved** Access: RO Format: MBZ
	16	**GTPM** Access: R/W One Clear
	15	**BCS** Access: R/W One Clear
	14:10	**Reserved**
	9:8	**Reserved** Access: RO Format: MBZ
	7	**CCS3** Access: R/W One Clear
	6	**CCS2** Access: R/W One Clear
	5	**CCS1** Access: R/W One Clear
	4	**CCS0** Access: R/W One Clear
	3:1	**Reserved** Access: RO Format: MBZ
	0	**RCS0** Access: R/W One Clear

GT Interrupt DW1

GT_INTR_DW1 - GT Interrupt DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	19001Ch	
Interrupt bits indicating one of theunderlying engine interrupts is non-zero		
DWord	**Bit**	**Description**
0	31	**VECS0** Access: R/W One Clear
	30	**VECS1** Access: R/W One Clear
	29	**VECS2** Access: R/W One Clear
	28	**VECS3** Access: R/W One Clear
	27:8	**Reserved** Access: RO Format: MBZ
	7	**VCS7** Access: R/W One Clear
	6	**VCS6** Access: R/W One Clear
	5	**VCS5** Access: R/W One Clear
	4	**VCS4** Access: R/W One Clear
	3	**VCS3** Access: R/W One Clear
	2	**VCS2** Access: R/W One Clear
	1	**VCS1** Access: R/W One Clear
	0	**VCS0** Access: R/W One Clear

GT Interrupt Identity

GT_INTR_IDENTITY - GT Interrupt Identity

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	190060h
ShortName:	INTR_IDENTITY_REG0
Address:	190064h
Name:	INTR_IDENTITY_REG1
ShortName:	INTR_IDENTITY_REG1

HW displays the interrupt bits for engine chosen using Selector.
Only unmasked interrupts are displayed. Masked interrupts continue to accumulate behind the mask.
After processing, SW shall write 1's to clear. (Bit 31 must be cleared by SW)
Write to Clear indicates to HW that processing is complete (for displayed interrupts).

DWord	Bit	Description
0	31	**Data Valid** Access: R/W
	30:26	**Reserved** Access: RO Format: MBZ
	25:20	**Engine Instance ID** Engine Instance ID format is defined in structure "Engine ID Definition"
	19	**Reserved** Access: RO Format: MBZ
	18:16	**Engine Class ID** Engine class is defined in structure "Engine ID Definition"
	15:0	**Engine Interrupt** Access: R/W Format is specific to the engine that is sending the interrupt. Format is defined in structure "EngineInterrupt Vector" (where engine isBlitter/G-Unit/GTPM/GuC/Render Engine/Video Decoder/VideoEnhancement).

GT Interrupt IIR Selector

GT_INTR_IIR_SELECTOR - GT Interrupt IIR Selector

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	190070h
ShortName:	IIR_REG0_SELECTOR
Address:	190074h
ShortName:	IIR_REG1_SELECTOR

This is a basic register template

DWord	Bit	Description
0	31:0	**Engine ID** Access: R/W SW/FW shall program the appropriate Engine ID to view the interrupts from an engine Engine_ID is a one-hot encoding that follows the bit definition of GuC GT Interrupt DW register. Register: IIR_REG0_SELECTOR — Bit Definiition: Format: GT Interrupt DW0 Register: IIR_REG1_SELECTOR — Bit Definiition: Format: GT Interrupt DW1

GTI PGFET control register with lock

GTIPFETCTL - GTI PGFET control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24008h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of MEDIA1 PGFETCTL register are R/W 1 = All bits of MEDIA1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:26	**Reserved** Access: RO Format: MBZ
	25	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	24	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up

GTIPFETCTL - GTI PGFET control register with lock

	Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
22	**Reserved** Access: RO Format: MBZ
21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 110b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
18:16	**Strobe pulse period** Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) Value: 001b — Name: **[Default]**
15:0	**PFET Ladder Step Sequence** Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.

GTIPFETCTL - GTI PGFET control register with lock

15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Value	Name
1000011111111001b	**[Default]**

GTI Power Gate Control Request

GTIPGCTLREQ - GTI Power Gate Control Request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24000h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS Media1 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

GT Mode Register

GT_MODE - GT Mode Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	07008h
Name:	GT Mode Register
ShortName:	GT_MODE

This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**EU Local Thread Checking Enable** Access: R/W _Custom_GTIReset: DEV This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address. Value / Name / Description: 0h / Disable **[Default]** / EU local thread checking is disabled. 1h / Enable / EU local thread checking is enabled.
	14:13	**SFR mode** Access: R/W Format: U2 _Custom_GTIReset: DEV This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.
	12:11	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

GT_MODE - GT Mode Register

10 HW Binding Table Alignment

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

This bit changes the format of the binding table pointer.

When this bit is set, the format of the binding table is SW binding table format whether Binding Table Pool is enabled or disabled.

Value	Name	Description
0h	Legacy **[Default]**	Binding table pointer 15:5 Maps to 15:5 for INTERFACE_DESCRIPTOR DATA. Binding table pointer 15:5 Maps to 15:5 for 3DSTATE_BINDING_TABLE_POINTER_* if Binding Table Pool is disabled. Binding table pointer 15:5 Maps to 16:6 for 3DSTATE_BINDING_TABLE_POINTER_* if Binding Table Pool is enabled.
1h	Enable 512KB Binding Table size	Binding table pointer maps to 18:8 for both 3DSTATE_BINDING_TABLE_POINTER_* and INTERFACE_DESCRIPTOR DATA.

9 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

8 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

7 Reserved

Access:	RO
Format:	MBZ

6 Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

GT_MODE - GT Mode Register

5:4 **Slice2 IZ Hashing: 7 EU subslice encoding**

Access:	R/W
_Custom_GTIReset:	DEV

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EU.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 2.

3:2 **Slice1 IZ Hashing: 7 EU subslice encoding**

Access:	R/W
_Custom_GTIReset:	DEV

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 1.

1:0 **Slice 0 IZ Hashing: 7 EU subslice encoding**

Access:	R/W
_Custom_GTIReset:	DEV

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 0.

GT Non Fatal Err Status Register

ERR_STAT_FUSA_GT_NONFATAL - GT Non Fatal Err Status Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	100164h

This register captures GT Non-Fatal errors for FuSa functionality

DWord	Bit	Description
0	31:16	**Error Mask** Default Value: ffffh Access: R/W _Custom_GTIReset: BUS bits for masking errors defined on bit 15:0 of ERR_STAT_FUSA_DISP_NONFATAL. These bits are independent of the lower 16 bits -i.e a write to one of these bits is not required to set/clear the lower 16.
	15:0	**Reserved**

GTPO Triggering Block 1 Mask A

GTPO_TRIGGERING_BLOCK_1_MASK_A - GTPO Triggering Block 1 Mask A

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	0D214h-0D21Bh

Primary 64bit Mask Value for GTPO Triggering Block 1

DWord	Bit	Description
0..1	63:32	**GTPO TRIGGERING MASK A UPPER** Access: R/W _Custom_GTIReset: BUS Lower 32bit Mask Value for the value programmed in the corresponding match register
	31:0	**GTPO TRIGGERING MASK A LOWER** Access: R/W _Custom_GTIReset: BUS Lower 32bit Mask Value for the value programmed in the corresponding match register

GTPO Triggering Block 1 Mask B

GTPO_TRIGGERING_BLOCK_1_MASK_B - GTPO Triggering Block 1 Mask B	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	0D21Ch-0D223h
Secondary 64bit Mask Value for GTPO Triggering Block 1	

DWord	Bit	Description
0..1	63:32	**GTPO TRIGGERING Mask B Upper** Access: R/W _Custom_GTIReset: BUS Upper 32bit Mask Value for the value programmed in the corresponding match register
	31:0	**GTPO TRIGGERING Mask B Lower** Access: R/W _Custom_GTIReset: BUS Lower 32bit Mask Value for the value programmed in the corresponding match register

GTPO Triggering Block 1 Match A

GTPO_TRIGGERING_BLOCK1_MATCHA - GTPO Triggering Block 1 Match A

Register Space:	MMIO: 0/2/0
Size (in bits):	64
Address:	0D224h-0D22Bh

Primary 64bit Match Value for GTPO Triggering Block 1

DWord	Bit	Description
0..1	63:32	**Match A Upper** Access: R/W _Custom_GTIReset: BUS Upper 32bit match value for use by GTPO triggering block
	31:0	**Macth A Lower** _Custom_GTIReset: BUS Lower 32bit match value for use by GTPO triggering block

GTPO Triggering Block 1 Match B

GTPO_TRIGGERING_BLOCK_1_MATCH_B - GTPO Triggering Block 1 Match B

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	0D22Ch-0D233h

Secondary 64bit Match Value for GTPO Triggering Block 1

DWord	Bit	Description
0..1	63:32	**GTPO TRIGGERING Match B Upper** Access: R/W _Custom_GTIReset: BUS Upper 32bit match value for use by GTPO triggering block
	31:0	**GTPO Triggering Match B Lower** Access: R/W _Custom_GTIReset: BUS Lower 32bit match value for use by GTPO triggering block

GTPO Triggering Block Mode Enable

GTPO_TRIGGERING_BLOCK_MODE - GTPO Triggering Block Mode Enable

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0D234h

Register to enable and set the mode for 4 GTPO triggering blocks

DWord	Bit	Description
0	31:3	**GTPO BLOCK MODE ENABLE RSVD** Access: R/W _Custom_GTIReset: BUS
	2:1	**GTPO Triggering Block 1 Mode** Default Value: 00b Access: R/W _Custom_GTIReset: BUS 01 - Match; 10 - Match Secondary; 11 - Match Content;
	0	**GTPO Triggering Block 1 Enable** Default Value: 0b _Custom_GTIReset: BUS

GTSCRATCH

GTSCRATCH	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	4F100h-4F11Fh
Name:	GT SCRATCH
ShortName:	GTSCRATCH_*

There are 8 instances of this register format.

Restriction
These registers are used by hardware and must not be used by software.

DWord	Bit	Description
0	31:0	**GT Sratchpad** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS GT Scratchpad

GTSP

GTSP	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	130040h-13005Fh
Name:	GT SCRATCHPAD
ShortName:	GTSP_*

There are 8 instances of this register format.

DWord	Bit	Description
0	31:0	**GT Scratchpad** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS GT Scratchpad

GT Virtual Function Engine Interrupt Enable

GT_ENG_INTR_ENABLE - GT Virtual Function Engine Interrupt Enable	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	191030h
ShortName:	VF1_RENDER_COPY_INTR_ENABLE
Address:	192030h
ShortName:	VF2_RENDER_COPY_INTR_ENABLE
Address:	193030h
ShortName:	VF3_RENDER_COPY_INTR_ENABLE
Address:	194030h
ShortName:	VF4_RENDER_COPY_INTR_ENABLE
Address:	195030h
ShortName:	VF5_RENDER_COPY_INTR_ENABLE
Address:	196030h
ShortName:	VF6_RENDER_COPY_INTR_ENABLE
Address:	197030h
ShortName:	VF7_RENDER_COPY_INTR_ENABLE
Address:	191034h
ShortName:	VF1_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	192034h
ShortName:	VF2_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	193034h
ShortName:	VF3_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	194034h
ShortName:	VF4_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	195034h
ShortName:	VF5_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	196034h
ShortName:	VF6_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	197034h
ShortName:	VF7_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	191038h

GT_ENG_INTR_ENABLE - GT Virtual Function Engine Interrupt Enable

ShortName:	VF1_GUC_RESVD_INTR_ENABLE
Address:	192038h
ShortName:	VF2_GUC_RESVD_INTR_ENABLE
Address:	193038h
ShortName:	VF3_GUC_RESVD_INTR_ENABLE
Address:	194038h
ShortName:	VF4_GUC_RESVD_INTR_ENABLE
Address:	195038h
ShortName:	VF5_GUC_RESVD_INTR_ENABLE
Address:	196038h
ShortName:	VF6_GUC_RESVD_INTR_ENABLE
Address:	197038h
ShortName:	VF7_GUC_RESVD_INTR_ENABLE
Address:	191048h
ShortName:	VF1_CCS_RSVD_INTR_ENABLE
Address:	192048h
ShortName:	VF2_CCS_RSVD_INTR_ENABLE
Address:	193048h
ShortName:	VF3_CCS_RSVD_INTR_ENABLE
Address:	194048h
ShortName:	VF4_CCS_RSVD_INTR_ENABLE
Address:	195048h
ShortName:	VF5_CCS_RSVD_INTR_ENABLE
Address:	196048h
ShortName:	VF6_CCS_RSVD_INTR_ENABLE
Address:	197048h
ShortName:	VF7_CCS_RSVD_INTR_ENABLE

DWord	Bit	Description
0	31:16	**Engine1 Interrupt Enable** Access: R/W
	15:0	**Engine0 Interrupt Enable** Access: R/W

GT Virtual Function Engine Interrupt Mask

GT Virtual Function Engine Interrupt Mask	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	191090h
ShortName:	VF1_RCS0_RSVD_INTR_MASK
Address:	192090h
ShortName:	VF2_RCS0_RSVD_INTR_MASK
Address:	193090h
ShortName:	VF3_RCS0_RSVD_INTR_MASK
Address:	194090h
ShortName:	VF4_RCS0_RSVD_INTR_MASK
Address:	195090h
ShortName:	VF5_RCS0_RSVD_INTR_MASK
Address:	196090h
ShortName:	VF6_RCS0_RSVD_INTR_MASK
Address:	197090h
ShortName:	VF7_RCS0_RSVD_INTR_MASK
Address:	1910A0h
ShortName:	VF1_BCS_RSVD_INTR_MASK
Address:	1920A0h
ShortName:	VF2_BCS_RSVD_INTR_MASK
Address:	1930A0h
ShortName:	VF3_BCS_RSVD_INTR_MASK
Address:	1940A0h
ShortName:	VF4_BCS_RSVD_INTR_MASK
Address:	1950A0h
ShortName:	VF5_BCS_RSVD_INTR_MASK
Address:	1960A0h
ShortName:	VF6_BCS_RSVD_INTR_MASK
Address:	1970A0h
ShortName:	VF7_BCS_RSVD_INTR_MASK
Address:	1910A8h
ShortName:	VF1_VCS0_VCS1_INTR_MASK

GT Virtual Function Engine Interrupt Mask	
Address:	1920A8h
ShortName:	VF2_VCS0_VCS1_INTR_MASK
Address:	1930A8h
ShortName:	VF3_VCS0_VCS1_INTR_MASK
Address:	1940A8h
ShortName:	VF4_VCS0_VCS1_INTR_MASK
Address:	1950A8h
ShortName:	VF5_VCS0_VCS1_INTR_MASK
Address:	1960A8h
ShortName:	VF6_VCS0_VCS1_INTR_MASK
Address:	1970A8h
ShortName:	VF7_VCS0_VCS1_INTR_MASK
Address:	1910ACh
ShortName:	VF1_VCS2_VCS3_INTR_MASK
Address:	1920ACh
ShortName:	VF2_VCS2_VCS3_INTR_MASK
Address:	1930ACh
ShortName:	VF3_VCS2_VCS3_INTR_MASK
Address:	1940ACh
ShortName:	VF4_VCS2_VCS3_INTR_MASK
Address:	1950ACh
ShortName:	VF5_VCS2_VCS3_INTR_MASK
Address:	1960ACh
ShortName:	VF6_VCS2_VCS3_INTR_MASK
Address:	1970ACh
ShortName:	VF7_VCS2_VCS3_INTR_MASK
Address:	1910B0h
ShortName:	VF1_VCS4_VCS5_INTR_MASK
Address:	1920B0h
ShortName:	VF2_VCS4_VCS5_INTR_MASK
Address:	1930B0h
ShortName:	VF3_VCS4_VCS5_INTR_MASK
Address:	1940B0h
ShortName:	VF4_VCS4_VCS5_INTR_MASK

GT Virtual Function Engine Interrupt Mask

Address:	1950B0h
ShortName:	VF5_VCS4_VCS5_INTR_MASK
Address:	1960B0h
ShortName:	VF6_VCS4_VCS5_INTR_MASK
Address:	1970B0h
ShortName:	VF7_VCS4_VCS5_INTR_MASK
Address:	1910B4h
ShortName:	VF1_VCS6_VCS7_INTR_MASK
Address:	1920B4h
ShortName:	VF2_VCS6_VCS7_INTR_MASK
Address:	1930B4h
ShortName:	VF3_VCS6_VCS7_INTR_MASK
Address:	1940B4h
ShortName:	VF4_VCS6_VCS7_INTR_MASK
Address:	1950B4h
ShortName:	VF5_VCS6_VCS7_INTR_MASK
Address:	1960B4h
ShortName:	VF6_VCS6_VCS7_INTR_MASK
Address:	1970B4h
ShortName:	VF7_VCS6_VCS7_INTR_MASK
Address:	1910D0h
ShortName:	VF1_VECS0_VECS1_INTR_MASK
Address:	1920D0h
ShortName:	VF2_VECS0_VECS1_INTR_MASK
Address:	1930D0h
ShortName:	VF3_VECS0_VECS1_INTR_MASK
Address:	1940D0h
ShortName:	VF4_VECS0_VECS1_INTR_MASK
Address:	1950D0h
ShortName:	VF5_VECS0_VECS1_INTR_MASK
Address:	1960D0h
ShortName:	VF6_VECS0_VECS1_INTR_MASK
Address:	1970D0h
ShortName:	VF7_VECS0_VECS1_INTR_MASK

GT Virtual Function Engine Interrupt Mask	
Address:	1910D4h
ShortName:	VF1_VECS2_VECS3_INTR_MASK
Address:	1920D4h
ShortName:	VF2_VECS2_VECS3_INTR_MASK
Address:	1930D4h
ShortName:	VF3_VECS2_VECS3_INTR_MASK
Address:	1940D4h
ShortName:	VF4_VECS2_VECS3_INTR_MASK
Address:	1950D4h
ShortName:	VF5_VECS2_VECS3_INTR_MASK
Address:	1960D4h
ShortName:	VF6_VECS2_VECS3_INTR_MASK
Address:	1970D4h
ShortName:	VF7_VECS2_VECS3_INTR_MASK
Address:	1910E8h
ShortName:	VF1_GUC_RESVD_INTR_MASK
Address:	1920E8h
ShortName:	VF2_GUC_RESVD_INTR_MASK
Address:	1930E8h
ShortName:	VF3_GUC_RESVD_INTR_MASK
Address:	1940E8h
ShortName:	VF4_GUC_RESVD_INTR_MASK
Address:	1950E8h
ShortName:	VF5_GUC_RESVD_INTR_MASK
Address:	1960E8h
ShortName:	VF6_GUC_RESVD_INTR_MASK
Address:	1970E8h
ShortName:	VF7_GUC_RESVD_INTR_MASK
Address:	191100h
ShortName:	VF1_GPGPU1_GPGPU2_INTR_MASK
SW/FW programs this register to mask interrupt events to GuC. Register content is saved/restored during RC6. Bits in the registers described above are in the order: Engine1_Engine0_INTR_MASK. For e.g: Engine1 houses bits for: RCS0, BCS, VCS0,... Engine0 houses bits for: RSVD, RSVD, VCS1,...	

GT Virtual Function Engine Interrupt Mask

Register Address	Engine 1	Engine 0	Structure defining bits
190090	RCS0	Reserved	Format: Render Engine Interrupt Vector
1900A0	BCS	Reserved	Format: Blitter Interrupt Vector
1900A8 1900AC 1900B0 1900B4	VCS0 VCS2 VCS4 VCS6	VCS1 VCS3 VCS5 VCS7	Format: VideoDecoder Interrupt Vector
1900D0 1900D4	VECS0 VECS2	VECS1 VECS3	Format: VideEnhancement Interrupt Vector
1900E8	GuC	Scatter Gather	GuC: GUC Interrupt Vector Scatter Gather: Scatter Gather Interrupt Vector
1900EC	GPM	WGBoxPerf	GPM: GTPM Interrupt Vector WGBoxPerf: WDBoxOAInterrupt Vector
1900F0		Reserved	Reserved:
1900F4	GUnit	CSME	GUnit: G-Unit Interrupt Vector CSME: Manageability Engine Interrupt Vector

DWord	Bit	Description
0	31:16	**Engine1 Interrupt Mask** Access: R/W
	15:0	**Engine0 Interrupt Mask** Access: R/W

GT Virtual Function IIR Selector

GT_VF_INTR_IIR_SELECTOR - GT Virtual Function IIR Selector	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	191070h
ShortName:	VF1_IIR_REG0_SELECTOR
Address:	191074h
ShortName:	VF1_IIR_REG1_SELECTOR
Address:	192070h
ShortName:	VF2_IIR_REG0_SELECTOR
Address:	192074h
ShortName:	VF2_IIR_REG1_SELECTOR
Address:	193070h
ShortName:	VF3_IIR_REG0_SELECTOR
Address:	193074h
ShortName:	VF3_IIR_REG1_SELECTOR
Address:	194070h
ShortName:	VF4_IIR_REG0_SELECTOR
Address:	194074h
ShortName:	VF4_IIR_REG1_SELECTOR
Address:	195070h
ShortName:	VF5_IIR_REG0_SELECTOR
Address:	195074h
ShortName:	VF5_IIR_REG1_SELECTOR
Address:	196070h
ShortName:	VF6_IIR_REG0_SELECTOR
Address:	196074h
ShortName:	VF6_IIR_REG1_SELECTOR
Address:	197070h
ShortName:	VF7_IIR_REG0_SELECTOR
Address:	197074h
ShortName:	VF7_IIR_REG1_SELECTOR
This is a basic register template	

DWord	Bit	Description

GT_VF_INTR_IIR_SELECTOR - GT Virtual Function IIR Selector

0	31:0	**Engine ID** Access: R/W SW/FW shall program the appropriate Engine ID to view the interrupts from an engine Engine_ID is a one-hot encoding that follows the bit definition of GuC GT Interrupt DW register. Register: IIR_REG0_SELECTOR — Bit Definiition: Format: GT Interrupt DW0 Register: IIR_REG1_SELECTOR — Bit Definiition: Format: GT Interrupt DW1

GT Virtual Function Interrupt DW0

GT_VF_INTR_DW0 - GT Virtual Function Interrupt DW0	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	191018h
Name:	VF1_INTR_DW0
ShortName:	VF1_INTR_DW0
Address:	192018h
Name:	VF2_INTR_DW0
ShortName:	VF2_INTR_DW0
Address:	193018h
Name:	VF3_INTR_DW0
ShortName:	VF3_INTR_DW0
Address:	194018h
Name:	VF4_INTR_DW0
ShortName:	VF4_INTR_DW0
Address:	195018h
Name:	VF5_INTR_DW0
ShortName:	VF5_INTR_DW0
Address:	196018h
Name:	VF6_INTR_DW0
ShortName:	VF6_INTR_DW0
Address:	197018h
Name:	VF7_INTR_DW0
ShortName:	VF7_INTR_DW0

Bits set in this register indicate if an engine has an interrupt that requires servicing.

DWord	Bit	Description
0	31	**CSME** Access: R/W
	30:29	**Reserved** Access: RO Format: MBZ
	28	**GUNIT** Access: R/W

GT_VF_INTR_DW0 - GT Virtual Function Interrupt DW0

	27:26	**Reserved** Access: RO Format: MBZ
	25	**GUC** Access: R/W
	24	**Reserved** Access: RO Format: MBZ
	23	**SCTRGTHR** Access: R/W
	22:21	**Reserved** Access: RO Format: MBZ
	20	**WDPERF** Access: R/W
	19	**KCR** Access: R/W
	18:17	**Reserved** Access: RO Format: MBZ
	16	**GTPM** Access: R/W
	15	**BCS** Access: R/W
	14:8	**Reserved** Access: RO Format: MBZ
	7	**CCS3**
	6	**CCS2**
	5	**CCS1**
	4	**CCS0**
	3:1	**Reserved** Access: RO Format: MBZ
	0	**RCS0** Access: R/W

GT Virtual Function Interrupt DW1

GT_VF_INTR_DW1 - GT Virtual Function Interrupt DW1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	19101Ch
ShortName:	VF1_INTR_DW1
Address:	19201Ch
ShortName:	VF2_INTR_DW1
Address:	19301Ch
ShortName:	VF3_INTR_DW1
Address:	19401Ch
ShortName:	VF4_INTR_DW1
Address:	19501Ch
ShortName:	VF5_INTR_DW1
Address:	19601Ch
ShortName:	VF6_INTR_DW1
Address:	19701Ch
ShortName:	VF7_INTR_DW1

Interrupt bits indicating one of theunderlying engine interrupts is non-zero

DWord	Bit	Description
0	31	**VECS0** Access: R/W
	30	**VECS1** Access: R/W
	29	**VECS2** Access: R/W
	28	**VECS3** Access: R/W
	27:8	**Reserved** Access: RO Format: MBZ
	7	**VCS7** Access: R/W
	6	**VCS6** Access: R/W

GT_VF_INTR_DW1 - GT Virtual Function Interrupt DW1		
	5	**VCS5** Access: R/W
	4	**VCS4** Access: R/W
	3	**VCS3** Access: R/W
	2	**VCS2** Access: R/W
	1	**VCS1** Access: R/W
	0	**VCS0** Access: R/W

GT Virtual Function Interrupt Identity

GT_VF_INTR_IDENTITY - GT Virtual Function Interrupt Identity	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	191060h
ShortName:	VF1_INTR_IDENTITY_REG0
Address:	191064h
ShortName:	VF1_INTR_IDENTITY_REG1
Address:	192060h
ShortName:	VF2_INTR_IDENTITY_REG0
Address:	192064h
ShortName:	VF2_INTR_IDENTITY_REG1
Address:	193060h
ShortName:	VF3_INTR_IDENTITY_REG0
Address:	193064h
ShortName:	VF3_INTR_IDENTITY_REG1
Address:	194060h
ShortName:	VF4_INTR_IDENTITY_REG0
Address:	194064h
ShortName:	VF4_INTR_IDENTITY_REG1
Address:	195060h
ShortName:	VF5_INTR_IDENTITY_REG0
Address:	195064h
ShortName:	VF5_INTR_IDENTITY_REG1
Address:	196060h
ShortName:	VF6_INTR_IDENTITY_REG0
Address:	196064h
ShortName:	VF6_INTR_IDENTITY_REG1
Address:	197060h
ShortName:	VF7_INTR_IDENTITY_REG0
Address:	197064h
ShortName:	VF7_INTR_IDENTITY_REG1
HW displays the interrupt bits for engine chosen using Selector. Only unmasked interrupts are displayed. Masked interrupts continue to accumulate behind the mask.	

GT_VF_INTR_IDENTITY - GT Virtual Function Interrupt Identity

After processing, SW shall write 1's to clear. (Bit 31 must be cleared by SW)
Write to Clear indicates to HW that processing is complete (for displayed interrupts).

DWord	Bit	Description
0	31	**Data Valid** Access: R/W
	30:26	**Reserved** Access: RO Format: MBZ
	25:20	**Engine Instance ID**
	19	**Reserved** Access: RO Format: MBZ
	18:16	**Engine Class ID**
	15:0	**Engine Interrupt** Access: R/W

GUC_HOST_INTR_IIR

GUC_HOST_INTR_IIR - GUC_HOST_INTR_IIR

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	1901F0h

This register provides a capability for a Host SW to communicate with GuC FW. The Host SW, whether Host OS/VMM or a Guest VM, writes to this register at MMIO offset 1901F0h with a 32-bit payload, which results in the Gunit sending an interrupt to GuC, which can then retrieve the payload from this register using the appropriate Gunit unique address.

DWord	Bit	Description
0	31:0	**Data** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS Data

GuC DMA Interrupt Input

GUC_DMA_IIR - GuC DMA Interrupt Input

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

DWord	Bit	Description
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**DMA Service Interrupt Routing** 0h – Host **[Default]** – Interrupts will be routed to the host CPU. 1h – Reserved – Reserved
	0	**DMA Interrupt** There can only be one DMA workload outstanding at any time. Set by DMA hardware. Cleared by Host. 0h – No DMA Interrupt Pending **[Default]** 1h – DMA Interrupt Pending

GuC Doorbell Group 0 Interrupt Status

GUC_DB_ISR_0 - GuC Doorbell Group 0 Interrupt Status	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
This is a "shadow" of registers in GTI. The GuC takes a snapshot when it services them. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.	

DWord	Bit	Description
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 0 through 31.

GuC Doorbell Group 1 Interrupt Status

GUC_DB_ISR_1 - GuC Doorbell Group 1 Interrupt Status	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32

Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.

DWord	Bit	Description
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 32 through 63.

GuC Doorbell Group 2 Interrupt Status

GUC_DB_ISR_2 - GuC Doorbell Group 2 Interrupt Status		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.		
DWord	**Bit**	**Description**
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 64 through 95.

GuC Doorbell Group 3 Interrupt Status

GUC_DB_ISR_3 - GuC Doorbell Group 3 Interrupt Status	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32

Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.

DWord	Bit	Description
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 96 through 127.

GuC Doorbell Group 4 Interrupt Status

GUC_DB_ISR_4 - GuC Doorbell Group 4 Interrupt Status		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.		
DWord	**Bit**	**Description**
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 128 through 159.

GuC Doorbell Group 5 Interrupt Status

GUC_DB_ISR_5 - GuC Doorbell Group 5 Interrupt Status	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32

Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.

DWord	Bit	Description
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 160 through 191.

GuC Doorbell Group 6 Interrupt Status

GUC_DB_ISR_6 - GuC Doorbell Group 6 Interrupt Status		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.		
DWord	**Bit**	**Description**
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 192 through 223.

GuC Doorbell Group 7 Interrupt Status

GUC_DB_ISR_7 - GuC Doorbell Group 7 Interrupt Status	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32

Interrupt status shadow copy. Access: copy-write by the GuC hardware, read and cleared by the uKernel and host CPU.

DWord	Bit	Description
0	31:0	**Interrupt Status** GuC shadow copy of the interrupt status mask for doorbells 224 through 255.

GuC Engine Interrupt Mask

GUC_ENG_INTR_MASK - GuC Engine Interrupt Mask		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:16	**Engine1 Interrupt Mask** Access: R/W
	15:0	**Engine0 Interrupt Mask** Access: R/W

Guc GT Interrupt DW1

GUC_GT_INTR_DW1 - Guc GT Interrupt DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
This is a basic register template		
DWord	**Bit**	**Description**
0	31	**VECS0** Access: R/W
	30	**VECS1** Access: R/W
	29	**VECS2** Access: R/W
	28	**VECS3** Access: R/W
	27:8	**Reserved** Access: RO Format: MBZ
	7	**VCS7** Access: R/W
	6	**VCS6** Access: R/W
	5	**VCS5** Access: R/W
	4	**VCS4** Access: R/W
	3	**VCS3** Access: R/W
	2	**VCS2** Access: R/W
	1	**VCS1** Access: R/W
	0	**VCS0** Access: R/W

GuC Host Interrupt Interrupt Input 0

GUC_HOST_INTR_IIR_0 - GuC Host Interrupt Interrupt Input 0		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
The format of this register is defined by software. The host CPU is expected to write this register and the uKernel to read it.		
DWord	**Bit**	**Description**
0	31:0	**Scratch**

GuC Host Interrupt Mask 0

GUC_HOST_INTR_MASK_0 - GuC Host Interrupt Mask 0		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Interrupt Masks for the host KMD that can generate interrupts. When virtualization is enabled, bits 1 through 31 may indicated interrupts		
DWord	**Bit**	**Description**
0	31:8	**VF N Intr Mask**
	7	**VF7 Intr Mask**
	6	**VF6 Intr Mask**
	5	**VF5 Intr Mask**
	4	**VF4 Intr Mask**
	3	**VF3 Intr Mask**
	2	**VF2 Intr Mask**
	1	**VF1 Intr Mask**
	0	**Host Intr Mask**

GuC Host Interupt Enable 0

GUC_HOST_INTR_ENA_0 - GuC Host Interupt Enable 0

Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32

Interrupt Enables for the host KMD that can generate interrupts.
When virtualization is enabled, bits 1 through 31 may indicated interrupts
Contents of the register are saved and restored across RC6 transitions.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**VF7 Intr Enable**
	6	**VF6 Intr Enable**
	5	**VF5 Intr Enable**
	4	**VF4 Intr Enable**
	3	**VF3 Intr Enable**
	2	**VF2 Intr Enable**
	1	**VF1 Intr Enable**
	0	**Host Intr Enable**

GuC Interupt IIR Selector

INTR_IIR_SELECTOR - GuC Interupt IIR Selector		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:0	**Engine ID** Access: R/W SW/FW shall program the appropriate Engine ID to view the interrupts from an engine. Engine_ID is a one-hot encoding that follows the bit definition of GuC GT Interrupt DW register. GUC_IIR_REG0_SELECTOR uses GuC GT Interrupt DW0. GUC_IIR_REG1_SELECTOR uses GuC GT Interrupt DW1. **Programming Notes** A write to the selector is dropped if there are no interrupts to be serviced - because the State Machine is not in the correct state to accept the selector write

Guc Peek Register 0

DRB0PEEK - Guc Peek Register 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01920h	

DWord	Bit	Description
0	31	**Doorbell #(0*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(0*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(0*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(0*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(0*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB0PEEK - Guc Peek Register 0

26	**Doorbell #(0*32+26) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+26) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
25	**Doorbell #(0*32+25) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+25) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
24	**Doorbell #(0*32+24) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+24) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
23	**Doorbell #(0*32+23) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+23) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
22	**Doorbell #(0*32+22) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+22) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
21	**Doorbell #(0*32+21) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+21) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB0PEEK - Guc Peek Register 0

	20	**Doorbell #(0*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	19	**Doorbell #(0*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	18	**Doorbell #(0*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	17	**Doorbell #(0*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	16	**Doorbell #(0*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	15	**Doorbell #(0*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB0PEEK - Guc Peek Register 0

14 Doorbell #(0*32+14) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(0*32+14) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

13 Doorbell #(0*32+13) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(0*32+13) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

12 Doorbell #(0*32+12) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(0*32+12) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

11 Doorbell #(0*32+11) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(0*32+11) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

10 Doorbell #(0*32+10) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(0*32+10) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

9 Doorbell #(0*32+9) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(0*32+9) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB0PEEK - Guc Peek Register 0

	8	**Doorbell #(0*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(0*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(0*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(0*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(0*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(0*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB0PEEK - Guc Peek Register 0

	2	**Doorbell #(0*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(0*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(0*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(0*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 1

DRB1PEEK - Guc Peek Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01924h	

DWord	Bit	Description
0	31	**Doorbell #(1*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(1*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(1*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(1*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(1*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB1PEEK - Guc Peek Register 1

26	**Doorbell #(1*32+26) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+26) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
25	**Doorbell #(1*32+25) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+25) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
24	**Doorbell #(1*32+24) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+24) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
23	**Doorbell #(1*32+23) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+23) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
22	**Doorbell #(1*32+22) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+22) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
21	**Doorbell #(1*32+21) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+21) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB1PEEK - Guc Peek Register 1

	20	**Doorbell #(1*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	19	**Doorbell #(1*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	18	**Doorbell #(1*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	17	**Doorbell #(1*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	16	**Doorbell #(1*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	15	**Doorbell #(1*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB1PEEK - Guc Peek Register 1

14	**Doorbell #(1*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
13	**Doorbell #(1*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
12	**Doorbell #(1*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
11	**Doorbell #(1*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
10	**Doorbell #(1*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
9	**Doorbell #(1*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB1PEEK - Guc Peek Register 1

	8	**Doorbell #(1*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(1*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(1*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(1*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(1*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(1*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB1PEEK - Guc Peek Register 1

	2	**Doorbell #(1*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(1*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(1*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(1*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 2

DRB2PEEK - Guc Peek Register 2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01928h	

DWord	Bit	Description
0	31	**Doorbell #(2*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(2*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(2*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(2*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(2*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB2PEEK - Guc Peek Register 2

26 Doorbell #(2*32+26) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(2*32+26) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

25 Doorbell #(2*32+25) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(2*32+25) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

24 Doorbell #(2*32+24) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(2*32+24) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

23 Doorbell #(2*32+23) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(2*32+23) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

22 Doorbell #(2*32+22) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(2*32+22) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

21 Doorbell #(2*32+21) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(2*32+21) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB2PEEK - Guc Peek Register 2

20	**Doorbell #(2*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
19	**Doorbell #(2*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
18	**Doorbell #(2*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
17	**Doorbell #(2*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
16	**Doorbell #(2*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
15	**Doorbell #(2*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB2PEEK - Guc Peek Register 2

	14	**Doorbell #(2*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	13	**Doorbell #(2*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	12	**Doorbell #(2*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	11	**Doorbell #(2*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	10	**Doorbell #(2*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	9	**Doorbell #(2*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB2PEEK - Guc Peek Register 2

	8	**Doorbell #(2*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(2*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(2*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(2*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(2*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(2*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB2PEEK - Guc Peek Register 2

	2	**Doorbell #(2*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(2*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(2*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(2*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 3

DRB3PEEK - Guc Peek Register 3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0192Ch	
DWord	**Bit**	**Description**
0	31	**Doorbell #(3*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(3*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(3*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(3*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(3*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB3PEEK - Guc Peek Register 3

26 Doorbell #(3*32+26) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(3*32+26) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

25 Doorbell #(3*32+25) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(3*32+25) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

24 Doorbell #(3*32+24) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(3*32+24) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

23 Doorbell #(3*32+23) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(3*32+23) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

22 Doorbell #(3*32+22) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(3*32+22) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

21 Doorbell #(3*32+21) Guc Peek

Access:	RO
_Custom_GTIReset:	BUS

Doorbell #(3*32+21) has been rung.
Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB3PEEK - Guc Peek Register 3

	20	**Doorbell #(3*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	19	**Doorbell #(3*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	18	**Doorbell #(3*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	17	**Doorbell #(3*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	16	**Doorbell #(3*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	15	**Doorbell #(3*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB3PEEK - Guc Peek Register 3

	14	**Doorbell #(3*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	13	**Doorbell #(3*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	12	**Doorbell #(3*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	11	**Doorbell #(3*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	10	**Doorbell #(3*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	9	**Doorbell #(3*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB3PEEK - Guc Peek Register 3

8	**Doorbell #(3*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
7	**Doorbell #(3*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
6	**Doorbell #(3*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
5	**Doorbell #(3*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
4	**Doorbell #(3*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
3	**Doorbell #(3*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB3PEEK - Guc Peek Register 3

	2	**Doorbell #(3*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(3*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(3*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(3*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 4

DRB4PEEK - Guc Peek Register 4		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01930h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(4*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(4*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(4*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(4*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(4*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB4PEEK - Guc Peek Register 4

	26	**Doorbell #(4*32+26) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+26) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	25	**Doorbell #(4*32+25) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+25) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	24	**Doorbell #(4*32+24) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+24) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	23	**Doorbell #(4*32+23) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+23) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	22	**Doorbell #(4*32+22) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+22) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	21	**Doorbell #(4*32+21) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+21) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB4PEEK - Guc Peek Register 4

20	**Doorbell #(4*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
19	**Doorbell #(4*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
18	**Doorbell #(4*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
17	**Doorbell #(4*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
16	**Doorbell #(4*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
15	**Doorbell #(4*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB4PEEK - Guc Peek Register 4

14	**Doorbell #(4*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
13	**Doorbell #(4*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
12	**Doorbell #(4*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
11	**Doorbell #(4*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
10	**Doorbell #(4*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
9	**Doorbell #(4*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB4PEEK - Guc Peek Register 4

	8	**Doorbell #(4*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(4*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(4*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(4*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(4*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(4*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB4PEEK - Guc Peek Register 4

	2	**Doorbell #(4*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(4*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(4*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(4*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 5

DRB5PEEK - Guc Peek Register 5		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01934h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(5*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(5*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(5*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(5*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(5*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB5PEEK - Guc Peek Register 5

26	**Doorbell #(5*32+26) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+26) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
25	**Doorbell #(5*32+25) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+25) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
24	**Doorbell #(5*32+24) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+24) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
23	**Doorbell #(5*32+23) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+23) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
22	**Doorbell #(5*32+22) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+22) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
21	**Doorbell #(5*32+21) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+21) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB5PEEK - Guc Peek Register 5

	20	**Doorbell #(5*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	19	**Doorbell #(5*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	18	**Doorbell #(5*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	17	**Doorbell #(5*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	16	**Doorbell #(5*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	15	**Doorbell #(5*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB5PEEK - Guc Peek Register 5

14	**Doorbell #(5*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
13	**Doorbell #(5*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
12	**Doorbell #(5*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
11	**Doorbell #(5*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
10	**Doorbell #(5*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
9	**Doorbell #(5*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB5PEEK - Guc Peek Register 5

	8	**Doorbell #(5*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(5*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(5*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(5*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(5*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(5*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB5PEEK - Guc Peek Register 5

	2	**Doorbell #(5*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(5*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(5*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(5*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 6

DRB6PEEK - Guc Peek Register 6		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	01938h	
DWord	**Bit**	**Description**
0	31	**Doorbell #(6*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(6*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(6*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(6*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(6*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB6PEEK - Guc Peek Register 6

	26	**Doorbell #(6*32+26) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+26) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	25	**Doorbell #(6*32+25) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+25) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	24	**Doorbell #(6*32+24) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+24) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	23	**Doorbell #(6*32+23) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+23) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	22	**Doorbell #(6*32+22) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+22) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	21	**Doorbell #(6*32+21) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+21) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB6PEEK - Guc Peek Register 6

	20	**Doorbell #(6*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	19	**Doorbell #(6*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	18	**Doorbell #(6*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	17	**Doorbell #(6*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	16	**Doorbell #(6*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	15	**Doorbell #(6*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB6PEEK - Guc Peek Register 6

14	**Doorbell #(6*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
13	**Doorbell #(6*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
12	**Doorbell #(6*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
11	**Doorbell #(6*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
10	**Doorbell #(6*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
9	**Doorbell #(6*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB6PEEK - Guc Peek Register 6

	8	**Doorbell #(6*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(6*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(6*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(6*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(6*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(6*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB6PEEK - Guc Peek Register 6

	2	**Doorbell #(6*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(6*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(6*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(6*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

Guc Peek Register 7

DRB7PEEK - Guc Peek Register 7		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0193Ch	

DWord	Bit	Description
0	31	**Doorbell #(7*32+31) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+31) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	30	**Doorbell #(7*32+30) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+30) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	29	**Doorbell #(7*32+29) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+29) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	28	**Doorbell #(7*32+28) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+28) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	27	**Doorbell #(7*32+27) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+27) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB7PEEK - Guc Peek Register 7

	26	**Doorbell #(7*32+26) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+26) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	25	**Doorbell #(7*32+25) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+25) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	24	**Doorbell #(7*32+24) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+24) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	23	**Doorbell #(7*32+23) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+23) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	22	**Doorbell #(7*32+22) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+22) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	21	**Doorbell #(7*32+21) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+21) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB7PEEK - Guc Peek Register 7

	20	**Doorbell #(7*32+20) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+20) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	19	**Doorbell #(7*32+19) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+19) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	18	**Doorbell #(7*32+18) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+18) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	17	**Doorbell #(7*32+17) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+17) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	16	**Doorbell #(7*32+16) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+16) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	15	**Doorbell #(7*32+15) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+15) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB7PEEK - Guc Peek Register 7

	14	**Doorbell #(7*32+14) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+14) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	13	**Doorbell #(7*32+13) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+13) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	12	**Doorbell #(7*32+12) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+12) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	11	**Doorbell #(7*32+11) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+11) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	10	**Doorbell #(7*32+10) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+10) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	9	**Doorbell #(7*32+9) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+9) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB7PEEK - Guc Peek Register 7

	8	**Doorbell #(7*32+8) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+8) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	7	**Doorbell #(7*32+7) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+7) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	6	**Doorbell #(7*32+6) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+6) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	5	**Doorbell #(7*32+5) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+5) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	4	**Doorbell #(7*32+4) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+4) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	3	**Doorbell #(7*32+3) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+3) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

DRB7PEEK - Guc Peek Register 7

	2	**Doorbell #(7*32+2) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+2) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	1	**Doorbell #(7*32+1) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+1) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.
	0	**Doorbell #(7*32+0) Guc Peek** Access: RO _Custom_GTIReset: BUS Doorbell #(7*32+0) has been rung. Shadow copy of matching register in DRB*ACT, which is not cleared after a read and only echoes the register value.

GuC PM Time Stamp Counter 0

GUC_PM_TSCVALUE0 - GuC PM Time Stamp Counter 0	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

This register value shadows the GPM time stamp counter value.

Programming Notes
This value is provided locally in the GuC Shim to avoid overhead of retrieving a time stamp value from GPM unit (for e.g: latency incurred for reading the timestamp value makes the value stale).
This register is saved in the power context.

DWord	Bit	Description
0	31:0	**Time Stamp Value** Holds the lower 32 bits of the incoming time stamp counter value.

GuC PM Time Stamp Counter 1

GUC_PM_TSCVALUE1 - GuC PM Time Stamp Counter 1

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

This register value shadows the GPM time stamp counter value.

Programming Notes
This value is provided locally in the GuC Shim to avoid overhead of retrieving a time stamp value from GPM unit (for e.g: latency incurred for reading the timestamp value makes the value stale).
This register is saved in the power context.

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Format: MBZ
	3:0	**Time Stamp Value** Holds the upper 4 bits of the incoming time stamp counter value.

GU Misc Interrupt Definition

GU Misc Interrupt Definition

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS

Address:	444F0h-444FFh
Name:	Gunit Miscellaneous Interrupts
ShortName:	GU_MISC_INTERRUPT

This table indicates which events are mapped to each bit of the Gunit Miscellaneous Interrupt registers.
0x444F0 = ISR
0x444F4 = IMR
0x444F8 = IIR
0x444FC = IER

DWord	Bit	Description
0	31	**Spare_31** _Custom_GTIReset: BUS Spare bit
	30	**Spare_30** _Custom_GTIReset: BUS Spare bit
	29	**Invalid GTT page table entry** _Custom_GTIReset: BUS The ISR is an active high pulse on receiving the iMPH invalid GTT page table entry indication.
	28	**Spare_28** _Custom_GTIReset: BUS Spare bit
	27	**GSE** _Custom_GTIReset: BUS The ISR is an active high pulse on the GSE system level event.
	26	**Spare_26** _Custom_GTIReset: BUS Spare bit

GU Misc Interrupt Definition

	25	**Spare_25** _Custom_GTIReset: BUS Spare bit
	24	**Spare_24** _Custom_GTIReset: BUS Spare bit
	23	**Spare_23** _Custom_GTIReset: BUS Spare bit
	22	**SVM Device Mode PRQ Event** _Custom_GTIReset: BUS The ISR is an active high pulse on receiving the iMPH SVM Device Mode PRQ event indication. This event indicates that a GT advanced context encountered a recoverable page fault.
	21	**SVM Device Mode VTD Fault** _Custom_GTIReset: BUS The ISR is an active high pulse on receiving the iMPH SVM Device Mode VT-d fault indication. This event indicates GT encountered a non-recoverable translation fault.
	20	**SVM Device Mode Wait Descriptor Completion** _Custom_GTIReset: BUS The ISR is an active high pulse on receiving the iMPH SVM Device Mode Wait Descriptor Completion indication.This event indicates that IMPH completed Invalidation Wait Descriptor.
	19	**Spare_19** _Custom_GTIReset: BUS Spare bit
	18	**Spare_18** _Custom_GTIReset: BUS Spare bit
	17	**Spare_17** _Custom_GTIReset: BUS Spare bit

GU Misc Interrupt Definition		
	16	**Spare_16** _Custom_GTIReset: BUS Spare bit
	15	**Spare_15** _Custom_GTIReset: BUS Spare bit
	14	**Spare_14** _Custom_GTIReset: BUS Spare bit
	13	**Spare_13** _Custom_GTIReset: BUS Spare bit
	12	**Spare_12** _Custom_GTIReset: BUS Spare bit
	11	**Spare_11** _Custom_GTIReset: BUS Spare bit
	10	**Spare_10** _Custom_GTIReset: BUS Spare bit
	9	**Spare_9** _Custom_GTIReset: BUS Spare bit
	8	**Spare_8** _Custom_GTIReset: BUS Spare bit
	7	**Spare_7** _Custom_GTIReset: BUS Spare bit

GU Misc Interrupt Definition		
	6	**Spare_6** _Custom_GTIReset: BUS Spare bit
	5	**Spare_5** _Custom_GTIReset: BUS Spare bit
	4	**Spare_4** _Custom_GTIReset: BUS Spare bit
	3	**Spare_3** _Custom_GTIReset: BUS Spare bit
	2	**Spare_2** _Custom_GTIReset: BUS Spare bit
	1	**Spare_1** _Custom_GTIReset: BUS Spare bit
	0	**Spare_0** _Custom_GTIReset: BUS Spare bit

Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02098h-0209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_RCSUNIT
Address:	18098h-1809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_POCSUNIT
Address:	22098h-2209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_BCSUNIT
Address:	1C0098h-1C009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT0
Address:	1C4098h-1C409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT1
Address:	1C8098h-1C809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT0
Address:	1D0098h-1D009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT2
Address:	1D4098h-1D409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT3
Address:	1D8098h-1D809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT1
Address:	1E0098h-1E009Bh
Name:	Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register

ShortName:	HWSTAM_VCSUNIT4
Address:	1E4098h-1E409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT5
Address:	1E8098h-1E809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT2
Address:	1F0098h-1F009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT6
Address:	1F4098h-1F409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT7
Address:	1F8098h-1F809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT3
Address:	1A098h-1A09Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_CCSUNIT0

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask** Default Value: 00000000h Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO.

Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02080h-02083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_RCSUNIT
Address:	18080h-18083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_POCSUNIT
Address:	22080h-22083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_BCSUNIT
Address:	1C0080h-1C0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT0
Address:	1C4080h-1C4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT1
Address:	1C8080h-1C8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT0
Address:	1D0080h-1D0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT2
Address:	1D4080h-1D4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT3
Address:	1D8080h-1D8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT1
Address:	1E0080h-1E0083h
Name:	Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register

ShortName:	HWS_PGA_VCSUNIT4
Address:	1E4080h-1E4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT5
Address:	1E8080h-1E8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT2
Address:	1F0080h-1F0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT6
Address:	1F4080h-1F4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT7
Address:	1F8080h-1F8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT3
Address:	1A080h-1A083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_CCSUNIT0

This register is used to program the 4 KB-aligned System Memory address of the Hardware Status Page used to report hardware status into (typically cacheable) System Memory.

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] This field is used by SW to specify Bits 31:12 of the 4 KB-aligned System Memory address of the 4 KB page known as the Hardware Status Page. The Global GTT is used to map this page from the graphics virtual address to physical address. **Programming Notes** If the Per-Process Virtual Address Space and Exec List Enable bit is set, HW requires that the status page is programmed to allow for the context switch status to be reported.
	11:0	**Reserved** Access: RO Format: MBZ

HCP Bitstream Output Minimal Size Padding Count Report Register

HCP_MINSIZE_PADDING_COUNT - HCP Bitstream Output Minimal Size Padding Count Report Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9B4h

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided forstatistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**HCP MinSize Padding Count** Format: U32 Total number of bytes in the bitstream output contributing to minimal size padding operation. Thiscount is updated each time when the padding count is incremented.

HCP CABAC Status

HCP_CABAC_STATUS - HCP CABAC Status	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C2804h
ShortName:	HCP_CABAC_STATUS_VCS0
Description:	For VDBox0
Address:	1C6804h
ShortName:	HCP_CABAC_STATUS_VCS1
Description:	For VDBox1
Address:	1D2804h
ShortName:	HCP_CABAC_STATUS_VCS2
Description:	For VDBox2
Address:	1D6804h
ShortName:	HCP_CABAC_STATUS_VCS3
Description:	For VDBox3
Address:	1E2804h
ShortName:	HCP_CABAC_STATUS_VCS4
Description:	For VDBox4
Address:	1E6804h
ShortName:	HCP_CABAC_STATUS_VCS5
Description:	For VDBox5
Address:	1F2804h
ShortName:	HCP_CABAC_STATUS_VCS6
Description:	For VDBox6
Address:	1F6804h
ShortName:	HCP_CABAC_STATUS_VCS7
Description:	For VDBox7
HCP CABAC status or VP9 Decode status	

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ

HCP_CABAC_STATUS - HCP CABAC Status

	17:0	**VP9 SuperBlock Concealment Counter** Exists If: // VP9 decode = 1 Format: U18 Indicate the number of Superblock (SB) concealed by VP9 decoder (not decoded from bitstream due to error)
	11	**Temporal Direction Motion Vector Out-of-Bound Error** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates motion vectors calculated from the Temporal Direct Motion vector is larger than the allowed range for HEVC decode.
	6	**Motion Vector Delta SE** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates out-of-bound motion vector delta SEs coded in the bit-stream for HEVC decode.
	5	**Delta QP SE** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates leading-one overflow during CABAC decode of cu_qp_delta_abs for HEVC decode.
	4	**Residual Error** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates out-of-bound absolute coefficient level SEs coded in the bit-streamfor HEVC decode.

HCP_CABAC_STATUS - HCP CABAC Status

	3	**Slice and Error** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates a pre-mature end to the slice or an inconsistent end of slice on the last Ctb of a slice for HEVC decode.
	0	**HEVC Ctb Concealment Flag** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 Each pulse from this flag indicates one Ctb is concealed by the HEVC decode.

HCP Decode Status

HCP_DEC_STATUS - HCP Decode Status

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Address:	1C2800h
ShortName:	HCP_DEC_STATUS_VCS0
Description:	For VDBox0

Address:	1C6800h
ShortName:	HCP_DEC_STATUS_VCS1
Description:	For VDBox1

Address:	1D2800h
ShortName:	HCP_DEC_STATUS_VCS2
Description:	For VDBox2

Address:	1D6800h
ShortName:	HCP_DEC_STATUS_VCS3
Description:	For VDBox3

Address:	1E2800h
ShortName:	HCP_DEC_STATUS_VCS4
Description:	For VDBox4

Address:	1E6800h
ShortName:	HCP_DEC_STATUS_VCS5
Description:	For VDBox5

Address:	1F2800h
ShortName:	HCP_DEC_STATUS_VCS6
Description:	For VDBox6

Address:	1F6800h
ShortName:	HCP_DEC_STATUS_VCS7
Description:	For VDBox7

HCP Decode status.

DWord	Bit	Description
0	31:18	**Number of Ctbs Concealed** Default Value: 0 Format: U14 This 14-bit field indicates the number of Ctbs concealed during the decoding of the current frame. This field is cleared with the HCP_PIPE_MODE_SELECT command.

HCP_DEC_STATUS - HCP Decode Status

	17	**Frame Dec Active** Default Value: 0 Format: U1 This flag indicates that the decoder hardware is actively decoding a picture.
	16	**Indirect Bitstream ObjectAccess Upper Bound Error** Default Value: 0 Format: U1 This flag indicates that the upper bound bit-stream address was reached.
	15:0	**Bit-stream Error Flags** Default Value: 0 Format: U16 This 16-bit field indicates the number of bit stream errors detected for each bit fieldindicated in the CABAC Status register.

HCP Frame BitStream BIN Count

HCP_BIN_CT - HCP Frame BitStream BIN Count

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E980h

This register stores the number of BINs decoded in a frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**HCP Frame Bit-stream BIN Count** Default Value: 723ba5c0h Format: U32 Total number of BINs decoded/ in current frame. This number is used with frame performance count to derive Bin/clk.

HCP Image Status Control

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1C28BCh

DWord	Bit	Description
0	31:24	**Cumulative Frame Delta QP/QIndex** Format: S7 Used for Frame Level Multi-pass Rate Control.HEVC: cu_qp = input (first pass) cu_qp + Cumulative Frame Delta Qp. Pak does clamping to max value based on bitdepth. Bit31 is the sign bit. VP9: cu_qindex = input (first pass) cu_qindex + Cumulative Frame Delta Qindex. Pak does clamping to -127..127 after adding. Bit31 is the sign bit. VDENC: In VDenc mode this value is added even in first pass (always)so the recommendation is to set this value to zero in first pass
	23	**Reserved** Access: RO Format: MBZ
	22:16	**Cumulative Frame Delta LF** Access: RO Format: S6 Used for Frame Level Multi-pass Rate Control. LF_level = input (first pass) LF_level + Cumulative Frame Delta LF level. Pak does clamping to -63..63 after adding.
	15:12	**Reserved** Access: RO Format: MBZ
	11:8	**Total Num-Pass** Format: U4
	7:3	**Reserved** Access: RO Format: MBZ
	2	**Frame Bit Count Violate - under run** Access: RO Format: U1 This can trigger Frame Level Multi-pass Rate Control.Set to 1 if frame bit count is less than or equal to FrameBitRateMin

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control		
	1	**Frame Bit Count Violate - over run** Access: RO Format: U1 This can trigger Frame Level Multi-pass Rate Control.Set to 1 if frame bit count is less than or equal to FrameBitRateMax
	0	**LCU Bit Count Violate- overrun**

HCP Image Status Mask

HCP_IMAGE_STATUS_MASK - HCP Image Status Mask		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1E9B8h	
This register stores the image status(flags).		

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2	**FrameBitRateMinReportMask** Same as **FrameSzUnderStatusEn** in HCP_PIC_STATE.
	1	**FrameBitRateMaxReportMask** Same as **FrameSzOverStatusEn** in HCP_PIC_STATE.
	0	**FrameLcuMaxReportMask**

HCP Last Position

HCP_LAST_POSITION - HCP Last Position

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C2808h
ShortName:	HCP_LAST_POSITION_VCS0
Description:	For VDBox0
Address:	1C6808h
ShortName:	HCP_LAST_POSITION_VCS1
Description:	For VDBox1
Address:	1D2808h
ShortName:	HCP_LAST_POSITION_VCS2
Description:	For VDBox2
Address:	1D6808h
ShortName:	HCP_LAST_POSITION_VCS3
Description:	For VDBox3
Address:	1E2808h
ShortName:	HCP_LAST_POSITION_VCS4
Description:	For VDBox4
Address:	1E6808h
ShortName:	HCP_LAST_POSITION_VCS5
Description:	For VDBox5
Address:	1F2808h
ShortName:	HCP_LAST_POSITION_VCS6
Description:	For VDBox6
Address:	1F6808h
ShortName:	HCP_LAST_POSITION_VCS7
Description:	For VDBox7

Last row and column position of the decoder.

- The HCP Last Position register reports the position of the last Ctb to be decoded by the HCP hardware.
- It can be reset to 0H with the HCP_PIPE_MODE_SELECT command.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO

HCP_LAST_POSITION - HCP Last Position

		Format: MBZ
	24:16	**Last Row Position in Ctbs** Default Value: 0 Access: RO Format: U9
	15:9	**Reserved** Access: RO Format: MBZ
	8:0	**Last Column Position in Ctbs** Default Value: 0 Access: RO Format: U9

HCP Picture Checksum cIdx0

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cIdx0	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C281Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS0
Description:	For VDBox0
Address:	1C681Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS1
Description:	For VDBox1
Address:	1D281Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS2
Description:	For VDBox2
Address:	1D681Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS3
Description:	For VDBox3
Address:	1E281Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS4
Description:	For VDBox4
Address:	1E681Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS5
Description:	For VDBox5
Address:	1F281Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS6
Description:	For VDBox6
Address:	1F681Ch
ShortName:	HCP_PICTURE_CHECKSUM_CIDX0_VCS7
Description:	For VDBox7

- The HCP Picture Checksum cIdx0 register reports the 32-bit unsigned picture checksum for cIdx=0 calculatedby the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx0**

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cIdx0			
		Default Value:	0
		Format:	U32

HCP Picture Checksum cIdx1

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cIdx1	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C2820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS0
Description:	For VDBox0
Address:	1C6820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS1
Description:	For VDBox1
Address:	1D2820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS2
Description:	For VDBox2
Address:	1D6820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS3
Description:	For VDBox3
Address:	1E2820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS4
Description:	For VDBox4
Address:	1E6820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS5
Description:	For VDBox5
Address:	1F2820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS6
Description:	For VDBox6
Address:	1F6820h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX1_VCS7
Description:	For VDBox7

- The HCP Picture Checksum cIdx1 register reports the 32-bit unsigned picture checksum for cIdx=1 calculatedby the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx1**

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cIdx1			
		Default Value:	0
		Format:	U32

HCP Picture Checksum cIdx2

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cIdx2	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C2824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS0
Description:	For VDBox0
Address:	1C6824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS1
Description:	For VDBox1
Address:	1D2824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS2
Description:	For VDBox2
Address:	1D6824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS3
Description:	For VDBox3
Address:	1E2824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS4
Description:	For VDBox4
Address:	1E6824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS5
Description:	For VDBox5
Address:	1F2824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS6
Description:	For VDBox6
Address:	1F6824h
ShortName:	HCP_PICTURE_CHECKSUM_CIDX2_VCS7
Description:	For VDBox7

- The HCP Picture Checksum cIdx2 register reports the 32-bit unsigned picture checksum for cIdx=2 calculatedby the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx2**

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cIdx2			
		Default Value:	0
		Format:	U32

HCP PMU Status

HCP_PMU_STATUS - HCP PMU Status	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C280Ch
ShortName:	HCP_PMU_STATUS_VCS0
Description:	For VDBox0
Address:	1C680Ch
ShortName:	HCP_PMU_STATUS_VCS1
Description:	For VDBox1
Address:	1D280Ch
ShortName:	HCP_PMU_STATUS_VCS2
Description:	For VDBox2
Address:	1D680Ch
ShortName:	HCP_PMU_STATUS_VCS3
Description:	For VDBox3
Address:	1E280Ch
ShortName:	HCP_PMU_STATUS_VCS4
Description:	For VDBox4
Address:	1E680Ch
ShortName:	HCP_PMU_STATUS_VCS5
Description:	For VDBox5
Address:	1F280Ch
ShortName:	HCP_PMU_STATUS_VCS6
Description:	For VDBox6
Address:	1F680Ch
ShortName:	HCP_PMU_STATUS_VCS7
Description:	For VDBox7

PMU counter overflow status.

- The HCP PMU Status register reports the overflow status of the HCP PMU Luma Cache Miss Counter,the HCP PMU Chroma cache Miss Counter and the HCP Frame Decode Active Counter.
- It can be reset to 0H with the HCP_PIPE_MODE_SELECT command.

DWord	Bit	Description
0	31:3	**Reserved**

HCP_PMU_STATUS - HCP PMU Status

Access:	RO
Format:	MBZ

2 Event Counter Overflow - Frame Decode Active

Access:	RO
Format:	U1

Value	Name
1	Counter overflow
0	Non-Active **[Default]**

1 Event Counter Overflow - Chroma Cache Miss

Access:	RO
Format:	U1

Value	Name
1	Counter overflow
0	Non-Active **[Default]**

0 Event Counter Overflow - Luma Cache Miss

Access:	RO
Format:	U1

Value	Name
1	Counter overflow
0	Non-Active **[Default]**

HCP Power Context Save request

HCPPGCTXREQ - HCP Power Context Save request

Register Space: MMIO: 0/2/0

Size (in bits): 32

DWord	Bit	Description
0	31:16	**Reserved**
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

HCP Power Down FSM control register with lock

HCPSPCPOWERDNFSMCTL - HCP Power Down FSM control register with lock

Register Space: MMIO: 0/2/0

Size (in bits): 32

DWord	Bit	Description
0	31	**Reserved**
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow

HCPSPCPOWERDNFSMCTL - HCP Power Down FSM control register with lock

	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
	8:0	**Reserved** Access: RO Format: MBZ

HCP Power Gate Control Request

HCPPGCTLREQ - HCP Power Gate Control Request

Register Space: MMIO: 0/2/0

Size (in bits): 32

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Reserved**
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS HCP CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS HCP power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

HCP Qp Status Count

HCP_QP_STATUS_COUNT - HCP Qp Status Count		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	64	
Address:	1E9C0h	

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Cumulative QP** Format: U24 Cumulative QP for all LCU of a Frame (Can be used for computing average QP).
1	31:15	**Reserved** Access: RO Format: MBZ
	14:8	**Frame Max CU QP** Format: U7 Valid Range: 0-51 for 8bit, 0-63 for 10bit and 0-75 for 12bit
	7	**Reserved** Access: RO Format: MBZ
	6:0	**Frame Min CU QP** Format: U7 Valid Range: 0-51 for 8bit and 0-63 for 10bit range 0-75 for 12bit

HCP Reported Bitstream Output Byte Count with header per Frame Register

HCP_BITSTREAM_BYTECOUNT_FRAME_WITH_HEADER - HCP Reported Bitstream Output Byte Count with header per Frame Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9A0h

DWord	Bit	Description
0	31:0	**HCP Bitstream Byte Count per Frame With header** Format: U32 Total number of bytes in the bitstream output per frame from the encoder. This includes header, optional tail, byte alignment, data bytes, EMU (emulation) bytes, capac-zero word insertion, and padding insertion. The optional header/optional tail includes all bits accumulated for PAK_INSERT_COMMAND when HeaderLenghtExcludeFrmSize is set to 0 and it does NOT include all bits generated by PAK_INSERT_COMMAND when HeaderLenghtExcludeFrmSize is set to 1. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

HCP Reported Bitstream Output Byte Count without header per Frame Register

HCP_BITSTREAM_BYTECOUNT_FRAME_NO_HEADER - HCP Reported Bitstream Output Byte Count without header per Frame Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9A4h

DWord	Bit	Description
0	31:0	**HCP Bitstream Byte Count per Frame Without header** Format: U32 Total number of bytes in the bitstream output per frame from the encoder. This includes optional header, optional tail, byte alignment, data bytes, EMU (emulation) bytes, capac-zero word insertion, and padding insertion. The optional header/optional tail includes all bits accumulated for PAK_INSERT_COMMAND when HeaderLenghtExcludeFrmSize is set to 0 and it does NOT include all bits generated by PAK_INSERT_COMMAND when HeaderLenghtExcludeFrmSize is set to 1. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

HCP Reported Bitstream Output CABAC Bin Count Register

HCP_CABAC_BIN_COUNT_FRAME - HCP Reported Bitstream Output CABAC Bin Count Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9ACh

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**HCP Cabac Bin Count** Default Value: 0 Format: U32 Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

HCP SLICE COUNT

HCP_SLICE_COUNT - HCP SLICE COUNT

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9C8h

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**Slice Count** Format: U20 Indicates Number of Slices in a Frame.

HCP Unit Done

HCP_UNIT_DONE - HCP Unit Done	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C28D8h
ShortName:	HCP_UNIT_DONE_VCS0
Description:	For VDBox0
Address:	1C68D8h
ShortName:	HCP_UNIT_DONE_VCS1
Description:	For VDBox1
Address:	1D28D8h
ShortName:	HCP_UNIT_DONE_VCS2
Description:	For VDBox2
Address:	1D68D8h
ShortName:	HCP_UNIT_DONE_VCS3
Description:	For VDBox3
Address:	1E28D8h
ShortName:	HCP_UNIT_DONE_VCS4
Description:	For VDBox4
Address:	1E68D8h
ShortName:	HCP_UNIT_DONE_VCS5
Description:	For VDBox5
Address:	1F28D8h
ShortName:	HCP_UNIT_DONE_VCS6
Description:	For VDBox6
Address:	1F68D8h
ShortName:	HCP_UNIT_DONE_VCS7
Description:	For VDBox7

Unit Done Signals.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ

HCP_UNIT_DONE - HCP Unit Done

	25	**SFI unit Done** Format: U1
	24	**HFC unit Done** Format: U1
	23	**HSF unit Done** Format: U1
	22	**VHLF unit Done** Format: U1
	21	**HHLF unit Done** Format: U1
	20	**HED unit Done** Format: U1
	19	**HVD unit Done** Format: U1
	18	**HPP unit Done** Format: U1
	17	**HMC unit Done** Format: U1
	16	**HIT unit Done** Format: U1
	15	**HPR unit Done** Format: U1
	14	**HFE unit Done** Format: U1
	13	**HBE unit Done** Format: U1
	12	**HMXF unit Done** Format: U1
	11	**HMXB unit Done** Format: U1
	10	**HTQunit Done** Format: U1
	9	**HSSE unit Done** Format: U1
	8	**VNC unit done** Format: U1

HCP_UNIT_DONE - HCP Unit Done		
	7	**VNE unit done** Format: U1
	6	**HSAO Unit Done** Format: U1
	5	**HLC unit done** Format: U1
	4	**HLE unit done** Format: U1
	3	**HFQ unit done** Format: U1
	2	**HFT unit done** Format: U1
	1	**HRS unit done** Format: U1
	0	**HPO unit done** Format: U1

Header Type

HDR2_0_2_0_PCI - Header Type		
Register Space: PCI: 0/2/0 Size (in bits): 8		
Address: 0000Eh		
This register contains the Header Type of the IGD.		
DWord	**Bit**	**Description**
0	7	**Multi Function Status** Default Value: 0b Access: RO _Custom_GTIReset: BUS Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
	6:0	**Header Code** Default Value: 0000000b Access: RO _Custom_GTIReset: BUS This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

Head pointer update

HEAD_PTR_UPDATE - Head pointer update	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1C2D90h-1C2D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG0
Address:	1C6D90h-1C6D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG1
Address:	1D2D90h-1D2D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG2
Address:	1D6D90h-1D6D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG3
Address:	1E2D90h-1E2D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG4
Address:	1E6D90h-1E6D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG5
Address:	1F2D90h-1F2D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG6
Address:	1F6D90h-1F6D93h
Name:	Head pointer Update
ShortName:	HEAD_PTR_UPDATE_VDENC_REG7

A write to this register with a value of 1 would result in head pointer update to Display.

DWord	Bit	Description
0	31:1	**Head pointer value** Access: R/W Hardware Clear The head pointer value is read only value. It is updated by HW.

HEAD_PTR_UPDATE - Head pointer update

	0	**Head pointer update enable** Access: R/W Hardware Clear This bit can be written with a value of 0 or 1. A write with 0 is ignored. A write with 1 would result in head pointer update to display if VDEnc is in WiDi session. While reading this bit always results zero. Head pointer update is achieved by performing config write to address 2005_0500 for widi session 0 when Capture Mode = 0, VDENC_PIPE_MODE_SELECT, DW 5. Head pointer update is achieved by performing config write to address 2005_0600 for widi session 1 when Capture Mode = 0, VDENC_PIPE_MODE_SELECT, DW 5. Head pointer update is achieved by performing config write to address 2024_2000 for widi session 0 when Capture Mode = 1, VDENC_PIPE_MODE_SELECT, DW 5. Head pointer update is achieved by performing config write to address 2024_2004 for widi session 1 when Capture Mode = 1, VDENC_PIPE_MODE_SELECT, DW 5. Head pointer update is achieved by performing config write to address 2024_2008 for widi session 2 when Capture Mode = 1, VDENC_PIPE_MODE_SELECT, DW 5. Head pointer update is achieved by performing config write to address 2024_200C for widi session 3 when Capture Mode = 1, VDENC_PIPE_MODE_SELECT, DW 5. Data format: 31:28 Zeros. 27:20 Tile number 19:16 Frame number (only bit 0 is used by HW) 15:0 Tail pointer pointing to pixel row.

HEVC Local APIC Retry Vector

HEVC_LAPIC_RETRY_VECT - HEVC Local APIC Retry Vector

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0D594h

Holds the 4 last retry interrupt vectors. The retry vector register holds the last 4 values acknowledged as an interrupt retry. Retries are errors in hardware and are not expected. HUCINT handles retries by logging the interrupt vector in this register. No interrupt is actually retried, and the interrupt stimulus will be lost if a retry occurs. The system will hang eventually. A 2-bit counter (starting at reset value of 0) is used to point to the slot/byte location from which to load the next retry vector (into the 4 available slots) in sequence. This means if a 5th retry vector shows up, it will be loaded into slot 0 again (as the counter wraps around), over-writing the retry vector which existed there in slot_0.

DWord	Bit	Description
0	31:24	**Vector Slot 3** Format: U8
	23:16	**Vector Slot 2** Format: U8
	15:8	**Vector Slot 1** Format: U8
	7:0	**Vector Slot 0** Format: U8

HIP_INDEX_REG0

HIP_INDEX_REG0 - HIP_INDEX_REG0		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	1010A0h	
DWord	**Bit**	**Description**
0	31:24	**HIP_16B_Index** _Custom_GTIReset: BUS Bits 27:24 provide a 4KB index window for the GTTMMADR[16_B000h to 16_BFFFh] decode range. Bits 31:28 are reserved.
	23:16	**HIP_16A_Index** _Custom_GTIReset: BUS Bits 19:16 provide a 4KB index window for the GTTMMADR[16_A000h to 16_AFFFh] decode range. Bits 23:20 are reserved.
	15:8	**HIP_169_Index** _Custom_GTIReset: BUS Bits 11:8 provide a 4KB index window for the GTTMMADR[16_9000h to 16_9FFFh] decode range. Bits 15:12 are reserved.
	7:0	**HIP_168_Index** _Custom_GTIReset: BUS Bits 3:0 provide a 4KB index window for the GTTMMADR[16_8000h to 16_8FFFh] decode range. Bits 7:4 are reserved.

HIP_INDEX_REG1

HIP_INDEX_REG1 - HIP_INDEX_REG1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	1010A4h	
DWord	**Bit**	**Description**
0	31:24	**HIP_16F_Index** _Custom_GTIReset: BUS Bits 27:24 provide a 4KB index window for the GTTMMADR[16_F000h to 16_FFFFh] decode range. Bits 31:28 are reserved.
	23:16	**HIP_16E_Index** _Custom_GTIReset: BUS Bits 19:16 provide a 4KB index window for the GTTMMADR[16_E000h to 16_EFFFh] decode range. Bits 23:20 are reserved.
	15:8	**HIP_16D_Index** _Custom_GTIReset: BUS Bits 11:8 provide a 4KB index window for the GTTMMADR[16_D000h to 16_DFFFh] decode range. Bits 15:12 are reserved.
	7:0	**HIP_16C_Index** _Custom_GTIReset: BUS Bits 3:0 provide a 4KB index window for the GTTMMADR[16_C000h to 16_CFFFh] decode range. Bits 7:4 are reserved.

HOTPLUG_CTL

HOTPLUG_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44030h-44033h
Name:	Thunderbolt Hot Plug Control
ShortName:	TBT_HOTPLUG_CTL
Reset:	soft
Address:	44038h-4403Bh
Name:	Type-C Hot Plug Control
ShortName:	TC_HOTPLUG_CTL
Reset:	soft

DWord	Bit	Description
0	31	**Port8 HPD Enable** Value: 0b – Disable Value: 1b – Enable
	30	**Reserved** Access: RO Format: MBZ
	29:28	**Port8 HPD Status** Access: R/WC Value: 00b – Hot plug event not detected Value: 01b – Short pulse detected Value: 10b – Long pulse detected Value: 11b – Short and long pulses detected
	27	**Port7 HPD Enable** Value: 0b – Disable Value: 1b – Enable
	26	**Reserved** Access: RO Format: MBZ

HOTPLUG_CTL

25:24	**Port7 HPD Status** Access: R/WC Value: 00b — Hot plug event not detected Value: 01b — Short pulse detected Value: 10b — Long pulse detected Value: 11b — Short and long pulses detected
23	**Port6 HPD Enable** Value: 0b — Disable Value: 1b — Enable
22	**Reserved** Access: RO Format: MBZ
21:20	**Port6 HPD Status** Access: R/WC Value: 00b — Hot plug event not detected Value: 01b — Short pulse detected Value: 10b — Long pulse detected Value: 11b — Short and long pulses detected
19	**Port5 HPD Enable** Value: 0b — Disable Value: 1b — Enable
18	**Reserved** Access: RO Format: MBZ
17:16	**Port5 HPD Status** Access: R/WC Value: 00b — Hot plug event not detected Value: 01b — Short pulse detected Value: 10b — Long pulse detected

HOTPLUG_CTL

		11b: Short and long pulses detected
	15	**Port4 HPD Enable** 0b: Disable 1b: Enable
	14	**Reserved** Access: RO Format: MBZ
	13:12	**Port4 HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	11	**Port3 HPD Enable** 0b: Disable 1b: Enable
	10	**Reserved** Access: RO Format: MBZ
	9:8	**Port3 HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	7	**Port2 HPD Enable** 0b: Disable 1b: Enable

HOTPLUG_CTL

	6	**Reserved** Access: RO Format: MBZ
	5:4	**Port2 HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	3	**Port1 HPD Enable** 0b: Disable 1b: Enable
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Port1 HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02300h
Name:	HS Invocation Counter
ShortName:	HS_INVOCATION_COUNT

This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology).This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**HS Invocation Count UDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS
	31:0	**HS Invocation Count LDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02310h-02317h
Name:	IA Vertices Count
ShortName:	IA_VERTICES_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18310h-18317h
Name:	IA Vertices Count
ShortName:	IA_VERTICES_COUNT_POCSUNIT_BE_GEOMETRY

This register stores the count of vertices processed by VF. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**IA Vertices Count Report UDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Vertices Count Report LDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

Idle Switch Delay

IDLEDLY - Idle Switch Delay	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0223Ch-0223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_RCSUNIT
Address:	1823Ch-1823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_POCSUNIT
Address:	2223Ch-2223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_BCSUNIT
Address:	1C023Ch-1C023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT0
Address:	1C423Ch-1C423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT1
Address:	1C823Ch-1C823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT0
Address:	1D023Ch-1D023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT2
Address:	1D423Ch-1D423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT3
Address:	1D823Ch-1D823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT1
Address:	1E023Ch-1E023Fh
Name:	Idle Switch Delay

IDLEDLY - Idle Switch Delay

ShortName:	IDLEDLY_VCSUNIT4
Address:	1E423Ch-1E423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT5
Address:	1E823Ch-1E823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT2
Address:	1F023Ch-1F023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT6
Address:	1F423Ch-1F423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT7
Address:	1F823Ch-1F823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT3
Address:	1A23Ch-1A23Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_CCSUNIT0

The IDLEDLY register contains an Idle Delay field which specifies eight times the time stamp base units allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. Refer Time Stamp Bases subsection in Power Management chapter for time stamp base unit granularity. Example: An IDLE Delay count of 2 with Time stamp base unit value of 80ns would mean an idle delay wait of 1280ns (2*8*80). A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:0	**IDLE Delay** Format: U21 Eight times the time stamp base units allowed. Refer Time Stamp Bases subsection in Power Management chapter for time stamp base unit granularity. Example: An IDLE Delay count of 2 with Time stamp base unit value of 80ns would mean an idle delay wait of 1280ns (2*8*80).

Indirect Context Offset Pointer

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	021C8h-021CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_RCSUNIT
Address:	181C8h-181CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_POCSUNIT
Address:	221C8h-221CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_BCSUNIT
Address:	1C01C8h-1C01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT0
Address:	1C41C8h-1C41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT1
Address:	1C81C8h-1C81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT0
Address:	1D01C8h-1D01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT2
Address:	1D41C8h-1D41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT3
Address:	1D81C8h-1D81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT1
Address:	1E01C8h-1E01CBh
Name:	Indirect Context Offset Pointer

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT4
Address:	1E41C8h-1E41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT5
Address:	1E81C8h-1E81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT2
Address:	1F01C8h-1F01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT6
Address:	1F41C8h-1F41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT7
Address:	1F81C8h-1F81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT3
Address:	1A1C8h-1A1CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_CCSUNIT0

This register is used to program the offset where commands RCS_INDIRECT_CTX points to will be executed as part of engine context restore.

Programming Notes

- BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS/PositionCS: This register functionality is not supported and must not be programmed for these command streamers.
- Offset of Indirect CS context must be always programmed to a command boundary and cacheline boundary inside the context image.
- Indirect context pointer itself is restored during context restore and hence Indirect Context Offset must not be programmed with value less than 0x5.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:6	**Offset of Indirect CS Context** Format: U10 This is the cache line offset for the Indirect CS context. This defaults to execute between CS and SVG context. It is not valid to program this to a value that is greater or equal to the starting offset for RS context. If context must be programmed at the end of engine context then program

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

		then use BB_PER_CTX_PTR. **Value** / **Name** 0Dh / **[Default]**
	5:0	**Reserved** Access: RO Format: MBZ

Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	021C4h-021C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_RCSUNIT
Address:	181C4h-181C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_POCSUNIT
Address:	221C4h-221C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_BCSUNIT
Address:	1C01C4h-1C01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT0
Address:	1C41C4h-1C41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT1
Address:	1C81C4h-1C81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT0
Address:	1D01C4h-1D01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT2
Address:	1D41C4h-1D41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT3
Address:	1D81C4h-1D81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT1
Address:	1E01C4h-1E01C7h
Name:	Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer

ShortName:	INDIRECT_CTX_VCSUNIT4
Address:	1E41C4h-1E41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT5
Address:	1E81C4h-1E81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT2
Address:	1F01C4h-1F01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT6
Address:	1F41C4h-1F41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT7
Address:	1F81C4h-1F81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT3
Address:	1A1C4h-1A1C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_CCSUNIT0

This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.

Programming Notes

BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS/PositionCS: This register functionality is not supported and must not be programmed for these command streamers.

The following commands are not supported within Render CS indirect context:

Command Name
MI_WAIT_FOR_EVENT
MI_ARB_CHECK
MI_REPORT_HEAD
MI_TOPOLOGY_FILTER
MI_SET_CONTEXT
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported. MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END

INDIRECT_CTX - Indirect Context Pointer

GPGPU_WALKER
3DPRIMITIVE
MI_BATCH_BUFFER_END

DWord	Bit	Description
0	31:6	**Indirect CS Context Address** Format: GraphicsAddress[31:6] Pointer to the Context in memory to be executed as a batch.
	5:0	**Size of Indirect CS Context** Format: U6 This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled. Value: [0,63] Name:

infcp Vdbox unit Level Clock Gating override during rstflow

INFMISCCP9568 - infcp Vdbox unit Level Clock Gating override during rstflow

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09568h

Micellaneous Clocking Config Bits

DWord	Bit	Description
0	31	**Reserved**
	30:0	**Reserved** Access: RO Format: MBZ

INF Power Context Save request

INFCGCTL9564 - INF Power Context Save request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09564h

DWord	Bit	Description
0	31:16	**Reserved**
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

INF unit Level Clock Gating Control 9560

INFCGCTL9560 - INF unit Level Clock Gating Control 9560

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 09560h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16:10	**Reserved** Access: RO Format: MBZ
	9	**Reserved**
	8	**SnoopFilter Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS **Description** Snoop filter Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Value** / **Name** 1b / **[Default]**
	7:0	**Reserved** Access: RO Format: MBZ

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020C0h-020C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_RCSUNIT
Address:	180C0h-180C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_POCSUNIT
Address:	220C0h-220C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_BCSUNIT
Address:	1C00C0h-1C00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT0
Address:	1C40C0h-1C40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT1
Address:	1C80C0h-1C80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT0
Address:	1D00C0h-1D00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT2
Address:	1D40C0h-1D40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT3
Address:	1D80C0h-1D80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT1
Address:	1E00C0h-1E00C3h
Name:	Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register

ShortName:	INSTPM_VCSUNIT4
Address:	1E40C0h-1E40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT5
Address:	1E80C0h-1E80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT2
Address:	1F00C0h-1F00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT6
Address:	1F40C0h-1F40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT7
Address:	1F80C0h-1F80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT3
Address:	1A0C0h-1A0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_CCSUNIT0

The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes

- If an instruction type is disabled, the parser will read those instructions but not process them.
- Error checking will be performed even if the instruction is ignored.
- All Reserved bits are implemented.
- This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.

INSTPM - Instruction Parser Mode Register

15 — Register Poll Mode Semaphore Wait Event IDLE message Disable

This bit controls the DOP CG behavior of CS while waiting for pending semaphore wait for event to be satisfied in register poll mode of operation.

Value	Name	Description
0	**[Default]**	When Rest, CS trigger DOP CG on an unsuccessful semaphore wait in register poll mode of operation.
1		When Set, CS doesn't trigger DOP CG on an unsuccessful semaphore wait in register poll mode of operation.

14 — Ignore Posh Start and Posh Enable fields in Batch Start command

Source:	RenderCS, PositionCS

This bit controls the execution of ring buffers and batch buffer by PositionCS and RenderCS.

Value	Name	Description
0	**[Default]**	PositonCS and RenderCS consider the Posh Start and Posh Enable fields programmed in the MI_BATCH_BUFFER_START command and execute accordingly. PositionCS parses (doesnt execute) the commands programmed in the ring buffer.
1		PositonCS and RenderCS ignores the Posh Start and Posh Enable fields programmed in the MI_BATCH_BUFFER_START command. PositionCS executes all the commands programmed in the ring buffer and the batch buffers.

13 — Enable Semaphore Register Poll Mask

This bit enables masking of the register data red prior to semaphore comparison on a register poll mode.

Value	Name	Description
1		In register poll mode of operation Semaphore Address Upper Dword will be used as mask and applied to the data red form the register prior to comparison. Mask Bit Set to 0 indicate the corresponding bit red from the register is considered as it is unmodified for comparison. Mask Bit Set to 1 indicate the corresponding bit red from the register is forced to 0 for comparison.
0	**[Default]**	Regular comparison with no mask applied.

12 — PreFetch Disable Status

This bit gets programmed on executing MI_ARB_CHK command with mask bit set for Pre-Fetch Disable. This bit is used to context save/restore the Pre-Fetch Disable status on a context switch. This bit must not be directly written by software.

11 — CLFLUSH Toggle

Source:	RenderCS, PositionCS
Access:	RO
Format:	U1

INSTPM - Instruction Parser Mode Register		
		This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.
	10	**Reserved**
	9:0	**Reserved** Access: RO Format: MBZ

Interrupt Group 0

INTR_GROUP_0 - Interrupt Group 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

The two Interrupt Group Registers (0 and 1) use their total 64 bits to map 16 groups to 16 base values (14 of which are currently used, 13 used prior) within the 256-bit interrupt vector. Each group (8 per register) is assigned a 4-bit value that specifies its position in the 256 vector.
The position of an interrupt within a group of 16 interrupts (as assigned by the group value) is HW determined. Groups with a single interrupt use the highest possible encoding (0XF), groups with multiple interrupts use a HW encoding as specified. Since Doorbell interrupts may use the same group value for more than one group of interrupts, each doorbell interrupt is assigned (by HW) a unique position in each group of 16. In other words, even though Doorbell groups have a single interrupt each, these do not all use the highest possible encoding, the encoding is as specified.
A value of 0 turns off that entire group of interrupts.

Programming Notes
When programmed to send doorbell interrupts to Host, only one group of 32 doorbells may be enabled. All other (seven) doorbell groups MUST be disabled by making their group value 0.
This register is saved in the power context

DWord	Bit	Description
0	31:28	**Doorbell Group 7** Interrupt vector group (dword index) for doorbell group 7, which covers input doorbells 224 through 255 Encoding: 0XF
	27:24	**Doorbell Group 6** Interrupt vector group (dword index) for doorbell group 6, which covers input doorbells 192 through 223 Encoding: 0XE
	23:20	**Doorbell Group 5** Interrupt vector group (dword index) for doorbell group 5, which covers input doorbells 160 through 191 Encoding: 0XD
	19:16	**Doorbell Group 4** Interrupt vector group (dword index) for doorbell group 4, which covers input doorbells 128 through 159 Encoding: 0XC
	15:12	**Doorbell Group 3** Interrupt vector group (dword index) for doorbell group 3, which covers input doorbells 96 through 127 Encoding: 0XB

INTR_GROUP_0 - Interrupt Group 0		
	11:8	**Doorbell Group 2** Interrupt vector group (dword index) for doorbell group 2, which covers input doorbells 64 through 95 Encoding: 0XA
	7:4	**Doorbell Group 1** Interrupt vector group (dword index) for doorbell group 1, which covers input doorbells 32 through 63 Encoding: 0X9
	3:0	**Doorbell Group 0** Interrupt vector group (dword index) for doorbell group 0, which covers input doorbells 0 through 31 Encoding: 0X8

Interrupt Group 1

INTR_GROUP_1 - Interrupt Group 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

The two Interrupt Group Registers (0 and 1) use their total 64 bits to map 16 groups to 16 base values (14 of which are currently used, 13 used prior) within the 256-bit interrupt vector. Each group (8 per register) is assigned a 4-bit value that specifies its position in the 256 vector.
The position of an interrupt within a group of 16 interrupts (as assigned by the group value) is HW determined. Groups with a single interrupt use the highest possible encoding (0XF), groups with multiple interrupts use a HW encoding as specified.
Since Doorbell interrupts may use the same group value for more than one group of interrupts, each doorbell interrupt is assigned (by HW) a unique position in each group of 16. In other words, even though Doorbell groups have a single interrupt each, these do not all use the highest possible encoding, the encoding is as specified.
A value of 0 turns off that entire group of interrupts.

Programming Notes
This register is saved in the power context

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:20	**Host Group** Interrupt vector group for Host. Encoding (see description above) used: 0xF
	19:16	**DMA/Timer/FLR Group** Interrupt vector group (dword index) for the DMA, Timer, FLR group. Encoding (see description above): FLR= 0XD, Timer = 0xE, DMA = 0xF
	15:12	**Display Events Group** Interrupt vector group (dword index) for display events Encoding (see description above): Solicited = 0XF Unsolicited = 0XE
	11:8	**IOMMU Interrupts Group** Interrupt vector group (dword index) for IOMMU interrupts Encoding (see description above): GuC Catastrophic Error = 0xF, Non GuC Catastrophic errors = 0XC, Page Faults = 0XB, Page Response = 0XA
	7:4	**Semaphore Group** Description Interrupt vector group (dword index) for semaphores Encoding of interrupts: VF0 = 0xF, VF1 = 0xE, VF2 = 0xD, VF3 = 0xC, VF4 = 0xB, VF5 = 0xA, VF6 = 0x9, VF7 = 0x8

INTR_GROUP_1 - Interrupt Group 1		
	3:0	**Engine Interrupts Group** Interrupt vector group (dword index) for engine interrupts Encoding: INTDW0 = 0XF, INTDW1 = 0XE

Interrupt Line

INTRLINE_0_2_0_PCI - Interrupt Line		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0003Ch	
This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.		
DWord	**Bit**	**Description**
0	7:0	**Interrupt Connection** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

Interrupt Pin

INTRPIN_0_2_0_PCI - Interrupt Pin		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0003Dh	
This register tells which interrupt pin the device uses.		
DWord	**Bit**	**Description**
0	7:0	**Interrupt Pin Value** Default Value: 00000001b Access: RO _Custom_GTIReset: BUS As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.

I/O Base Address

IOBAR_0_2_0_PCI - I/O Base Address

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00020h

This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms.Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:6	**IO Base Address** Default Value: 0000000000b Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [15:6].
	5:3	**Reserved** Access: RO Format: MBZ
	2:1	**Memory Type** Default Value: 00b Access: RO _Custom_GTIReset: BUS Hardwired to 0s to indicate 32-bit address.
	0	**Memory/IO Space** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to "1" to indicate IO space.

Jump Location

JMP_DEST - Jump Location

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

The Jump Location used by HW shall be in DW1 of the last Cacheline. The 32 bits are split up into two fields: one to specify the uOS load location, another to specify where in the uOS image to jump to. BootROMs shall use the 2 fields to compute uOS jump point.

Programming Notes

This register is saved in the power context

DWord	Bit	Description
0	31:18	**uOS Intended Base** Default Value: 0h Indicate the location at which uOS shall be loaded. BootROM shall verify that the ukernel was loaded at this intended location (by inspecting DMA_OUS_BASE register) before transferring control to the uOS. These 14 bits represent a cacheline aligned address [19:6] for the uOS location, allowing a uOS to be loaded at an address of upto 1MB in the MinuteIA address space.
	17:0	**uOS Offset** Default Value: 4000h Indicate the byte Offset (from the start of the uOS image) of the first executable instruction within the uOS image. This field allows the BootROM to determine where in the uOS image to transfer control to.

KVMR_SPR_COLOR_CTL

KVMR_SPR_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45030h-45033h
Name:	Kvmr Sprite Color Control
ShortName:	KVMR_SPR_COLOR_CTL
Reset:	soft

DWord	Bit	Description
0	31	**Enable Color Processing** This field enables the sRGB de-gamma, color space conversion to BT2020 and tone mapping with the programmed tone mapping factor. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30:10	**Reserved** Access: RO Format: MBZ
	9:0	**Tone Mapping Factor** This field specifies the tone mapping factor. Each color component gets corrected with this programmed 10 bit fractional value.

L3 Allocation Control Register

L3ALLOCREG - L3 Allocation Control Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B134h
Name:	L3 Allocation Control Register
ShortName:	L3ALLOCREG
Address:	0B234h
ShortName:	L3ALLOCREG_CCS0

This register controls the allocation of various sections of the L3 cache

DWord	Bit	Description
0 L3CacheLayout: 2x2 array	31:25	**All L3 Client Pool** Access: R/W Number of ways allocated for the all client pool. This is a combined pool for all clients. Value: 68h — Name: default **[Default]** Value: [0h,68h] — Name: **Programming Notes** When this field is non-zero, **DC Way Assignment** and **Read Only Client Pool** should be 0KB.
	24:18	**DC Way Assignment** Access: R/W Number of ways allocated for HDC. Value: 0h — Name: **[Default]** Value: [0h,68h] — Name: **Programming Notes** Note: This field must be 0KB if All L3 Client Pool is non-zero.
	17:11	**Read Only Client Pool** Access: R/W Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.

L3ALLOCREG - L3 Allocation Control Register

Value	Name
0h	**[Default]**
[0h,68h]	

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero.

10 **Reserved**

Access:	RO
Format:	MBZ

9 **Reserved**

Access:	RO
Format:	MBZ

8 **Reserved**

Access:	RO
Format:	MBZ

7:1 **URB Allocation**

Access:	R/W

Number of ways allocated for URB

Value	Name
10h	**[Default]**
20h	

0 **Allocation Error status**

Access:	RO

This bit indicates a programming error in L3 allocation registers (L3ALLOCREG and L3TCCNTRLREG).
0 : Indicates no error in programming
1 : Indicates that the L3 allocation programming is incorrect.L3 will use the most recent valid allocation OR default programming.

L3 Cache Runtime ECC capture Register

L3_ECC_CAPTURE_REG - L3 Cache Runtime ECC capture Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B144h

This register shows the captured value of the ECC calculated by the internal logic for L3 writes.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**L3 Cache Latched ECC Value** Access: RO This field holds the value of the ECC generated by the L3 cache pipeline for the preceding write cycle.

L3 Cache Runtime ECC Test Control Register

L3_ECC_TEST_CTL - L3 Cache Runtime ECC Test Control Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B13Ch

This register is used to control the run time testing of the ECC logic in the L3 cache.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21	**L3 ECC Latch Enable** Access: R/W This bit enables the latching of the ECC value generated for any write access made to the L3. The latched value of the ECC can be read from the "L3 Cache Runtime ECC capture Register". 0 – **[Default]** – Disable latching. 1 – Enable the latching
	20	**L3 ECC Override Enable** Access: R/W This bit enables the overriding of the ECC value generated for any write access made to the L3. The value in the field below will be used to override the ECC internally generated. 0 – **[Default]** – Disable override of the ECC value 1 – Enable the override of the ECC value
	19:0	**L3 ECC Override Value** Default Value: 00h Access: R/W This is the value to be used as the override for the ECC when enabled in the bit field above.

L3 Control Register

L3CNTLREG - L3 Control Register		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	07034h	
Name:	L3 Control Register	
ShortName:	L3CNTLREG	

DWord	Bit	Description
0	31:0	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

L3 Multi Context Reserved1

L3RCS0RSVD1 - L3 Multi Context Reserved1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B168h	
ShortName:	L3RCS0RSVD1	
Address:	0B268h	
ShortName:	L3CCS0RSVD1	

DWord	Bit	Description
0	31:0	**SCRATCH** Access: R/W

L3 Multi Context Reserved2

L3 Multi Context Reserved2			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	0B16Ch		
ShortName:	L3RCS0RSVD2		
Address:	0B26Ch		
ShortName:	L3CCS0RSVD2		
DWord	**Bit**	**Description**	
0	31:0	**SCRATCH**	
		Access:	R/W

L3 Node Units Idle Status

L3_NODE_IDLE - L3 Node Units Idle Status			
Register Space:	MMIO: 0/2/0		
Access:	RO Variant		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	0B0B0h		
Status register for l3 node units idle indication. Value 1 means idle			
DWord	**Bit**	**Description**	
0	31:10	**Reserved**	
		Access:	RO
		Format:	MBZ
	9	**IDLE_LTISEQSL**	
	8	**IDLE_GAPL3**	
	7	**IDLE_LNS**	
	6	**IDLE_LSN3**	
	5	**IDLE_LSN2**	
	4	**IDLE_LSN1**	
	3	**IDLE_LSN0**	
	2	**IDLE_LNIC**	
	1	**IDLE_LNIB**	
	0	**IDLE_LNE**	

L3 Parameter Information Register

L3PARAMINFO - L3 Parameter Information Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B164h

Programming Notes

GT_L3_NUM_WAYS_NOTAG + GT_L3_NUM_WAYS gives total number of ways for one L3 bank. Storage per way can be calculated as Total Storage per L3 bank / (GT_L3_NUM_WAYS_NOTAG + GT_L3_NUM_WAYS). L3ALLOCREG and L3TCCNTLREG can be programmed appropriately using storage/way information.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**GT_L3_NUM_WAYS_NOTAG** This field indicates number of ways in L3 bank without tag storage. These number of ways must be allocated for URB.
	7:0	**GT_L3_NUM_WAYS** This field indicates number of tagged ways in L3 bank which is maximum number of ways that can be allocated for cachable data.

L3 SQC register 4

L3SQCREG4 - L3 SQC register 4

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B118h
Address:	0B218h
ShortName:	L3SQCREG4_CCS0

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:15	**Reserved** Access: RO Format: MBZ
	14:11	**Clean Evict Regulation Window** Access: R/W This field determines the time of the clean-eviction evaluation window. Value: 0000b — Name: **[Default]** **Programming Notes** The value provided in this window is multiplied by 16 in hardware. This allows for a range of 0 to 240 clocks for the evaluation window.
	10:7	**Clean Evict Regulation Count** Access: R/W Within the evaluation window, this field defines the number of allowable clean evictions to be sent by the L3BANK. If the limit is reached in a given window, L3BANK will downgrade any further clean evictions (within that window) to silent evictions. This evaluation mechanism is only applicable if clean-evicts are enabled. Value: 0000b — Name: lp_default **[Default]** **Programming Notes** The value programmed in to this register is multiplied by 2 in hardware. This allows for a limit of 0 to 30 clean evictions within the programmable window.

L3SQCREG4 - L3 SQC register 4

	6	**Clean Evict Disable** Access: R/W Clean evicts are disabled when set Value: 1 — Name: **[Default]**
	5:0	**Reserved** Access: RO Format: MBZ

L3 SQC register 5

L3SQCREG5 - L3 SQC register 5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B158h	
Address:	0B258h	
ShortName:	L3SQCREG5_CCS0	

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23	**Reserved** Access: RO Format: MBZ
	22	**Coherent Partial Write Merge Enable** Default Value: 1 Access: R/W Format: Enable _Custom_GTIReset: DEV Enables partial write merge optimization for coherent surfaces.
	21	**Compressible Partial Write Merge Enable** Default Value: 1 Access: R/W Format: Enable _Custom_GTIReset: DEV Enables partial write merge optimization for compressible surfaces.
	20	**LRU update control for detecting oldest partial writes** Default Value: 0 Access: R/W '0' : (default) - Update LRU bit for parent and also for the child merge event '1' : Update LRU bit only for the parent

L3SQCREG5 - L3 SQC register 5

	19:10	**Reserved** Access: RO Format: MBZ
	9:0	**L3 cache partial Write merge timer initial value** Default Value: 1FFh Default Access: R/W If partial write merging is enabled, this timer controls the window to allow partial writes to merge together. The value is first loaded when an eligible request arrives, and is reloaded every time another partial write is collapsed in to the parent **Programming Notes** The value of this register must be nonzero if any partial write merging is enabled, consisting of the CZ + L3 Partial Write Merge Enables in TCCNTLREG*, and the Coherent + Compressible Partial Write Merge Enables in LSCREG5*

L3 SQC register 6

L3SQCREG6 - L3 SQC register 6		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B15Ch	
Address:	0B25Ch	
ShortName:	L3SQCREG6_CCS0	

DWord	Bit	Description
0	31:14	**Reserved** Access: RO Format: MBZ
	13:7	**Maximum number of partial write chains** Access: R/W Value / Name / Description: 10h **[Default]** 4-64 Upper bound is limited by the number of L3 SuperQueue slots
	6:0	**Maximum number of slots that can wait for timer to expire** Access: R/W Value / Name / Description: 20h **[Default]** 4-64 Upper bound is limited by the number of L3 SuperQueue slots

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B100h
Address:	0B200h
ShortName:	L3SQCREG1_CCS0

Programming Notes

Workaround Credits between LNI/LSQC are not updated in case of Render DOP gating condition- DOP Render clock ungating needs to happen before L3SQCREG1 is programmed and it should happen through the driver.

DWord	Bit	Description
0	31:30	**Lookup Fifo2or3 over Fifo1 counter** Default Value: 10b Access: R/W Fifo2 or Fifo3 will be selected as winner as many times as described by this counter before fifo1 that is also available can be selected as winner. Valid values are as follows: ^M 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt (Default). 3 = 8 cnt. lbcf_csr_lsqc_lookup_f2_f3_cnt[1:0]
	29:28	**Lookup Fifo1 over Fifo2or3 counter** Default Value: 11b Access: R/W Fifo1 will be selected as winner as many times as described by this counter before some other fifo (any between Fifo2/Fifo3) that is also available can be selected as winner. Valid values are as follows: ^M 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt 3 = 8 cnt (Default). lbcf_csr_lsqc_lookup_f1_cnt[1:0]

L3SQCREG1 - L3 SQC registers 1

27:26 **Lookup fifo3 counter**

Default Value:	00b
Access:	R/W

Fifo3 will be selected as winner as many times as described by this counter before Fifo2 that is also available can be selected as winner.
Valid values are as follows:
^M
0 = 1 cnt (Default).
1 = 2 cnt.
2 = 4 cnt
3 = 8 cnt.
lbcf_csr_lsqc_lookup_f3_cnt[1:0]

25:24 **Lookup fifo2 counter**

Default Value:	11b
Access:	R/W

Fifo2 will be selected as winner as many times as described by this counter before Fifo3 that is also available can be selected as winner.
Valid values are as follows:
^M
0 = 1 cnt.
1 = 2 cnt.
2 = 4 cnt
3 = 8 cnt (Default).
lbcf_csr_lsqc_lookup_f2_cnt[1:0]

23:17 **L3SQ General Priority Credit Initialization**

Access:	R/W

Description
Number of general priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. The number of general priority credits is always greater than that of high priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32 The number of general priority credits is equal to double the value written in this register. Example: [00001b = 2 credits; 00100b = 8 credits] Valid values for general priority credits can range from: [1 to 32]. Other values are reserved Signal name: lbcf_csr_lsqc_gen_credit_init

Value	Name
0100000b	**[Default]**

L3SQCREG1 - L3 SQC registers 1

		[2h,20h]

Programming Notes

The number of general priority credits is always greater than that of high priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32 lbcf_csr_lsqc_gen_credit_init + lbcf_csr_lsqc_hp_credit_init less than or equal to 32

16:11 **L3SQ High Priority Credit Initialization**

Access:	R/W

Number of high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots.
The number of high priority credits is always lesser than that of general priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32
The number of high priority credits is equal to double the value written in this register. Example: [00001b = 2 credits; 00100b = 8 credits]
Valid values for high priority credits can range from: [0 to 15]. Other values are reserved
Signal name: lbcf_csr_lsqc_gen_credit_init

Value	Name
000000b	**[Default]**

Programming Notes

The number of high priority credits is always lesser than that of general priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32 lbcf_csr_lsqc_gen_credit_init + lbcf_csr_lsqc_hp_credit_init less than or equal to 32

10 **Reserved**

Access:	RO
Format:	MBZ

9 **L3SQ Read Once Enable for Sampler Client**

Access:	R/W

L3SQ Read Once Enable for Sampler Client (SQROE):
Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once.
0 = (default) Reads from Sampler clients issue Read to L3 Cache.
1 = Reads from Sampler clients issue Read Once to L3 Cache.
lbcf_csr_sampler_readonce_en.

L3SQCREG1 - L3 SQC registers 1

8 — Error Detection Behavior Control

Access:	R/W

The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.

Value	Name	Description
0	**[Default]**	RTL does not hang on parity errors or double bit error
1		RTL enforces a hang on parity errors or double bit error

7 — GPGPU L3 Credit Mode Enable

Default Value:	0
Access:	R/W

This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage form L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.

6 — Reserved

Access:	RO
Format:	MBZ

5 — Flush all non coherent lines

The L3 will support destination based flushing for the unified sections of the cache. i.e., if we get a DC flush, even if we have a unified cache, only the lines brought in by DC will be flushed. Similarly, tile cache flushes only clean out lines brought in by the C/Z clients into the unified section.

When a pipeline flush or a tile cache flush is received and if this bit is set, then all the modified non-coherent lines irrespective of DC/C/Z in the unified cache section will be flushed. Also, all the Shared lines in the unified cache section will be downgraded to invalid for all Non- Coherent lines.

This bit will have no impact when DC and tile cache are in separate sections. Also note that this bit will not initiate the invalidation of RO lines in the cache. That is only controlled by the RO invalidation commands sent to the L3 on a per context basis.

Value	Name	Description
0	**[Default]**	By default, the full flush mode will be disabled.

4:0 — Reserved

Access:	RO
Format:	MBZ

L3 Unslice IDLE Status Register

L3_UNSL_IDLE - L3 Unslice IDLE Status Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B414h	
DWord	**Bit**	**Description**
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**LSN Endpoint Unit IDLE Indication** Access: RO Variant LSN Endpoint Unit IDLE. This bit is not used and assigned to zero.
	0	**LTISEQunit Unit IDLE Indication** Access: RO Variant LTISEQunit IDLE

LBCF Render config save msg

LBCFRCSR - LBCF Render config save msg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B3FCh

This register is not context saved and is written by CS unit

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**Render Context Save Request Mask** Access: R/W Hardware Clear Value / Name / Description 0 / default **[Default]** / Render context save request is ignored, and LBCFRCSR[0] is invalid. 1 / / LBCFRCSR[0] is valid.
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Render Context save Request** Access: R/W Hardware Clear Value / Name / Description 0 / default **[Default]** / Render context save is not being requested. 1 / / Render context save is being requested. This bit is self-cleared upon sampling.

LINKM

LINKM	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60040h-60043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_A
Reset:	soft
Address:	61040h-61043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_B
Reset:	soft
Address:	62040h-62043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_C
Reset:	soft
Address:	63040h-63043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_D
Reset:	soft

Description
This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Link M value** This field is the link M value for external transmission in the Main Stream Attributes.

LINKN

LINKN	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60044h-60047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_A
Reset:	soft
Address:	61044h-61047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_B
Reset:	soft
Address:	62044h-62047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_C
Reset:	soft
Address:	63044h-63047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_D
Reset:	soft

Description

This register is double buffered to update on the next MSA after written. **Writes to this register arm M/N registers for this transcoder.**

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Link N value** This field is the link N value for external transmission in the Main Stream Attributes and VB-ID.

LNCF MOCS Register 0

LNCFCMOCS0 - LNCF MOCS Register 0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B020h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS0 - LNCF MOCS Register 0

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	10 ^ 16
1	11 ^ 17
2	12 ^ 18

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS0 - LNCF MOCS Register 0

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 10 ^ 16 1 / 11 ^ 17 2 / 12 ^18
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 1

LNCFCMOCS1 - LNCF MOCS Register 1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B024h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS1 - LNCF MOCS Register 1

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	10 ^ 16
1	11 ^ 17
2	12 ^ 18

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register,this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS1 - LNCF MOCS Register 1

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 10 ^ 16 1 / 11 ^ 17 2 / 12 ^ 18
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 2

LNCFCMOCS2 - LNCF MOCS Register 2

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B028h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls **Value / Name / Description** 0h / UPPER_DIRECT / Use binding table index for direct EU accesses - for the rest it is reserved. 1h / UPPER_UC **[Default]** / Uncacheable 2h / UPPER_RESERVED / Reserved 3h / UPPER_WB / Writeback
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS2 - LNCF MOCS Register 2

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS2 - LNCF MOCS Register 2

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 3

LNCFCMOCS3 - LNCF MOCS Register 3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B02Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS3 - LNCF MOCS Register 3

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS3 - LNCF MOCS Register 3

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 4

LNCFCMOCS4 - LNCF MOCS Register 4

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B030h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls **Value / Name / Description** 0h / UPPER_DIRECT / Use binding table index for direct EU accesses - for the rest it is reserved. 1h / UPPER_UC / Uncacheable 2h / UPPER_RESERVED / Reserved 3h / UPPER_WB **[Default]** / Writeback
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS4 - LNCF MOCS Register 4

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS4 - LNCF MOCS Register 4

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	7h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 5

LNCFCMOCS5 - LNCF MOCS Register 5

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B034h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls **Value / Name / Description** 0h / UPPER_DIRECT / Use binding table index for direct EU accesses - for the rest it is reserved. 1h / UPPER_UC **[Default]** / Uncacheable 2h / UPPER_RESERVED / Reserved 3h / UPPER_WB / Writeback
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS5 - LNCF MOCS Register 5

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS5 - LNCF MOCS Register 5

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 6

LNCFCMOCS6 - LNCF MOCS Register 6

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B038h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS6 - LNCF MOCS Register 6

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS6 - LNCF MOCS Register 6

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	7h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 7

LNCFCMOCS7 - LNCF MOCS Register 7

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B03Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS7 - LNCF MOCS Register 7

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_WT	Writethrough
3h	LOWER_WB	Writeback

LNCFCMOCS7 - LNCF MOCS Register 7

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

LNCF MOCS Register 8

LNCFCMOCS8 - LNCF MOCS Register 8

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B040h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS8 - LNCF MOCS Register 8

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS8 - LNCF MOCS Register 8

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

LNCF MOCS Register 9

LNCFCMOCS9 - LNCF MOCS Register 9

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B044h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS9 - LNCF MOCS Register 9

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS9 - LNCF MOCS Register 9

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 10

LNCFCMOCS10 - LNCF MOCS Register 10

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B048h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS10 - LNCF MOCS Register 10

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS10 - LNCF MOCS Register 10

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 11

LNCFCMOCS11 - LNCF MOCS Register 11

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B04Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS11 - LNCF MOCS Register 11

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS11 - LNCF MOCS Register 11

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 12

LNCFCMOCS12 - LNCF MOCS Register 12

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B050h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register,this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB **[Default]**	Writeback

LNCFCMOCS12 - LNCF MOCS Register 12

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS12 - LNCF MOCS Register 12

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 13

LNCFCMOCS13 - LNCF MOCS Register 13

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B054h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS13 - LNCF MOCS Register 13

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register,this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS13 - LNCF MOCS Register 13

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 14

LNCFCMOCS14 - LNCF MOCS Register 14

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B058h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

DWord	Bit	Description
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS14 - LNCF MOCS Register 14

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS14 - LNCF MOCS Register 14

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 15

LNCFCMOCS15 - LNCF MOCS Register 15

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B05Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS15 - LNCF MOCS Register 15

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS15 - LNCF MOCS Register 15

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

LNCF MOCS Register 16

LNCFCMOCS16 - LNCF MOCS Register 16

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B060h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS16 - LNCF MOCS Register 16

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS16 - LNCF MOCS Register 16

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 17

LNCFCMOCS17 - LNCF MOCS Register 17

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B064h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS17 - LNCF MOCS Register 17

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS17 - LNCF MOCS Register 17

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 18

LNCFCMOCS18 - LNCF MOCS Register 18

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B068h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS18 - LNCF MOCS Register 18

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS18 - LNCF MOCS Register 18

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 19

LNCFCMOCS19 - LNCF MOCS Register 19

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B06Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS19 - LNCF MOCS Register 19

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS19 - LNCF MOCS Register 19

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 20

LNCFCMOCS20 - LNCF MOCS Register 20

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B070h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls **Value / Name / Description** 0h / UPPER_DIRECT / Use binding table index for direct EU accesses - for the rest it is reserved. 1h / UPPER_UC / Uncacheable 2h / UPPER_RESERVED / Reserved 3h / UPPER_WB **[Default]** / Writeback
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS20 - LNCF MOCS Register 20

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS20 - LNCF MOCS Register 20

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 21

LNCFCMOCS21 - LNCF MOCS Register 21

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B074h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

DWord	Bit	Description
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS21 - LNCF MOCS Register 21

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS21 - LNCF MOCS Register 21

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 22

LNCFCMOCS22 - LNCF MOCS Register 22

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B078h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS22 - LNCF MOCS Register 22

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS22 - LNCF MOCS Register 22

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 23

LNCFCMOCS23 - LNCF MOCS Register 23

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B07Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS23 - LNCF MOCS Register 23

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS23 - LNCF MOCS Register 23

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

LNCF MOCS Register 24

LNCFCMOCS24 - LNCF MOCS Register 24

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B080h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS24 - LNCF MOCS Register 24

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS24 - LNCF MOCS Register 24

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 25

LNCFCMOCS25 - LNCF MOCS Register 25

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B084h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS25 - LNCF MOCS Register 25

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS25 - LNCF MOCS Register 25

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 26

LNCFCMOCS26 - LNCF MOCS Register 26

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B088h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS26 - LNCF MOCS Register 26

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS26 - LNCF MOCS Register 26

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 27

LNCFCMOCS27 - LNCF MOCS Register 27

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B08Ch

Programming Notes
WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls **Value / Name / Description** 0h / UPPER_DIRECT / Use binding table index for direct EU accesses - for the rest it is reserved. 1h / UPPER_UC **[Default]** / Uncacheable 2h / UPPER_RESERVED / Reserved 3h / UPPER_WB / Writeback
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS27 - LNCF MOCS Register 27

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS27 - LNCF MOCS Register 27

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 28

LNCFCMOCS28 - LNCF MOCS Register 28

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B090h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls **Value / Name / Description** 0h / UPPER_DIRECT / Use binding table index for direct EU accesses - for the rest it is reserved. 1h / UPPER_UC / Uncacheable 2h / UPPER_RESERVED / Reserved 3h / UPPER_WB **[Default]** / Writeback
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS28 - LNCF MOCS Register 28

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS28 - LNCF MOCS Register 28

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 29

LNCFCMOCS29 - LNCF MOCS Register 29

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B094h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 3h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

LNCFCMOCS29 - LNCF MOCS Register 29

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

7:6 **Reserved**

Access:	RO
Format:	MBZ

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS29 - LNCF MOCS Register 29

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 30

LNCFCMOCS30 - LNCF MOCS Register 30

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B098h

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

DWord	Bit	Description
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS30 - LNCF MOCS Register 30

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS30 - LNCF MOCS Register 30

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 31

LNCFCMOCS31 - LNCF MOCS Register 31

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B09Ch

Programming Notes

WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

DWord	Bit	Description
	19:17	**Upper MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

LNCFCMOCS31 - LNCF MOCS Register 31

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

7:6 Reserved

Access:	RO
Format:	MBZ

5:4 Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS31 - LNCF MOCS Register 31

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02440h-02443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_RCSUNIT_BE_GEOMETRY
Address:	18440h-18443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Base Vertex** Format: S31 This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 0

3DPRIM_XP0 - Load Indirect Extended Parameter 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02690h-02693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_RCSUNIT_BE_GEOMETRY
Address:	18690h-18693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Extended Parameter 0** Format: U32 **Description** This register is used to store the Extended Parameter 0 of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 1

3DPRIM_XP1 - Load Indirect Extended Parameter 1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02694h-02697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_RCSUNIT_BE_GEOMETRY
Address:	18694h-18697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Extended Parameter 1** Format: U32 **Description** This register is used to store the Extended Parameter 1 of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 2

3DPRIM_XP2 - Load Indirect Extended Parameter 2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02698h-0269Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_RCSUNIT_BE_GEOMETRY
Address:	18698h-1869Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Extended Parameter 2** Format: U32 **Description** This register is used to store the Extended Parameter 2 of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02438h-0243Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18438h-1843Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Instance Count** This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0243Ch-0243Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_RCSUNIT_BE_GEOMETRY
Address:	1843Ch-1843Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02430h-02433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_RCSUNIT_BE_GEOMETRY
Address:	18430h-18433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02434h-02437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18434h-18437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Vertex Count** Format: U32 This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Lock register for Bank

L3BANKLOCK - Lock register for Bank

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B160h

This is a basic register template

DWord	Bit	Description
0	31	**Lockdown L3BANKLOCK for writes** Default Value: 0h Access: R/W 0 : (default) All bits of L3BANKLOCK (offset 0xB160) register are R/W 1 : All bits of L3BANKLOCK (offset 0xB160) register are RO Once written to 1, the lock is set for all of 0B160 and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock Control is 0B160h bit 31
	30:17	**Reserved** Access: RO Format: MBZ
	16:14	**Reserved** Access: RO Format: MBZ
	13	**Lockdown L3_ECC_TEST_CTL for writes** Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Value / Name / Description: 0 / **[Default]** / 1 / / All bits of L3_ECC_TEST_CTL (offset 0xB13C) and URB_ECC_TEST_CTL (offset 0xB148) registers are RO.
	12	**Lockdown L3SQCREG3 for writes** Access: R/W Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Value / Name / Description: 0 / default **[Default]** / 1 / / All bits of L3SQCREG3 (offset 0xB108) register are RO.

L3BANKLOCK - Lock register for Bank

11 — Lockdown LBSREG for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of LBSREG (offset 0xB124) register are RO.

10 — Lockdown LSQCFIFOARB for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of LSQCFIFOARB (offset 0xB150) register are RO.

9 — Lockdown SCRATCH1 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of SCRATCH1 (offset 0xB11C) register are RO.

8 — Lockdown LTCDREG2 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of LTCDREG2 (offset 0xB110) register are RO.

7 — Lockdown L3SQCREG2 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of L3SQCREG2 (offset 0xB104) register are RO.

6 — Lockdown L3SCRATCH3 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

L3BANKLOCK - Lock register for Bank

Value	Name	Description
0	default **[Default]**	All bits of L3SCRATCH3 (offset 0xB154) register are R/W
1		Bits [10:4] of L3SCRATCH3 (offset 0xB154) register are RO.

5 **Lockdown L3SCRATCH2 for writes**

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of L3SCRATCH2;(offset 0xB140) register are R/W
1		All bits of L3SCRATCH2 offset 0xB140) register are RO

4 **Lockdown L3SQCREG1 for writes**

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	Default **[Default]**	All valid bits of L3SQREG1 (offset 0xB100) register are R/W
1		All valid bits of L3SQREG1 (offset 0xB100) register are R/W (no locking effect)

3 **Lockdown LTCDREG for writes**

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of LTCDREG (offset 0xB120) register are R/W
1		All bits of LTCDREG (offset 0xB120) register are RO

2 **Lockdown L3SQCREG4 for writes**

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of L3SQREG4 (offset 0xB118) register are R/W
1		All bits of L3SQREG4 (offset 0xB118) register are R/W (no locking effect)

L3BANKLOCK - Lock register for Bank

	1	**Lockdown L3CHMD for writes** Access: R/W Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). **Value** / **Name** / **Description** 0h / **[Default]** / (default) All bits of L3CHMD (offset 0xB114) register are R/W 1 / / All bits of L3CHMD (offset 0xB114) register are RO
	0	**Lockdown L3CNTLREG1 for writes** Access: R/W Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). **Value** / **Name** / **Description** 0h / **[Default]** / (default) - All bits of L3CNTLREG1 (offset 0xB10C) register are R/W 1 / / All bits of L3CNTLREG1 (offset 0xB10C) register are RO

Lock register for LPFC

L3LPFCLOCK - Lock register for LPFC

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B460h

This is a basic register template

DWord	Bit	Description
0	31	**Lockdown L3LPFCLOCK** Default Value: 0h Access: R/W 0 : (default) All bits of L3LPFCLOCK (offset 0xB460) register are R/W 1 : All bits of L3LPFCLOCK (offset 0xB460) register are RO Once written to 1, the lock is set for all of 0xB460 and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock Control is B460h bit 31
	30:3	**Reserved** Access: RO Format: MBZ
	2	**Reserved**
	1	**Lockdown LSN Unslice Client Virtual Channel Assignment** Default Value: 0h Access: R/W 0 : (default) bits is R/W 1 : bit is RO Once Lock Control B460h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).
	0	**Lockdown LPFC hashing disable** Default Value: 0h Access: R/W 0 : (default) bit is R/W 1 : bit is RO Once Lock Control B460h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Lock register for Node

L3NODELOCK - Lock register for Node

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0ACh

This is a basic register template

DWord	Bit	Description
0	31	**Lockdown L3NODELOCK** Default Value: 0h Access: R/W 0 : (default) All bits of L3NODELOCK (offset 0xB0AC) register are R/W 1 : All bits of L3NODELOCK (offset 0xB0AC) register are RO Once written to 1, the lock is set for all of 0xB0AC and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock Control is 0B0ACh bit 31
	30:4	**Reserved** Access: RO Format: MBZ
	3	**Lockdown Color client arb pri, Z client Arb pri** Default Value: 0h Access: R/W 0 : (default) bits is R/W 1 : bit is RO Once Lock Control 0B0ACh bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).
	2	**Lockdown slow client fix dis** Default Value: 0h Access: R/W 0 : (default) bits is R/W 1 : bit is RO Once Lock Control 0B0ACh bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

L3NODELOCK - Lock register for Node

	1	**Lockdown TC/vc sel, LSN arb pri sel** Default Value: 0h Access: R/W 0 : (default) bits is R/W 1 : bit is RO Once Lock Control 0B0ACh bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).
	0	**Lockdown Hashing disable, mod5 hash dis, Non coh completion from node enable** Default Value: 0h Access: R/W 0 : (default) bit is R/W 1 : bit is RO Once Lock Control 0xB0ACh bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

LPFC FUSA Register

LPFC_FUSA - LPFC FUSA Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B480h

Functional Safety Register. LPFC collects updates of single and double bit errors from all LBCF in ECC Checker Mode.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Double bit error indication from Bank 7** Access: R/W Double Error detection indication from Bank7.
	14	**Single bit error indication from Bank 7** Access: R/W Single Error detection indication from Bank7.
	13	**Double bit error indication from Bank 6** Access: R/W Double Error detection indication from Bank6.
	12	**Single bit error indication from Bank 6** Access: R/W Single Error detection indication from Bank6.
	11	**Double bit error indication from Bank 5** Access: R/W Double Error detection indication from Bank5.
	10	**Single bit error indication from Bank 5** Access: R/W Single Error detection indication from Bank5.

LPFC_FUSA - LPFC FUSA Register

	9	**Double bit error indication from Bank 4** Access: R/W Double Error detection indication from Bank4.
	8	**Single bit error indication from Bank 4** Access: R/W Single Error detection indication from Bank4.
	7	**Double bit error indication from Bank 3** Access: R/W Double Error detection indication from Bank3.
	6	**Single bit error indication from Bank 3** Access: R/W Single Error detection indication from Bank3.
	5	**Double bit error indication from Bank 2** Access: R/W Double Error detection indication from Bank2.
	4	**Single bit error indication from Bank 2** Access: R/W Single Error detection indication from Bank2.
	3	**Double bit error indication from Bank 1** Access: R/W Double Error detection indication from Bank1.
	2	**Single bit error indication from Bank 1** Access: R/W Single Error detection indication from Bank1.
	1	**Double bit error indication from Bank 0** Access: R/W Double Error detection indication from Bank0.
	0	**Single bit error indication from Bank 0** Access: R/W Single Error detection indication from Bank0.

LSN Arbitration Priority Register 0

LSN_ARBPRI0 - LSN Arbitration Priority Register 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0D0h

DWord	Bit	Description
0	31:28	**GAPS Local-Slice Arbitration Priority** This value is 'n' in the m:n priority scheme for L3 vs. GAPS local-slice traffic. Value: 1 — **[Default]** Value: [1,15]
	27:24	**L3 Local-Slice Arbitration Priority** This value is 'm' in the m:n priority scheme for L3 vs. GAPS local-slice traffic. Value: 4 — **[Default]** Value: [1,15]
	23:20	**LNE Traffic Class Channel 1 Priority Value** This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LNE cycles. Value: 4 — **[Default]** Value: [1,15]
	19:16	**LNE Traffic Class Channel 0 Priority Value** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LNE cycles. Value: 1 — **[Default]** Value: [1,15]
	15:12	**LSN Virtual Channel 1 Traffic Class Channel 1 Priority Value** This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 1 cycles. Value: 4 — **[Default]** Value: [1,15]

LSN_ARBPRI0 - LSN Arbitration Priority Register 0

	11:8	**LSN Virtual Channel 1 Traffic Class Channel 0 Priority Value** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 1 cycles. **Value** / **Name** 1 / **[Default]** [1,15] /
	7:4	**LSN Virtual Channel 0 Traffic Class Channel 1 Priority Value** This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 0 cycles. **Value** / **Name** 4 / **[Default]** [1,15] /
	3:0	**LSN Virtual Channel 0 Traffic Class Channel 0 Priority Value** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 0 cycles. **Value** / **Name** 1 / **[Default]** [1,15] /

LSN Arbitration Priority Register 1

LSN_ARBPRI1 - LSN Arbitration Priority Register 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0D4h

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24	**LSN Opporunistic Arbitration Disable** Default Value: 0 _Custom_GTIReset: DEV 0 (default) - Opportunistic Arbitration mechanism of LSN Cross-Slice, LSN-LNI and LSN-LNE arbiters is enabled. 1- Opportunistic Arbitration mechanism of LSN Cross-Slice, LSN-LNI and LSN-LNE arbiters is disabled. Signal name - lncf_csr_lsn_opprtnstc_arb_dis
	23:20	**LNI Egress Traffic Class Channel 1 Priority Value** This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on completions to LNI's egress port. Value: 4 **[Default]** Value: [1,15]
	19:16	**LNI Egress Traffic Class Channel 0 Priority Value** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on completions to LNI's egress port. Value: 1 **[Default]** Value: [1,15]
	15:12	**LNI Ingress Traffic Class Channel 1 Priority Value** This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on completions to LNI's ingress port. Value: 4 **[Default]** Value: [1,15]

LSN_ARBPRI1 - LSN Arbitration Priority Register 1

	11:8	**LNI Ingress Traffic Class Channel 0 Priority Value** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on completions to LNI's ingress port. **Value** / **Name** 1 / **[Default]** [1,15] /
	7:4	**Cross-Slice Completion Traffic Class Channel 1 Priority Value** This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on cross-slice completions. **Value** / **Name** 4 / **[Default]** [1,15] /
	3:0	**Cross-Slice Completion Traffic Class Channel 0 Priority Value** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on cross-slice completions. **Value** / **Name** 1 / **[Default]** [1,15] /

LSN Miscellaneous Configuration

LSN_MISC - LSN Miscellaneous Configuration

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0CCh

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	5	**L3 Smart Repeater Bypass Enable** When set, L3 smart repeaters in unslice will bypass all FIFOs for requests. The simple flop bypass path will be used.
	4	**LSN Egress Pipeline Clock Gating Enable** Value / Name / Description: 1 / **[Default]** / Enable fub-level clock gating of the LSN egress pipeline. 0 / / Disable fub-level clock gating of the LSN egress pipeline.
	3	**LSN Smart Gating for Slice-Bound Memory Fill Repeaters Disable** Value / Name / Description: 1 / **[Default]** / Disable the smart gating of slice-bound memory fill repeaters. 0 / / Allow smart-gating for slice-bound memory fill repeaters.
	2	**LSN Conservative Arbitration Control** Controls whether LSN uses a more conservative form of arbitration by removing assumptions about packet arrival Value / Name / Description: 1 / / Cycles are only eligible for arbitration in the pipeline after arrival of all packets of the cycle. 0 / **[Default]** / Cycles are eligible for arbitration after the arrival of the first packet of the cycle.
	1	**GAFS Return Simple Arbitration Control** Enables simple arbitration between upstream LSN busses when returning GAFS-bound read returns. This arbitration uses a continuously running counter to select two busses for GAFS-bound read returns.

LSN_MISC - LSN Miscellaneous Configuration

Value	Name	Description
1	SIMPLE	Enable simple (always running) arbitration
0	PRIORITY **[Default]**	Enable priority-based arbitration

0 **LSN Cross-Slice Virtual Channel Arbitration Control**

Controls whether to use round-robin or fixed priority arbitration between cross-slice virtual channels

Value	Name	Description
1	RR_PRI	Enable round-robin priority between VC1 and VC0
0	FIXED_PRI **[Default]**	Enable fixed priority between VC1 and VC0. VC1 will always take higher priority

LSN Slice Client Virtual Channel Assignment

LSN_SLCVC - LSN Slice Client Virtual Channel Assignment

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0C8h

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:14	**Reserved** Access: RO Format: MBZ
	13	**Traffic Class Channel ID for GAFS-Bound L3 Returns in LNE Ingress FIFOs** Default Value: 1
	12	**Traffic Class Channel ID for L3-Bound L3 Returns in LNE Ingress FIFOs** Default Value: 0
	11	**Traffic Class Channel ID for GAFS-Bound Completions in LNI Completion Ingress FIFO** Default Value: 1
	10	**Traffic Class Channel ID for L3-Bound Completions in LNI Completion Ingress FIFO** Default Value: 0
	9	**Traffic Class Channel ID for L3 Cycles** Value: 0 — Name: **[Default]**
	8	**Virtual Channel ID for L3 Cycles** Default Value: 0
	7	**Traffic Class Channel ID for GAFS-Bound Read Returns** Default Value: 1
	6	**Virtual Channel ID for GAFS-Bound Read Returns** Default Value: 1
	5	**Traffic Class Channel ID for Downstream L3-Bound Read Returns** Value: 1 — Name: **[Default]**

LSN_SLCVC - LSN Slice Client Virtual Channel Assignment

	4	**Virtual Channel ID for Downstream L3-Bound Read Returns** Default Value: 1
	3	**Traffic Class Channel ID for Upstream L3-Bound Read Returns** Value: 1 — Name: **[Default]**
	2	**Virtual Channel ID for Upstream L3-Bound Read Returns** Default Value: 1
	1	**Traffic Class Channel ID for GAPS Cycles** Value: 1 — Name: **[Default]**
	0	**Virtual Channel ID for GAPS Cycles** Default Value: 0

LSQC FIFO Arbitration

LSQCFIFOARB - LSQC FIFO Arbitration

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0B150h

LSQC FIFO Arbitration register enables programmable arbitration used for selecting a winner amongst multiple FIFO's in LSQC

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:22	**Memory read over memory write** Access: R/W _Custom_GTIReset: DEV This count will determine for how many clocks the memory reads will be selected as winner before allowing memory writes. Needed as Cmd port from lsqc to gapl3 is just 1. Valid values are as follows: 0 = 1 cnt (Default). 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt. lbcf_csr_lsqc_memrd_over_memwr_cnt[1:0] Value: 1 — Name: **[Default]**
	21:20	**Memory write over Memory Read** Access: R/W _Custom_GTIReset: DEV This count will determine for how many clocks the memory writes will be selected as winner before allowing memory reads. Needed as Cmd port from lsqc to gapl3 is just 1. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt (Default). lbcf_csr_lsqc_memwr_over_memrd_cnt[1:0] Value: 0 — Name: def **[Default]**

LSQCFIFOARB - LSQC FIFO Arbitration

	19:18	**Memory read Fifo2 counter** Default Value: 00b Access: R/W _Custom_GTIReset: DEV This count will determine for how many clocks the memory reads fifo2 will be selected as winner before allowing memory read Fifo1. Valid values are as follows: 0 = 1 cnt (Default). 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt. lbcf_csr_lsqc_memrd_f2_cnt[1:0]
	17:16	**Memory read Fifo1 counter** Default Value: 11b Access: R/W _Custom_GTIReset: DEV This count will determine for how many clocks the memory reads fifo1 will be selected as winner before allowing memory read Fifo2. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt (Default). lbcf_csr_lsqc_memrd_f1_cnt[1:0]
	15:14	**Memory write Fifo2 counter** Default Value: 00b Access: R/W _Custom_GTIReset: DEV This count will determine for how many clocks the memory writes fifo2 will be selected as winner before allowing read returns. Valid values are as follows: 0 = 1 cnt (Default). 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt. lbcf_csr_lsqc_memwr_f2_cnt[1:0]

LSQCFIFOARB - LSQC FIFO Arbitration

	13:12	**Memory write Fifo1 counter** Default Value: 11b Access: R/W _Custom_GTIReset: DEV This count will determine for how many clocks the memory writes fifo1 will be selected as winner before allowing read returns. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt (Default). lbcf_csr_lsqc_memwr_f1_cnt[1:0]
	11:10	**Read Return Fifo3 counter** Default Value: 00b Access: R/W _Custom_GTIReset: DEV Fifo3 will be selected as winner as many times as described by this counter before some other fifo that is also available can be selected as winner. Valid values are as follows: 0 = 1 cnt (Default). 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt. lbcf_csr_lsqc_rdret_f3_cnt[1:0]
	9:8	**Read Return Fifo2 counter** Default Value: 10b Access: R/W _Custom_GTIReset: DEV Fifo2 will be selected as winner as many times as described by this counter before some other fifo that is also available can be selected as winner. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt (Default). 3 = 8 cnt. lbcf_csr_lsqc_rdret_f2_cnt[1:0]

LSQCFIFOARB - LSQC FIFO Arbitration

	7:6	**Read Return Fifo1 counter** Default Value: 11b Access: R/W _Custom_GTIReset: DEV Fifo1 will be selected as winner as many times as described by this counter before some other fifo that is also available can be selected as winner. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt (Default). lbcf_csr_lsqc_rdret_f1_cnt[1:0]
	5:4	**Fill Fifo3 counter** Default Value: 00b Access: R/W _Custom_GTIReset: DEV Fifo3 will be selected as winner as many times as described by this counter before some other fifo that is also available can be selected as winner. Valid values are as follows: 0 = 1 cnt (Default). 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt. lbcf_csr_lsqc_fill_f3_cnt[1:0]
	3:2	**Fill Fifo2 counter** Default Value: 10b Access: R/W _Custom_GTIReset: DEV Fifo2 will be selected as winner as many times as described by this counter before some other fifo that is also available can be selected as winner. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt (Default). 3 = 8 cnt. lbcf_csr_lsqc_fill_f2_cnt[1:0]

LSQCFIFOARB - LSQC FIFO Arbitration

	1:0	**Fill Fifo1 counter** Default Value: 11b Access: R/W _Custom_GTIReset: DEV Fifo1 will be selected as winner as many times as described by this counter before some other fifo that is also available can be selected as winner. Valid values are as follows: 0 = 1 cnt. 1 = 2 cnt. 2 = 4 cnt. 3 = 8 cnt (Default). lbcf_csr_lsqc_fill_f1_cnt[1:0]

LUT_3D_CTL

LUT_3D_CTL

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled

Address:	490A4h-490A7h
Name:	Pipe A 3D LUT Control
ShortName:	LUT_3D_CTL_A
Reset:	soft

Address:	491A4h-491A7h
Name:	Pipe B 3D LUT Control
ShortName:	LUT_3D_CTL_B
Reset:	soft

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>31</td><td>LUT 3D Enable
This field enables the 3D LUT.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Disable</td></tr>
<tr><td>1b</td><td>Enable</td></tr>
</table>
<table>
<tr><th>Programming Notes</th></tr>
<tr><td>3D LUT can be enabled/disabled at any time irrespective of when the pipe is enabled/disabled. Program the Bit 10 of register 420b0h to 1b to ensure that the 3D LUT functionality gets enabled on the first frame after the pipe turns on.</td></tr>
</table></td></tr>
<tr><td>30</td><td>New LUT Ready
<table>
<tr><td>Access:</td><td>R/W Set</td></tr>
</table>
This bit must be set to '1' after all the 3D LUT entries are programmed. This bit will get cleared by hardware after the LUT buffer is loaded in to the internal working RAM.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>New LUT not ready</td><td>New LUT is not yet ready/hardware finished loading the LUT buffer in to internal working RAM.</td></tr>
<tr><td>1b</td><td>New LUT Ready</td><td>New LUT is ready.</td></tr>
</table>
<table>
<tr><th>Restriction</th></tr>
<tr><td>Once set, only hardware is allowed to clear this bit. Software cannot clear this bit.</td></tr>
</table></td></tr>
</table>

LUT_3D_CTL

	29	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for the 3D LUT registers that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled. Updates to the LUT entries, triggered by New LUT Ready, do not have double buffer updating disabled. **Value** / **Name** 0b: Not Allowed 1b: Allowed **[Default]**
	28:0	**Reserved** Access: RO Format: MBZ

LUT_3D_DATA

LUT_3D_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	490ACh-490AFh
Name:	Pipe A 3D LUT Data
ShortName:	LUT_3D_DATA_A
Reset:	soft
Address:	491ACh-491AFh
Name:	Pipe B 3D LUT Data
ShortName:	LUT_3D_DATA_B
Reset:	soft

These are the 3D LUT entries. The 3D LUT Index Value indicates the 3D LUT location to be accessed through this register.
Even though this specific register is not double buffered, the 3D LUT table that this register accesses is (i.e. this register updates the table's back buffer). The double buffering point for the table (after DB'ing is armed) is the start of V. Blank or the Pipe is disabled

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:0	**LUT 3D Entry** 3D LUT entry value programmed as R10G10B10.

LUT_3D_INDEX

LUT_3D_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	490A8h-490ABh
Name:	Pipe A 3D LUT Index
ShortName:	LUT_3D_INDEX_A
Reset:	soft

Address:	491A8h-491ABh
Name:	Pipe B 3D LUT Index
ShortName:	LUT_3D_INDEX_B
Reset:	soft

This index controls access to the pre-double buffered array of 3D LUT entries.
Even though this specific register is not double buffered, the 3D LUT table that this register accesses is (i.e. this register updates the table's back buffer). The double buffering point for the table (after DB'ing is armed) is the start of V. Blank or the Pipe is disabled

DWord	Bit	Description
0	31:14	**Reserved** Access: RO Format: MBZ
	13	**Index Auto Increment** This field enables the index value to auto increment on each read or write to the data register. 0b – No Increment 1b – Auto Increment
	12:0	**Index Value** This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. [0,4912]