Enabling Nios® II Boot from Quad Serial Configuration (EPCQ) and Serial Configuration (EPCS) devices in Quartus® II 13.0

Introduction.

EPCQ / EPCS configuration devices can store FPGA images and NIOS II software. The flow below should be followed to setup a system to configure the FPGA from EPCQ / EPCS and load NIOS II software from the EPCQ / EPCS. The flow below also includes the workarounds needed to solve problems in the Quartus II software version 13.0

1. Altera V Series Devices only: Install required patch files

To resolve the known issues with the NIOS II boot loader for V series devices, the relevant patches must be installed

Notes:

1. **The patches for EPCS and EPCQ will overwrite each other**
2. **The patch files can be downloaded from:** http://www.altera.com/support/kdb/solutions/rd11122013_865.html

To support boot from EPCQ

- Quartus II 13.0
  - Run the installer for ACS patch 0.23 for Quartus® II 13.0 targeting your 13.0 installation.

- Quartus II 13.0 SP1
  - Run the installer for ACS patch 0.23 for Quartus II 13.0 targeting an empty directory
  - Replace the em_epcs.pl and em_epcs_qsys.pm files found in the Quartus II installation:

<13.0SP1_Installation_Directory>\ip\altera\sopc_builder_ip\altera_avalon_epcs_flash_controller\

  - with the files from step 1:

<ACS Patch 0.23 install directory>\ip\altera\sopc_builder_ip\altera_avalon_epcs_flash_controller\

To support boot from EPCS

- Quartus II 13.0 and 13.0SP1
  - Extract the EPCS_Fix_For_V_Series_Devices.zip file to your Quartus II installation directory.

2. Configure your Quartus II project

1. Close your Qsys and Quartus II projects
2. Open the <project>.qsf file for your project in a text editor and add the following to lines set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME "ACTIVE SERIAL X1"

set_global_assignment -name ENABLE_INIT_DONE_OUTPUT ON
Note: set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME "ACTIVE SERIAL X4" may be set, this assignment should be removed.

3. Delete the “db”, “incremental_db” and “qsys generated folders” in your project directory

3. Configure your Qsys project

1. Open your Quartus II and Qsys Projects
2. Ensure the Nios II’s Reset Vector is pointing at EPCS/EPCQ Controller
3. Ensure the Nios II’s Exception Vector is pointing at onchip_memory or some other memory device
4. Generate your design in Qsys
5. Compile your design in Quartus II

4. Compile your Nios II software

1. Create (or update) your Nios II BSP in Eclipse, based on the .sopcinfo file created in section 3.
2. Build your BSP and application projects

Note: For testing the count binary example application can be used if you have a pio_led device in your Qsys system connected to LEDs (this exists in most golden system designs for Altera development kits)

5. Generate programing files for configuration and EPCQ programming

1. **Open a Nios II command shell**
   Linux: `<Quartus II Install>/nios2eds/nios2_command_shell.sh`
   Windows: `<Quartus II Install>/nios2eds/nios2_command_shell.bat` or launch a Nios II Command shell from the Nios II EDS start menu group (under Quartus II)

2. **Create a flash image of your FPGA configuration file**
   ```
   sof2flash --input=hw.sof --output=hw.flash --epcq --verbose
   ```
   Note: We are using --epcq instead of --epcs here for EPCQ devices

3. **Create a flash image of your NIOS II .elf file**
   ```
   elf2flash --input=sw.elf --output=sw.flash --epcs --after=hw.flash –verbose
   ```

4. **Create the .hex image of your Nios II software**
   ```
   nios2-elf-objcopy --input-target srec --output-target ihex sw.flash sw.hex
   ```

5. **Generate the .jic file to program the EPCQ using the “Convert Programming File” tool**
   1. Open the Convert Programming File tool from the file menu in Quartus II
   2. Select .jic file for “Programming file type”
   3. Select EPCQ256 for “Configuration device”
   4. Make sure “Active Serial” is selected for “Configuring device mode”.
   5. Click on “Flash Loader”, then click on “Add Device” to select the Cyclone V device you’re using then click “Ok”.
   6. Click on “SOF Data”, then click on “Add File” to select the .sof file generated by Quartus II compilation.
   7. Click on the .sof file you have just added, click on “Properties” and enable the “Compression”

8. Click the “Add Hex Data” button
9. Select “Relative Addressing”
10. Select your <project>.hex file containing your Nios II software image
11. Click on “Generate” to generate the .jic file

6. Configure your development kit / board for EPCQ programming

- Cyclone V SOC kit
  1. Program the Max V device with the max2_CVSocEPCQ.pof
  2. Set MSEL[4:0] to 10011

  The MSEL pins are laid out 0,1,2,4 and down is on.
  MSEL[4:0] to 10011 is (left to right): down, down, up, up, down

- Cyclone V E kit
  1. Program the Max V device with the relevant image to allow EPCQ programming and ensure board is configured correctly (some resistors may need to be de populated).
  2. Set MSEL[4:0] to 10011
- Other kits: Ensure EPCQ is enabled and MSEL is correctly set for your device

7. Program the EPCQ/ EPCS

1. Connect your board
2. Open the Quartus II Programmer
3. Press Auto-detect
4. Left Click on the FPGA part in the lower section of the Programmer Window
5. Right click and select add flash device
6. Select the relevant EPCS/EPCQ device
   For Cyclone V Boards: Altera EPCQ 256 device
7. Right click on the FPGA part in the top section of the Programmer window
8. Select change file
9. Select the .jic file you have generated
10. Select program/configure for the EPCQ/EPCS device which should be shown under the FPGA device in the top section of the window
    Note: This action should also tick the program/ configure option for the FPGA device
11. Click start
12. Once programming is complete power cycle your board, it should boot from EPCQ/EPCS and load your NIOS Ii Code.

8. Conclusion

This document is a guide on how to configure a NIOS II system to boot from EPCS or EPCQ devices in Quartus II 13.0, including the use of the required software patched

If the behavior of your Nios II system is not as expected the first debug step is to try and connect to the NIOS II by launching the nios2-terminal from a Nios II Embedded Command prompt.

If the nios2-terminal can connect this will show if the FPGA has been configured, and the NIOS II is live: Check the boot loader patches have been installed correctly.

If the nios2-terminal cannot connect it suggests the FPGA has not been configured, or the NIOS II is in reset: Check the flow used to convert the .sof and the EPCQ programming flow.

9. Revision History

Revision	Changes Made	Date
V1.0	Initial release.	Oct 2013