Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B1	VREFB1N0	VCCD_PLL3			1	1	D4	F5						
B1	VREFB1N0	GNDA3			2	2	E5	E5						
B1	VREFB1N0	VCCA3			3	3	F5	E4						
B1	VREFB1N0	IO	DIFFIO_L1p			4		B2					DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L1n			5		B1						
B1	VREFB1N0	IO	DIFFIO_L2p			6		C2						
B1	VREFB1N0	IO	DIFFIO_L2n					C1					DQ1L	DQ1L
B1	VREFB1N0	VCCIO1				7								
B1	VREFB1N0	IO		nRESET				C3						
B1	VREFB1N0	GND				8								
B1	VREFB1N0	IO			4	9	B1	D3		DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0
B1	VREFB1N0	VCCINT			5	10								
B1	VREFB1N0	IO	DIFFIO_L3p				C2	D2					DQ1L	DQ1L
B1	VREFB1N0	GND				11								
B1	VREFB1N0	IO	DIFFIO_L3n	DATA1, ASDO	6	12	C1	D1						
B1	VREFB1N0	IO	VREFB1N0		7	13	F3	F3						
B1	VREFB1N0	IO	DIFFIO_L4p	FLASH_nCE, nCSO	8	14	D2	E2						
B1	VREFB1N0	VCCIO1				15								
B1	VREFB1N0	IO	DIFFIO_L4n				D1	E1					DQ1L	DQ1L
B1	VREFB1N0	GND				16								
B1	VREFB1N0	nSTATUS		nSTATUS	9	17	F4	G5						
B1	VREFB1N0	IO				18	G5	H6						
B1	VREFB1N0	IO	DIFFIO_L5p				F2	G2					DQ1L	DQ1L
B1	VREFB1N0	VCCINT				19								
B1	VREFB1N0	IO	DIFFIO_L5n				F1	G1					DQ1L	DQ1L
B1	VREFB1N0	GND				20								
B1	VREFB1N0	IO	DIFFIO_L6p		10	21	G2	H2	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0
B1	VREFB1N0	IO	DIFFIO_L6n		11	22	G1	H1						
B1	VREFB1N0	DCLK		DCLK	12	23	H1	H4						
B1	VREFB1N0	IO		DATA0	13	24	H2	H3						
B1	VREFB1N0	nCONFIG		nCONFIG	14	25	H5	H5						
B1	VREFB1N0	TDI		TDI	15	26	H4	J6						
B1	VREFB1N0	TCK		TCK	16	27	H3	J1						
B1	VREFB1N0	VCCIO1			17									
B1	VREFB1N0	TMS		TMS	18	28	J5	J2						
B1	VREFB1N0	GND			19									
B1	VREFB1N0	TDO		TDO	20	29	J4	J5						
B1	VREFB1N0	nCE		nCE	21	30	J3	K6						
B1	VREFB1N0	CLK0	DIFFCLK_0p		22	31	E2	F2						
B1	VREFB1N0	CLK1	DIFFCLK_0n		23	32	E1	F1						
B2	VREFB2N0	CLK2	DIFFCLK_1p		24	33	M2	N2						
B2	VREFB2N0	CLK3	DIFFCLK_1n		25	34	M1	N1						
B2	VREFB2N0	IO	DIFFIO_L7p				J2	K2			DQ1L		DQ1L	DQ1L
B2	VREFB2N0	VCCIO2			26	35								
B2	VREFB2N0	IO	DIFFIO_L7n				J1	K1			DQ1L		DQ1L	DQ1L
B2	VREFB2N0	GND			27	36								
B2	VREFB2N0	IO	DIFFIO_L8p		28	37		K5		DQ1L			DQ1L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L8n			38		L5		DQ1L			DM1L/BWS#1L	DM1L0/BWS#1L1
B2	VREFB2N0	IO						L6						
B2	VREFB2N0	IO	DIFFIO_L9p					L2					DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L9n			39		L1					DQ3L	DQ1L
B2	VREFB2N0	VCCINT			29	40								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B2	VREFB2N0	IO	DIFFIO_L10p			41	K2	L4		DQ1L			DQ3L	DQ1L
B2	VREFB2N0	GND				42								
B2	VREFB2N0	IO	DIFFIO_L10n			43	K1	L3		DQ1L	DQ1L		DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L11p		30	44	L2	M2	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1
B2	VREFB2N0	IO	DIFFIO_L11n			45	L1	M1		DQ1L	DQ1L			
B2	VREFB2N0	IO	VREFB2N0		31	46	L3	M3						
B2	VREFB2N0	IO	DIFFIO_L12p					P2					DQ3L	DQ1L
B2	VREFB2N0	VCCIO2				47								
B2	VREFB2N0	IO	DIFFIO_L12n					P1					DQ3L	DQ1L
B2	VREFB2N0	GND				48								
B2	VREFB2N0	IO	DIFFIO_L13p			49	N2	R2		DQ1L	DQ1L		DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L13n			50	N1	R1			DQ1L			
B2	VREFB2N0	IO	RUP1		32	51	K5	T2		DQ1L	DQ1L			
B2	VREFB2N0	IO	RDN1		33	52	L4	T1		DQ1L	DQ1L			
B2	VREFB2N0	IO	DIFFIO_L14p					T3					DQ3L	DQ1L
B2	VREFB2N0	VCCINT			34	53								
B2	VREFB2N0	IO	DIFFIO_L14n					R3					DQ3L	DQ1L
B2	VREFB2N0	GND				54								
B2	VREFB2N0	IO				55	R1	M5		DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1
B2	VREFB2N0	IO	DIFFIO_L15p			56	P2	R5			DQ1L			
B2	VREFB2N0	IO	DIFFIO_L15n			57	P1	R4		DQ1L	DM1L/BWS#1L		DM3L/BWS#3L	DM1L1/BWS#1L2
B2	VREFB2N0	VCCA1			35	58	L5	N5						
B2	VREFB2N0	GNDA1			36	59	M5	P5						
B2	VREFB2N0	VCCD_PLL1			37	60	N4	P4						
B3	VREFB3N0	IO	DIFFIO_B1p				N3	U1						
B3	VREFB3N0	VCCINT			38	61								
B3	VREFB3N0	IO	DIFFIO_B1n				P3	V1			DM3B/BWS#3B	DM5B1/BWS#5B2		
B3	VREFB3N0	GND				62								
B3	VREFB3N0	IO	DIFFIO_B2p		39	63	R3	M6			DQ3B	DQ5B		
B3	VREFB3N0	IO	DIFFIO_B2n			64	T3	N6						
B3	VREFB3N0	IO	DIFFIO_B3p			65		T4						
B3	VREFB3N0	VCCIO3			40	66								
B3	VREFB3N0	GND			41	67								
B3	VREFB3N0	IO			42	68	T2	P6	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2
B3	VREFB3N0	IO	PLL1_CLKOUTp		43	69	R4	U2						
B3	VREFB3N0	IO	PLL1_CLKOUTn		44	70	T4	V2						
B3	VREFB3N0	IO	DIFFIO_B4p			71	N5				DQ3B	DQ5B		
B3	VREFB3N0	IO	DIFFIO_B4n			72	N6	N7			DQ3B	DQ5B		
B3	VREFB3N0	IO				73	M6	N8			DQ3B	DQ5B		
B3	VREFB3N0	VCCINT			45	74								
B3	VREFB3N0	GND				75								
B3	VREFB3N0	IO						P7						
B3	VREFB3N0	IO	VREFB3N0		46	76	P6	T6						
B3	VREFB3N0	VCCIO3			47	77								
B3	VREFB3N0	IO	DIFFIO_B5p			78	M7	U3		DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2
B3	VREFB3N0	GND			48	79								
B3	VREFB3N0	IO	DIFFIO_B5n					V3					DM3B/BWS#3B	DM5B1/BWS#5B2
B3	VREFB3N0	IO						N9						
B3	VREFB3N0	IO	DIFFIO_B6p				R5	U4			DQ3B	DQ5B	DQ3B	DQ5B

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B3	VREFB3N0	IO	DIFFIO_B6n			80	T5	V4		DM5B/BWS#5B			DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B7p			81	R6	U5		DQ5B	DQ3B	DQ5B		
B3	VREFB3N0	IO	DIFFIO_B7n			82	T6	V5		DQ5B			DQ3B	DQ5B
B3	VREFB3N0	IO					L7				DQ3B	DQ5B		
B3	VREFB3N0	IO	DIFFIO_B8p				R7	R8			DQ3B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B8n			83	T7	T8		DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3
B3	VREFB3N0	IO	DIFFIO_B9p					P8						
B3	VREFB3N0	IO	DIFFIO_B9n		49	84	L8	P9	DQ1B		DQ3B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	VCCINT				85								
B3	VREFB3N0	IO	DIFFIO_B10p					U6					DQ3B	DQ5B
B3	VREFB3N0	GND				86								
B3	VREFB3N0	IO	DIFFIO_B10n		50	87	M8	V6	DQ1B	DQ5B	DM5B/BWS#5B	DM5B0/BWS#5B1	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B11p		51	88	N8	U7	DQ1B	DQ5B	DQ5B	DQ5B		
B3	VREFB3N0	IO	DIFFIO_B11n					V7					DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B12p					U8					DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B12n				P8	V8			DQ5B	DQ5B	DM5B/BWS#5B	DM5B0/BWS#5B1
B3	VREFB3N0	CLK15	DIFFCLK_6p		52	89	R8	U9						
B3	VREFB3N0	CLK14	DIFFCLK_6n		53	90	T8	V9						
B4	VREFB4N0	CLK13	DIFFCLK_7p		54	91	R9	U10						
B4	VREFB4N0	CLK12	DIFFCLK_7n		55	92	T9	V10						
B4	VREFB4N0	IO	DIFFIO_B13p			93		U11		DQ5B			DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B13n			94		V11		DQ5B				
B4	VREFB4N0	IO	DIFFIO_B14p					U12					DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B14n			95	N9	V12			DQ5B	DQ5B		
B4	VREFB4N0	VCCIO4			56	96								
B4	VREFB4N0	GND			57	97								
B4	VREFB4N0	IO	DIFFIO_B16p		58	98	R10	U13	DQ1B	DQ5B	DQ5B	DQ5B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B16n			99	T10	V13		DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4
B4	VREFB4N0	IO	DIFFIO_B17p		59		R11	P10	DQ1B		DQ5B	DQ5B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B17n		60	100	T11	P11	DQ1B	DQ5B				
B4	VREFB4N0	VCCINT			61	101								
B4	VREFB4N0	IO	DIFFIO_B18p				R12	U14			DQ5B	DQ5B	DQ5B	DQ5B
B4	VREFB4N0	GND				102								
B4	VREFB4N0	IO	DIFFIO_B18n			103	T12	V14		DQ5B	DQ5B	DQ5B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B19p					U15						
B4	VREFB4N0	IO	DIFFIO_B19n					V15					DQ5B	DQ5B
B4	VREFB4N0	VCCIO4			62	104								
B4	VREFB4N0	IO						R11					DQ5B	DQ5B
B4	VREFB4N0	GND			63	105								
B4	VREFB4N0	IO			64	106	P9	P12		DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5
B4	VREFB4N0	IO	VREFB4N0		65	107	P11	T11						
B4	VREFB4N0	IO	DIFFIO_B20p			108	R13	U16						
B4	VREFB4N0	IO	DIFFIO_B20n			109	T13	V16			DQ5B	DQ5B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B21p					N10						
B4	VREFB4N0	IO	DIFFIO_B21n			110		N11						
B4	VREFB4N0	IO	RUP2		66	111	M10	T13	DQ1B					
B4	VREFB4N0	IO	RDN2		67	112	N11	T14	DQ1B					
B4	VREFB4N0	IO	DIFFIO_B22p					U17						
B4	VREFB4N0	IO	DIFFIO_B22n					V17						
B4	VREFB4N0	IO	DIFFIO_B23p				T14				DQ5B	DQ5B		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B4	VREFB4N0	IO	DIFFIO_B23n		68	113	T15	R13	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3
B4	VREFB4N0	IO	DIFFIO_B24p		69	114	N12	P13						
B4	VREFB4N0	VCCINT			70	115								
B4	VREFB4N0	IO	DIFFIO_B24n					N12						
B4	VREFB4N0	GND				116								
B4	VREFB4N0	IO	PLL4_CLKOUTp		71	117	P14	U18						
B4	VREFB4N0	IO	PLL4_CLKOUTn		72	118	R14	V18						
B4	VREFB4N0	IO	DIFFIO_B25p			119		M13						
B4	VREFB4N0	IO	DIFFIO_B25n			120		N13						
B5	VREFB5N0	VCCD_PLL4			73	121	N13	P15						
B5	VREFB5N0	GNDA4			74	122	M12	P14						
B5	VREFB5N0	VCCA4			75	123	L12	N14						
B5	VREFB5N0	VCCIO5				124								
B5	VREFB5N0	IO						N15					DM3R/BWS#3R	DM1R1/BWS#1R2
B5	VREFB5N0	GND				125								
B5	VREFB5N0	IO	RUP3		76	126	N14	T16		DQ1R	DM1R/BWS#1R		DQ3R	DQ1R
B5	VREFB5N0	IO	RDN3		77	127	P15	R16		DQ1R	DQ1R			
B5	VREFB5N0	IO	DIFFIO_R15n			128	P16	T18		DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4
B5	VREFB5N0	IO	DIFFIO_R15p				R16	T17			DQ1R		DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R14n					R18						
B5	VREFB5N0	VCCINT			78	129								
B5	VREFB5N0	IO	DIFFIO_R14p					R17						
B5	VREFB5N0	GND				130								
B5	VREFB5N0	IO	DIFFIO_R13n		79	131	N16	P18		DQ1R	DQ1R		DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R13p			132	N15	P17		DQ1R	DQ1R		DQ3R	DQ1R
B5	VREFB5N0	IO	VREFB5N0		80	133	L14	N16						
B5	VREFB5N0	IO	DIFFIO_R12n			134		M14		DQ1R			DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R12p			135	L13	L13		DQ1R	DQ1R		DQ3R	DQ1R
B5	VREFB5N0	VCCIO5			81	136								
B5	VREFB5N0	IO	DIFFIO_R11n			137	L16	L15		DQ1R	DQ1R		DQ3R	DQ1R
B5	VREFB5N0	GND			82	138								
B5	VREFB5N0	IO	DIFFIO_R11p		83	139	L15	L14					DQ3R	DQ1R
B5	VREFB5N0	VCCINT			84	140								
B5	VREFB5N0	GND				141								
B5	VREFB5N0	IO	DIFFIO_R10n			142	K16	M17			DQ1R		DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R10p		85	143	K15	L16	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6
B5	VREFB5N0	IO	DIFFIO_R9n	DEV_OE	86	144	J16	M18						
B5	VREFB5N0	IO	DIFFIO_R9p	DEV_CLRn	87	145	J15	L17						
B5	VREFB5N0	IO	DIFFIO_R8n			146	J14	L18			DQ1R			
B5	VREFB5N0	IO	DIFFIO_R8p					K18					DM1R/BWS#1R	DM1R0/BWS#1R1
B5	VREFB5N0	IO	DIFFIO_R7n			147	J13	K17			DQ1R		DQ1R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R7p			148								
B5	VREFB5N0	CLK7	DIFFCLK_3n		88	149	M16	N18						
B5	VREFB5N0	CLK6	DIFFCLK_3p		89	150	M15	N17						
B6	VREFB6N0	CLK5	DIFFCLK_2n		90	151	E16	F18						
B6	VREFB6N0	CLK4	DIFFCLK_2p		91	152	E15	F17						
B6	VREFB6N0	CONF_DONE		CONF_DONE	92	153	H14	K14						
B6	VREFB6N0	VCCIO6			93	154								
B6	VREFB6N0	MSEL0		MSEL0	94	155	H13	K13						
B6	VREFB6N0	GND			95	156								
B6	VREFB6N0	MSEL1		MSEL1	96	157	H12	J18						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B6	VREFB6N0	MSEL2		MSEL2	97	158	G12	J17						
B6	VREFB6N0	MSEL3		MSEL3 (1)				J14						
B6	VREFB6N0	IO	DIFFIO_R6n				H16	H18						
B6	VREFB6N0	IO	DIFFIO_R6p				H15	H17					DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R5n	INIT_DONE	98	159	G16	G18						
B6	VREFB6N0	IO	DIFFIO_R5p	CRC_ERROR	99	160	G15	G17						
B6	VREFB6N0	IO			100	161	F13	J13						
B6	VREFB6N0	IO	DIFFIO_R4n	nCEO	101	162	F16	E18						
B6	VREFB6N0	VCCINT			102	163								
B6	VREFB6N0	IO	DIFFIO_R4p	CLKUSR	103	164	F15	E17						
B6	VREFB6N0	GND				165								
B6	VREFB6N0	IO			104	166	B16	H16	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7
B6	VREFB6N0	IO	DIFFIO_R3n	nWE		167		D18					DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R3p	nOE		168		D17					DQ1R	DQ1R
B6	VREFB6N0	IO	VREFB6N0		105	169	F14	H15						
B6	VREFB6N0	IO		nAVD				H14					DQ1R	DQ1R
B6	VREFB6N0	VCCIO6				170								
B6	VREFB6N0	IO				171	D16	H13		DQ1R			DQ1R	DQ1R
B6	VREFB6N0	GND				172								
B6	VREFB6N0	IO		PADD23		173	D15	G14					DQ1R	DQ1R
B6	VREFB6N0	VCCINT				174								
B6	VREFB6N0	IO	DIFFIO_R2n	PADD22				C18					DQ1R	DQ1R
B6	VREFB6N0	GND				175								
B6	VREFB6N0	IO	DIFFIO_R2p	PADD21				C17					DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R1n	PADD20	106	176	C16	B18		DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5
B6	VREFB6N0	IO	DIFFIO_R1p			177	C15	B17						
B6	VREFB6N0	VCCA2			107	178	F12	F14						
B6	VREFB6N0	GNDA2			108	179	E12	F15						
B6	VREFB6N0	VCCD_PLL2			109	180	D13	E15						
B7	VREFB7N0	IO	DIFFIO_T24n				C14	F13						
B7	VREFB7N0	IO	DIFFIO_T24p			181	D14	G13			DQ5T	DQ5T		
B7	VREFB7N0	IO	DIFFIO_T23n			182	D11	C16						
B7	VREFB7N0	IO	DIFFIO_T23p		110	183	D12	D16	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6
B7	VREFB7N0	IO	DIFFIO_T22n				A13	A18					DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T22p		111	184	B13	A17			DQ5T	DQ5T		
B7	VREFB7N0	IO	PLL2_CLKOUTn		112	185	A14	C14						
B7	VREFB7N0	IO	PLL2_CLKOUTp		113	186	B14	D14						
B7	VREFB7N0	IO	RUP4		114	187	E11	E14	DQ1T					
B7	VREFB7N0	IO	RDN4		115	188	E10	E13	DQ1T					
B7	VREFB7N0	IO				189								
B7	VREFB7N0	VCCINT			116	190								
B7	VREFB7N0	IO	DIFFIO_T21n				A12				DQ5T	DQ5T		
B7	VREFB7N0	GND				191								
B7	VREFB7N0	IO	DIFFIO_T21p				B12	F12			DQ5T	DQ5T		
B7	VREFB7N0	VCCIO7			117	192								
B7	VREFB7N0	IO	DIFFIO_T20n				A11				DQ5T	DQ5T		
B7	VREFB7N0	GND			118	193								
B7	VREFB7N0	IO	DIFFIO_T20p	PADD0		194	B11	E12		DQ5T	DQ5T	DQ5T	DQ5T	DQ5T
B7	VREFB7N0	IO	VREFB7N0		119	195	C11	D12						
B7	VREFB7N0	IO	DIFFIO_T19n	PADD1	120	196	A15	A16	DQ1T					
B7	VREFB7N0	IO	DIFFIO_T19p	PADD2		197		B16		DQ5T			DQ5T	DQ5T

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B7	VREFB7N0	IO	DIFFIO_T18n					F11						
B7	VREFB7N0	IO	DIFFIO_T18p					F10						
B7	VREFB7N0	IO						C12						
B7	VREFB7N0	VCCINT				198								
B7	VREFB7N0	IO	DIFFIO_T17n	PADD3				A15					DQ5T	DQ5T
B7	VREFB7N0	GND				199								
B7	VREFB7N0	IO	DIFFIO_T17p	PADD4	121	200	F9	B15		DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8
B7	VREFB7N0	VCCIO7			122									
B7	VREFB7N0	IO	DIFFIO_T16n	PADD5		201	A10	A14		DQ5T	DQ5T	DQ5T	DQ5T	DQ5T
B7	VREFB7N0	GND			123									
B7	VREFB7N0	IO	DIFFIO_T16p	PADD6			B10	B14			DQ5T	DQ5T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T15n	PADD7		202	C9	A13		DQ5T	DQ5T	DQ5T		
B7	VREFB7N0	IO	DIFFIO_T15p	PADD8		203	D9	B13			DM5T/BWS#5T	DM5T0/BWS#5T1	DQ5T	DQ5T
B7	VREFB7N0	VCCINT			124	204								
B7	VREFB7N0	GND				205								
B7	VREFB7N0	IO	DIFFIO_T14n	PADD9				A12					DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T14p	PADD10				B12						
B7	VREFB7N0	IO	DIFFIO_T13n	PADD11				A11					DQ5T	DQ5T
B7	VREFB7N0	VCCIO7				206								
B7	VREFB7N0	IO	DIFFIO_T13p	PADD12	125	207	E9	B11		DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9
B7	VREFB7N0	GND				208								
B7	VREFB7N0	IO						E11						
B7	VREFB7N0	IO	DIFFIO_T12n	PADD13				C10					DM5T/BWS#5T	DM5T0/BWS#5T1
B7	VREFB7N0	IO	DIFFIO_T12p	PADD14				D10						
B7	VREFB7N0	CLK8	DIFFCLK_5n		126	209	A9	A10						
B7	VREFB7N0	CLK9	DIFFCLK_5p		127	210	B9	B10						
B8	VREFB8N0	CLK10	DIFFCLK_4n		128	211	A8	A9						
B8	VREFB8N0	CLK11	DIFFCLK_4p		129	212	B8	B9						
B8	VREFB8N0	IO		PADD15				E10						
B8	VREFB8N0	IO	DIFFIO_T11n	PADD16				C9					DQ3T	DQ5T
B8	VREFB8N0	VCCIO8			130	213								
B8	VREFB8N0	IO	DIFFIO_T11p	PADD17		214	C8	D9		DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10
B8	VREFB8N0	GND			131	215								
B8	VREFB8N0	IO				216	D8	E9			DQ3T	DQ5T		
B8	VREFB8N0	IO				217				DQ5T				
B8	VREFB8N0	IO	DIFFIO_T10n	DATA2	132	218	E8	A8	DQ1T		DQ3T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T10p	DATA3	133	219	F8	B8	DQ1T	DQ5T				
B8	VREFB8N0	IO	DIFFIO_T9n	PADD18			A7	A7			DQ3T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	VCCINT			134	220								
B8	VREFB8N0	IO	DIFFIO_T9p	DATA4	135	221	B7	B7	DQ1T	DQ5T	DQ3T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	GND				222								
B8	VREFB8N0	IO	DIFFIO_T8n	PADD19				A6					DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T8p	DATA15				B6						
B8	VREFB8N0	IO	VREFB8N0		136	223	C6	C7						
B8	VREFB8N0	IO	DIFFIO_T7n	DATA14		224	A6	A5		DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11
B8	VREFB8N0	IO	DIFFIO_T7p	DATA13			B6	B5			DQ3T	DQ5T		
B8	VREFB8N0	VCCIO8				225								
B8	VREFB8N0	IO		DATA5	137	226	E7	C5	DQ1T	DQ5T	DQ3T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	GND				227								
B8	VREFB8N0	IO						D7						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
B8	VREFB8N0	VCCINT			138	228								
B8	VREFB8N0	GND				229								
B8	VREFB8N0	IO	DIFFIO_T6n			230		F9						
B8	VREFB8N0	IO	DIFFIO_T6p	DATA6		231	E6	E8		DQ5T	DQ3T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T5n	DATA7		232	A5	A4		DM5T/BWS#5T	DQ3T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T5p	DATA8			B5	B4			DQ3T	DQ5T		
B8	VREFB8N0	IO	DIFFIO_T4n	DATA9			D6	E7					DQ3T	DQ5T
B8	VREFB8N0	VCCIO8			139									
B8	VREFB8N0	IO	DIFFIO_T4p					F8						
B8	VREFB8N0	GND			140									
B8	VREFB8N0	IO	DIFFIO_T3n	DATA10			A4	A3			DM3T/BWS#3T	DM5T1/BWS#5T2	DM3T/BWS#3T	DM5T1/BWS#5T2
B8	VREFB8N0	IO	DIFFIO_T3p	DATA11		233	B4	B3						
B8	VREFB8N0	IO	DIFFIO_T2n			234	A2	E6						
B8	VREFB8N0	IO	DIFFIO_T2p		141	235	A3	F7						
B8	VREFB8N0	IO					D5	F6						
B8	VREFB8N0	IO		DATA12	142	236	B3	D5	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7
B8	VREFB8N0	IO	DIFFIO_T1n			237								
B8	VREFB8N0	IO	DIFFIO_T1p			238								
B8	VREFB8N0	IO	PLL3_CLKOUTn		143	239	C3	A1	DQ1T					
B8	VREFB8N0	IO	PLL3_CLKOUTp		144	240	D3	A2	DM1T					
B8	VREFB8N0	IO						G6						
		VCCINT					F7	G7						
		VCCINT					F11	G8						
		VCCINT					G6	G10						
		VCCINT					G7	G11						
		VCCINT					G8	G12						
		VCCINT					G9	H7						
		VCCINT					G10	H12						
		VCCINT					H6	J7						
		VCCINT					H11	J12						
		VCCINT					J6	K7						
		VCCINT					K7	K12						
		VCCINT					K11	L7						
		VCCINT					L6	L12						
		VCCINT					K9	M7						
		VCCINT					K10	M8						
		VCCINT					M9	M9						
		VCCINT					M11	M11						
		VCCINT					J12	M12						
		VCCIO1					E3	F4						
		VCCIO1					G3	G4						
		VCCIO1						J4						
		VCCIO2					K3	K4						
		VCCIO2					M3	M4						
		VCCIO2						N4						
		VCCIO3					P4	R6						
		VCCIO3					P7	R7						
		VCCIO3					T1	R9						
		VCCIO4					P10	R10						
		VCCIO4					P13	R12						
		VCCIO4					T16	R14						
		VCCIO5					K14	K15						
		VCCIO5					M14	M15						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
		VCCIO5						R15						
		VCCIO6					E14	F16						
		VCCIO6					G14	G15						
		VCCIO6						J15						
		VCCIO7					A16	D11						
		VCCIO7					C10	D13						
		VCCIO7					C13	D15						
		VCCIO8					A1	D4						
		VCCIO8					C4	D6						
		VCCIO8					C7	D8						
		GND					H7	G9						
		GND					H8	H9						
		GND					H9	H8						
		GND					H10	J8						
		GND					J7	J9						
		GND					J8	J10						
		GND					J9	H10						
		GND					J10	H11						
		GND					F6	J11						
		GND					F10	K11						
		GND					J11	K10						
		GND					K8	K9						
		GND					K6	K8						
		GND					L9	L8						
		GND					L10	L9						
		GND					L11	L10						
		GND					K12	M10						
		GND					G11	L11						
		GND					B2	C15						
		GND					B15	C13						
		GND					C5	C11						
		GND					C12	C8						
		GND					D7	C6						
		GND					D10	C4						
		GND					E4	E3						
		GND					E13	G3						
		GND					G4	J3						
		GND					G13	K3						
		GND					K4	N3						
		GND					K13	P3						
		GND					M4	T5						
		GND					M13	T7						
		GND					N7	T9						
		GND					N10	T10						
		GND					P5	T12						
		GND					P12	T15						
		GND					R2	P16						
		GND					R15	M16						
		GND						J16						

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	E144 (4)	Q240	F256/ U256	F324	DQS for x8/x9 in E144	DQS for x8/x9 in Q240	DQS for x8/x9 in F256/U256	DQS for x16/x18 in F256/U256	DQS for x8/x9 in F324	DQS for x16/x18 in F324
		GND						K16						
		GND						G16						
		GND						E16						

Notes:

(1) E144, Q240, and F256 in the EP3C25 device do not have the MSEL [3] pin and do not support the Active Parallel (AP) configuration mode.

(2) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(3) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.

(4) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity, and not for thermal purposes.

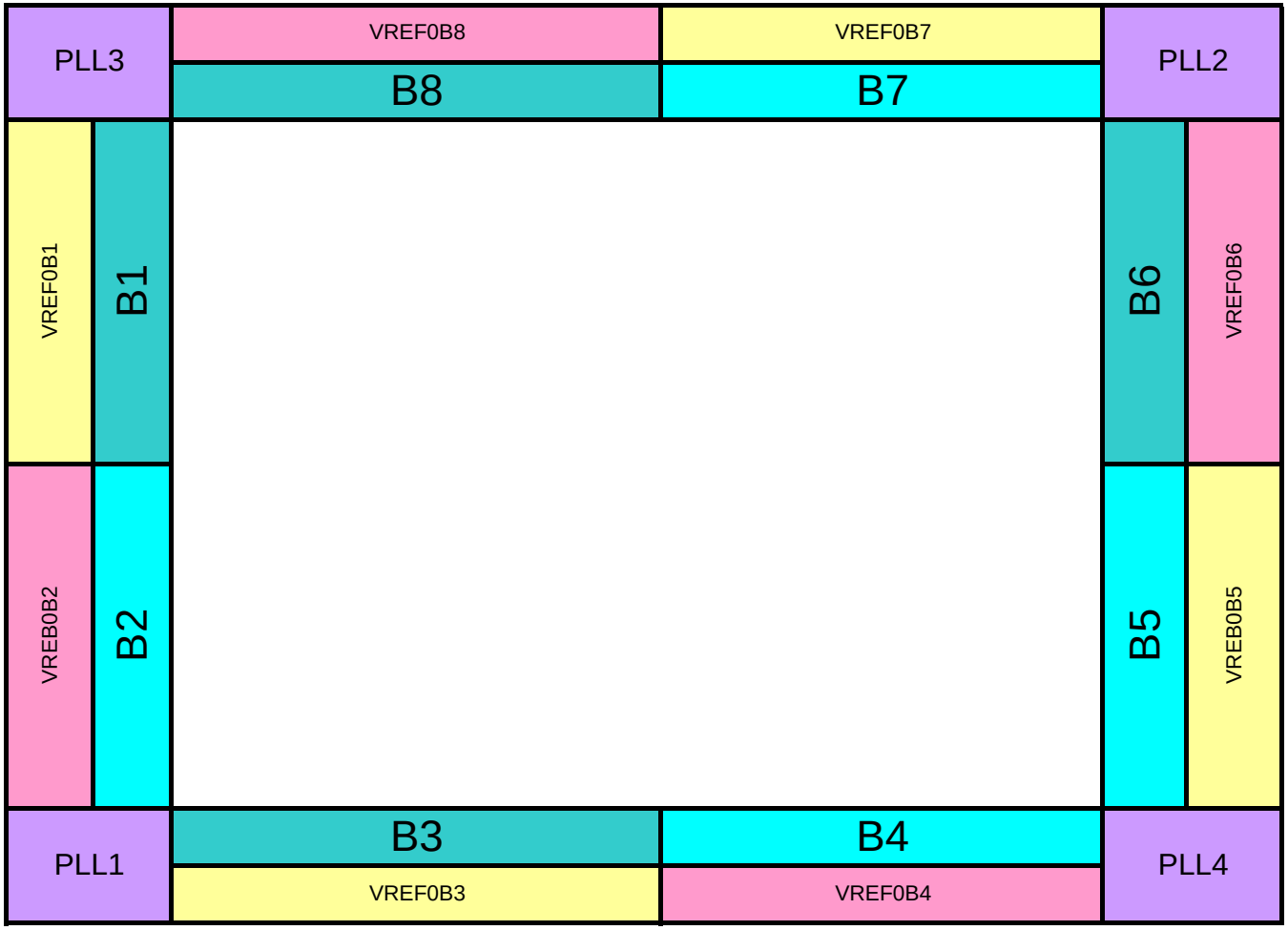
Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI, and TDO) and the following configuration pins: nCONFIG, DCLK, DATA[15..0], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO and CLKUSR.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank. If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA[1..4]	Power	Supply (analog) voltage for PLLs[1..4] and other analog circuits in the device.
VCCD_PLL[1..4]	Power	Supply (digital) voltage for PLLs[1..4].
RUP[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank. If not required, this pin is a regular I/O pin.
RDN[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank. If not required, this pin is a regular I/O pin.
GNDA[1..4]	Ground	Ground for PLL[1..4]. You can connect these pins to GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
	Dedicated Configuration/JTAG Pins	
DATA0	Input (PS, FPP, AS) Bidirectional open drain (AP)	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or PP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA0 is a dedicated bidirectional pin with optional user control.
MSEL[3..0]	Input	Configuration input pins that set the Cyclone III device configuration scheme. These pins must be hardwired to VCCA or GND. Some of the smaller devices or package options do not support the AP flash programming and do not have the MSEL[3] pin.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin.
	Clock and PLL Pins	
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
PLL[1..4]_CLKOUT[p,n]	I/O, Output	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.These pins can only use the differential I/O standard if it is being fed by a PLL output.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
		Optional/Dual-Purpose Configuration Pins
DCLK	Input (PS, FPP) I/O, Output (AS, AP)	Configuration clock pin. In PS and PP configuration modes, DCLK is used to clock configuration data from an external source into the Cyclone III device. In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. After AS or AP configuration, this pin is available as a user I/O pin with optional user control.
nCEO	I/O, Output	Output that drives low when device configuration is complete.
FLASH_nCE, nCSO	I/O, Output	This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active. nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.
DATA1, ASDO	Input (FPP) Output (AS) Bidirectional open-drain (AP)	This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA1 is a dedicated bidirectional pin with optional user control. ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.
DATA[7..2]	Input (FPP) Bidirectional open-drain (AP)	Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings. After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control.
DATA[15..8]	Bidirectional open-drain (AP)	Data inputs. Btye-wide or word-wide configuration data is presented to the target device on DATA[15..0]. In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15..8] are dedicated bidirectional pins with optional user control.
PADD[23..0]	I/O, Output (AP)	24-bit address bus from the Cyclone III device to the parallel flash in AP mode.
nRESET	I/O, Output (AP)	Active-low reset output. Driving the nRESET pin low resets the parallel flash.
nAVD	I/O, Output (AP)	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus.
nOE	I/O, Output (AP)	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0]).
nWE	I/O, Output (AP)	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.This pin can be set in Quartus II software to support open-drain output.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Dual-Purpose Differential and External Memory Interface Pins		
DIFFIO_[L,R,T,B][0..61][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7]	I/O, DQS/CQ, CDPCLK	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[0..5][L,R,T,B]	I/O, DQ	Optional data signal for use in external memory interfaces.
DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.

Note:

(1) The pin definitions are prepared based on the device with the largest density, EP3C120. Refer to the pin list for the availability of pins in each density.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Changes Made	Date
1.0	Initial release.	3/19/2007
1.1	Updated pin description for MSEL pins. Changed to connecting to VCCA instead of VCCPD.	5/24/2007
	Added I/O to pin type for dual-purpose configuration pins.	
1.2	Updated Note(2) in Pin List.	11/29/2007
1.3	Updated pin function for CRC_ERROR pin	5/13/2008
	Updated pin function for PLL[1..4]_CLKOUT[p,n] pin	
	Remove RDY from pin list and pin definitions	
	Incorporated pin connection guideline into Pin Definitions worksheet	
	Incorporated VCCA and VCCD Decoupling recommendations	
1.4	Removed Pin Connection Guideline from Pin Definitions worksheet.	10/7/2009
	Removed VCCA and VCCD Decoupling recommendations.	
	Removed PKG notes from Pin List Worksheet.	
	Updated pin function for DCLK pin.	