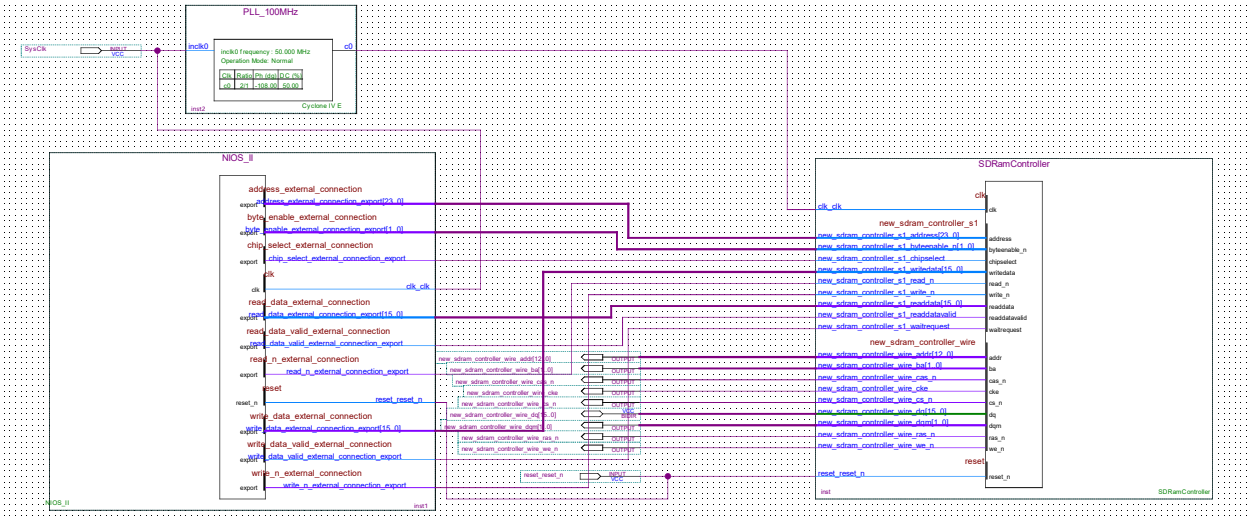
PLL_100MHz
SysClk
inclk0
c0
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Cyclone IV E
inst2
NIOS_II
address_external_connection
byte_enable_external_connection
chip_select_external_connection
clk
read_data_external_connection
read_data_valid_external_connection
read_n_external_connection
reset
write_data_external_connection
write_data_valid_external_connection
write_n_external_connection
inst1
SDRamController
new_sdram_controller_s1
new_sdram_controller_wire
inst