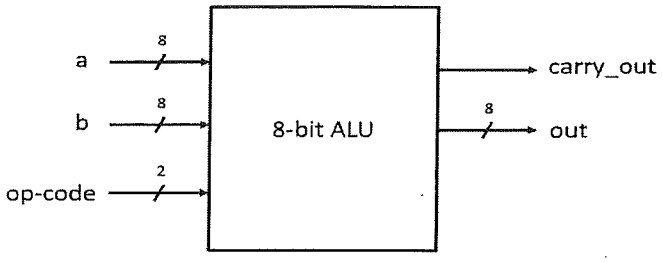
Design an 8-bit Arithmetic Logic Unit (ALU) that performs the following operations:

- Addition
- Subtraction
- 2's complement for one of the two operands
- Bit-wise Exclusive OR

Description:
Your design should have a single 8-bit output and a carry line. There should be two 8-bit inputs and an operation code (op-code) to select the operation as shown in the figure.



Use the following op-codes for the four functions:

Operation	Op-code
Addition	00
Subtraction	01
2's complement	10
Bit-wise XOR	11

Goal:

- Implement the ALU in Verilog or VHDL (The design should be synthesizable).
- Simulate your design to demonstrate the working of all four operations.
- Minimize the hardware logic. (EXTRA CREDIT!)

Submission guidelines:

- Use the Verilog template file uploaded on blackboard.
- Submit the compressed version of Quartus project on blackboard.
- A lab report (in hard form) should be submitted in class. It should have the following contents:
  - Design description using block diagram
  - Snapshots of the RTL schematic and simulations
  - Logic Utilization (Give numbers! Explain your approach to minimize hardware logic)
  - Conclusion
  - Verilog/VHDL code