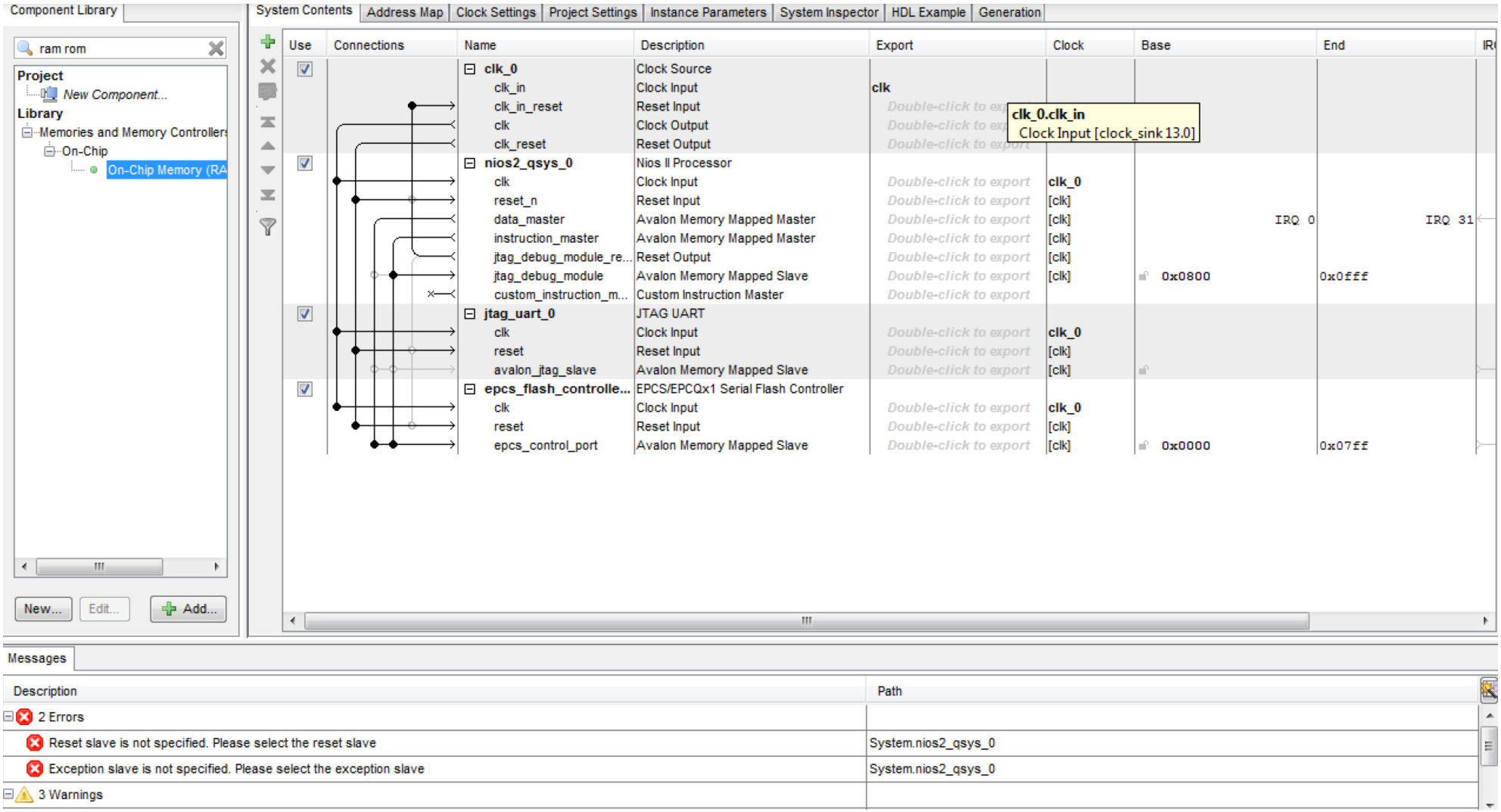
Component Library
ram rom
Project
New Component...
Library
Memories and Memory Controllers
On-Chip
On-Chip Memory (RA
New...
Edit...
Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
End
clk_0
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
clk
Clock Output
clk_reset
Reset Output
clk_0.clk_in
Clock Input [clock_sink 13.0]
nios2_qsys_0
Nios II Processor
clk
Clock Input
Double-click to export
clk_0
reset_n
Reset Input
[clk]
data_master
Avalon Memory Mapped Master
IRQ 0
IRQ 31
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
0x0800
0x0fff
custom_instruction_m...
Custom Instruction Master
jtag_uart_0
JTAG UART
avalon_jtag_slave
epcs_flash_controlle...
EPCS/EPCQx1 Serial Flash Controller
epcs_control_port
0x0000
0x07ff
Messages
Description
Path
2 Errors
Reset slave is not specified. Please select the reset slave
System.nios2_qsys_0
Exception slave is not specified. Please select the exception slave
System.nios2_qsys_0
3 Warnings