Cyclone® IV Device Family Pin Connection Guidelines
PCG-01008- 1.0

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Cyclone® IV Device Family Pin Connection Guidelines
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Cyclone IV Devices Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[5, 7, 9, 11, 12,14], DIFFCLK_[2..7]p Note 9	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND. See Note 12.
CLK[4, 6, 8, 10, 13, 15], DIFFCLK_[2..7]n Note 9	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND. See Note 12.
PLL[1..8]_CLKOUTp Note 10	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..8]. Each pin can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Quartus II software. See Note 12.
PLL[1..8]_CLKOUTn Note 10	I/O, Output	Optional negative terminal for external clock outputs from PLL [1..8]. Each pin can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Quartus II software. See Note 12.
Configuration/ JTAG Pins			
MSEL[0..3]	Input	Configuration input pins that set the Cyclone IV device configuration scheme. The smaller devices like EP4CGX15, EP4CGX22, and EP4CGX30 do have the MSEL3 pin.	These pins are internally connected through a 9-KΩ resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND. Refer to the "Configuration and Remote System Upgrades in Cyclone IV Devices" chapter in the Cyclone IV Handbook. If only JTAG configuration is used, connect these pins to GND.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In a multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If you are using PS configuration scheme with a download cable, connect this pin through a 10-KΩ resistor to VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-KΩ resistor to VCCIO.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.	This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-KΩ pull-up resistor.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.	When not using this pin, you can leave it unconnected. During multi-device configuration, this pin feeds the nCE pin of a subsequent device. In this case, tie the 10-KΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. During single device configuration, this pin can be used as a regular I/O.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.	This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-KΩ pull-up resistor.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-KΩ pull-down resistor to GND. To disable the JTAG circuitry connect TCK to GND.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 10-KΩ pull-up resistor to VCCA. (Note 13) To disable the JTAG circuitry connect TMS to VCCA.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 10-KΩ pull-up resistor to VCCA. (Note 13) To disable the JTAG circuitry connect TDI to VCCA.
TDO	Output	Dedicated JTAG test data output pin.	If the TDO pin is not used, leave this pin unconnected.
nCSO	I/O, Output(AS)	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode, nCSO is not used. If the pin is not used as an I/O, you should leave the pin unconnected.
DATA1, ASDO	Input (PS, FPP) Output (AS)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide configuration data is presented to the target device on DATA[0..7]. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual- Purpose Pin settings. ASDO: Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode, this pin is available as a user I/O pin. If the pin is not used as an I/O, then you should leave the pin unconnected.
DATA[2..7]	Input (FPP)	Data inputs. Byte-wide configuration data is presented to the target device on DATA [0..7]. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.	When not programming the device in AS mode, this pin is available as a user I/O pin. If the pin is not used as an I/O you should leave the pin unconnected.

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Cyclone IV Devices Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.	When using this pin, connect it to an external 10-KΩ pull-up resistor to an acceptable voltage for all devices in the chain that satisfies the input voltage of the receiving device. When not using this pin, it can be left floating.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O, tie this pin to GND.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O, then you should tie this pin to GND.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	If you are using a serial configuration device in AS configuration mode, you must connect a 25-Ω series resistor at the near end of the serial configuration device for the DATA0. When the dedicated input for DATA0 is not used and this pin is not used as an I/O, then you should to leave this pin unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	When using this pin, connect it to an external 10-KΩ pull-up resistor to an acceptable voltage for all devices in the chain that satisfies the input voltage of the receiving device. When not using this pin, it can be left floating or tied to GND.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, then you should connect this pin to GND.
Differential I/O Pins			
DIFFIO_[R,T,B][0..72][p,n] Note 14	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these IO pins are not used, they can be tied to GND. See Note 12.
External Memory Interface Pins			
DQS[0..5][R,T,B]/CQ[0,1,3,5][R,T,B]#, DPCLK[0..17] Note 15	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these IO pins are not used, they can be tied to GND. See Note 12.
DQ[0..5][R,T,B] Note 15	I/O, DQ	Optional data signal for use in external memory interface.	When these IO pins are not used, they can be tied to GND. See Note 12.
DM[0..5][R,T,B]/BWS#[0..5][R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.	When these IO pins are not used ,they can be tied to GND. See Note 12.
Reference Pins			
RUP[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.	When using OCT tie these pins to the required banks VCCIO through either a 25 Ω or 50 Ω resistor, depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to VCCIO of the bank in which the RUP pin resides or GND.
RDN[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.	When using OCT tie these pins to GND through either a 25 Ω or 50 Ω resistor depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to GND.

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NC	No Connect	Do not drive signals into these pins.	When designing for device migration, these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.
***Supply Pins** (See Notes 16 and 17)*			
VCCINT	Power	These are internal logic array voltage supply pins.	All VCCINT pins must be connected to a 1.2 V supply. Can share VCCD_PLL and VCCL_GXB with VCCINT with proper isolation filters. Decoupling depends on the design decoupling requirements of the specific board. See Notes 3 and 5.
VCCD_PLL	Power	Digital power for PLLs[1..8]. The designer must power up these pins, even if the PLL is not used.	You are required to connect these pins to 1.2 V, even if the PLL is not used. With a proper isolation filter these pins can be sourced from the same regulator as VCCINT and VCCL_GXB. Use an isolated switching power supply with ± 3 % maximum voltage ripple. (Note 11) Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 5, and 8.
VCCA	Power	Analog power for PLLs[1..8]. All VCCA pins must be powered and all VCCA pins must be powered up and powered down at the same time even if not all the PLLs are used. Designer is advised to keep this pin isolated from other VCC pins for better jitter performance.	You are required to connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear or switching power supply with ± 3 % maximum voltage ripple. (Note 11) It is advised to keep this pin isolated from other VCC for better jitter performance. These pins can share the same regulator as VCCA_GXB and VCCH_GXB with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 5, 6, and 8.
VCCIO[3..9]	Power	These are I/O supply voltage pins for banks 3 through 9. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards.	Connect VCCIO pins on banks 4, 5, 6, and 7 to 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V supplies, depending on the I/O standard connected to the specified bank. I/O banks 3, 8, and 9 contain configuration pins. VCCIO pins on banks 3 and 9 support only 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V. If FPP configuration is used, connect VCCIO pins on bank 8 to similar voltage level as banks 3 and 9. When these pins require 2.5 V, can share VCCH_GXB, VCCA_GXB, VCCA, and/or VCC_CLKIN with a common 2.5 V supply with proper isolation filters. See Notes 3 and 5.
VCC_CLKIN[3,8]	Power	Differential clock input power supply for banks 3 and 8.	These pins can be tied to the same 2.5 V plane as VCCA, but only if each of these supplies require 2.5 V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
GND	Ground	Device ground pins.	All GND pins should be connected to the board GND plane.
VREFB[3..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 3.
***Transceiver Pins** (See Notes 16 and 17)*			
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.	Connect VCCL_GXB to a 1.2 V supply. With a proper isolation filter these pins can be sourced from the same regulator as VCCINT and VCCD_PLL. Use an isolated switching power supply with ± 3 % maximum voltage ripple. (Note 11) Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 5, and 6.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.	Connect VCCH_GXB to a 2.5 V supply. These pins can be tied to the same 2.5 V plane as VCCA_GXB. Use an isolated linear or switching power supply with ± 3 % maximum voltage ripple. (Note 11) These pins may be sourced from the same regulator as VCCA with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 5, and 6.
VCCA_GXB	Power	Supplies power to the transceiver PMA regulator.	Connect VCCA_GXB to a 2.5 V supply. These pins may be tied to the same 2.5 V plane as VCCH_GXB. Use an isolated linear or switching power supply with ± 3 % maximum voltage ripple. (Note 11) These pins may be sourced from the same linear regulator as VCCA with a proper isolation filter. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 3, 5, and 6.
GXB_RX[0..7]p	Input	High speed positive differential receiver channels.	These pins may be AC-coupled or DC-coupled when used. (Note 4) Connect all unused GXB_RXp pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible. See Note 7.
GXB_RX[0..7]n	Input	High speed negative differential receiver channels.	These pins may be AC-coupled or DC-coupled when used. (Note 4) Connect all unused GXB_RXn pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible. See Note 7.
GXB_TX[0..7]p	Output	High speed positive differential transmitter channels.	Leave all unused GXB_TXp pins floating. See Note 7.
GXB_TX[0..7]n	Output	High speed negative differential transmitter channels.	Leave all unused GXB_TXn pins floating. See Note 7.
REFCLK[0..5]p	Input	High speed differential reference clock positive.	These pins should be AC-coupled when used. Connect all unused pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10KΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.

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REFCLK[0..5]n	Input	High speed differential reference clock complement.	These pins should be AC-coupled when used. Connect all unused pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
RREF0	Input	Reference resistor for transceiver.	Each of these pins must be connected to its own individual 2.00-K Ω ± 1 % resistor to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Notes:

(1) References to Cyclone IV devices in this pin connection guideline refer only to Cyclone IV GX devices. Information about Cyclone IV E devices will be included in a future revision of this pin connection guideline.

(2) VCC_CLKIN must be set to 2.5 V if the CLKIN is used as a transceiver refclk. The voltages of VCC_CLKIN for each device density is different. EP4CGX30 and smaller densities have VCC_CLKIN on Banks 3A and 8A that support 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V voltages. EP4CGX50 and larger densities have VCC_CLKIN on Banks 3A and 8A that support 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V voltages, and VCC_CLKIN on Banks 3B and 8B that support 2.5 V.

(3) Capacitance values for the power supply decoupling capacitors should be selected after consideration of the amount of power needed to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis, Altera's "Power Distribution Network (PDN) Design Tool" serves as an excellent decoupling analysis tool. The PDN design tool can be obtained at

Power Distribution Network Design Tool.

(4) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.

(5) Use the Cyclone IV Early Power Estimator to determine the current requirements for VCCINT and other power supplies.

(6) These supplies may share power planes across multiple Cyclone IV devices.

(7) Transceiver signals GXB_RX[0:7] and GXB_TX[0:7] are device specific.

(8) Use seperate power island for VCCA and VCCD_PLL. PLL power supply may originate from another plane on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to(VCCA or VCCD_PLL) and high impedance at 100 MHz.

(9) The number of dedicated global clocks for each device density is different. Please refer to the "Clock Networks and PLLs in Cyclone IV Devices" chapter in the Cyclone IV Device Handbook.

(10) The number of PLLs consisting of GPLLs and MPLLs for each device density is different. EP4CGX15 support 3 PLLs. EP4CGX22 and EP4CGX30 support 4 PLLs. EP4CGX50 and other larger densities support 8 PLLs.

(11) VCCH_GXB, VCCA_GXB, and VCCA may use a switching regulator with a voltage ripple of ± 3 % maximum. VCCD_PLL, and VCCL_GXB may use a switching power supply with a voltage ripple of ± 3 % maximum.

(12) The unused pins must be connected as specified in the Quartus II software settings. The default Quartus II setting for unused pins is 'As inputs tri-stated with weak pull-up resistors', unless for specific pins that Quartus II software connects them to GND automatically. To change the setting, go to 'Assignments', then 'Device'. Click on 'Device & Pin options' dialog box and go to 'Unused Pins' tab. You may choose the desired setting from the 'Reserve all unused pins' drop down list.

(13) You must follow specific requirements when interfacing Cyclone IV device with 2.5 V/3.0 V/3.3 V configuration voltage standards. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Refer to Configuration and JTAG Pin I/O Requirements of the "Configuration and Remote System Upgrades in Cyclone IV Devices" chapter.

(14) The differential TX/RX channels for each device density and package is different. Please refer to the "I/O Features in Cyclone IV Devices" chapter in the Cyclone IV Device Handbook.

(15) For details about the DQ and DQS bus modes support in different device densities, refer to the "External Memory Interfaces in Cyclone IV Devices" chapter in the Cyclone IV Device Handbook.

(16) Altera highly recommends using an independent PCB via for each independent power or ground ball on the package. Sharing power or ground pin vias on the PCB could lead to noise coupling into the device and result in reduced jitter performance.

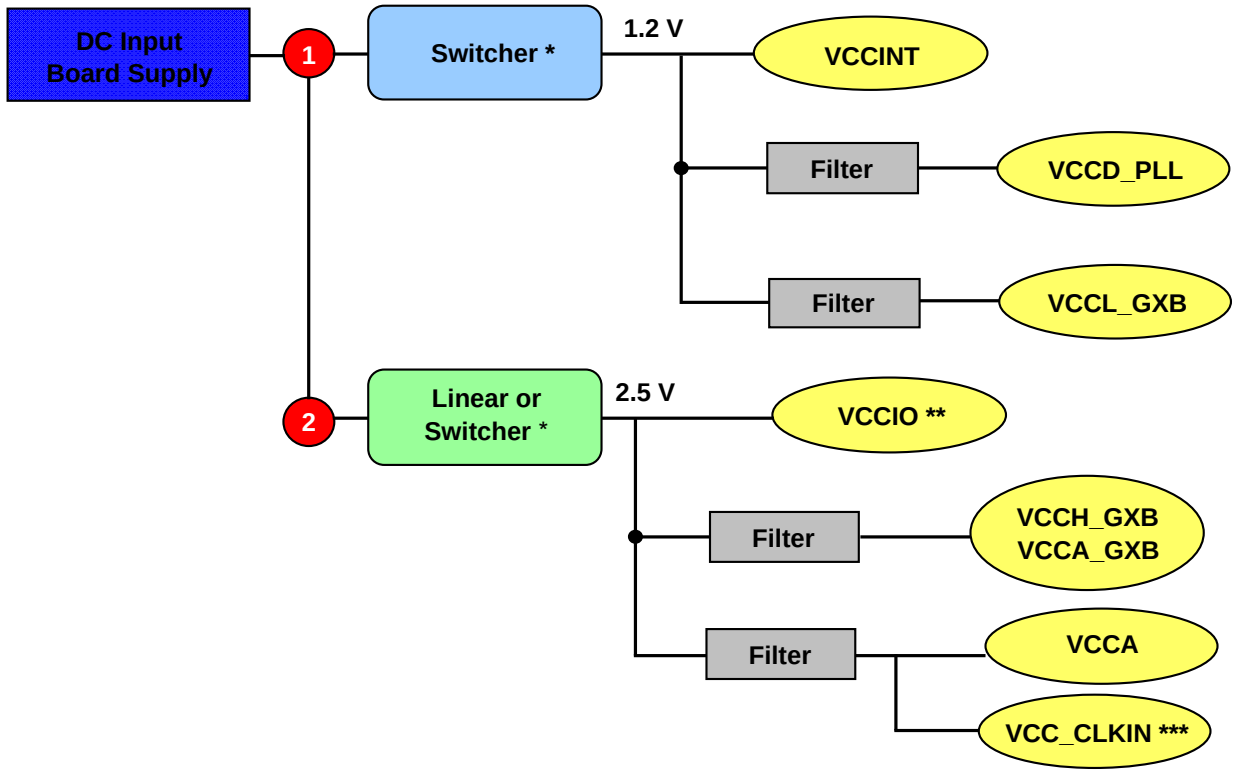
(17) Refer to Example 1 and Figure 1 on the "Power Regs" tab below for the minimum power supply regulator recommendations.

Example 1. Power Supply Sharing Guidelines

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Switching	Notes
VCCINT	1	1.2	± 40 mV	Switcher	Share	May be able to share VCCD_PLL and VCCL_GXB with VCCINT with proper isolation filters. If not sharing the regulator with VCCINT, the VCCD_PLL and VCCL_GXB supplies should not exceed a tolerance of ± 3 %. Depending on the regulator capabilities this supply may be shared with multiple Cyclone IV devices. Use the Early Power Estimation (EPE) tool within Quartus II to assist in determining the power required for your specific design.
VCCD_PLL					Isolate	
VCCL_GXB					Isolate	
VCCIO	2	Varies	± 3 %	Linear or Switcher *	Share if 2.5 V	If VCCIO requires 2.5 V, may be able to share VCCH_GXB, VCCA_GXB, VCCA, and/or VCC_CLKIN with a common 2.5 V supply with proper isolation filters. However, for any other VCCIO voltage you will require a 2.5 V regulator for VCCH_GXB, VCCA_GXB, and VCCA. Use the EPE tool to assist in determining the power required for your specific design.
VCCH_GXB		2.5			Isolate	May be able to share VCCH_GXB and VCCA_GXB with a common 2.5 V supply with a proper isolation filter. Depending on the regulator capabilities, this supply may be shared with multiple Cyclone IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCA_GXB						
VCCA					Isolate	VCC_CLKIN must be set to 2.5 V if the CLKIN is used as a transceiver refclk. If VCC_CLKIN requires 2.5 V, may be able to share VCCA with a common 2.5 V supply with a proper isolation filter. However, for any other VCC_CLKIN voltage you will require a 2.5 V regulator for VCCH_GXB, VCCA_GXB, and VCCA. Depending on the regulator capabilities, this supply may be shared with multiple Cyclone IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCC_CLKIN		Varies			Isolate. Share if 2.5 V	

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 1.

Figure 1. Example Cyclone IV Power Supplies Block Diagram



*** When using a switcher power supply for VCCH_GXB, VCCA_GXB, and/or VCCA, limit these supplies to ± 3 % maximum ripple voltage. When using a switcher power supply for VCCD_PLL, and/or VCCL_GXB, limit these supplies to ± 3 % maximum ripple voltage.**

**** Connect VCCIO pins on banks 4, 5, 6, and 7 to 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V supplies, depending on the I/O standard connected to the specified bank. I/O banks 3, 8, and 9 contain configuration pins. VCCIO pins on banks 3 and 9 support only 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V. If FPP configuration is used, connect VCCIO pins on bank 8 to similar voltage level as banks 3 and 9. If VCCIO requires 2.5 V, can share VCCH_GXB, VCCA_GXB, VCCA, and/or VCC_CLKIN with a common 2.5 V supply with proper isolation filters.**

***** VCC_CLKIN must be set to 2.5 V if the CLKIN is used as a transceiver refclk. The voltages of VCC_CLKIN for each device density is different. EP4CGX30 and smaller densities have VCC_CLKIN on Banks 3A and 8A that support 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V voltages. EP4CGX50 and larger densities have VCC_CLKIN on Banks 3A and 8A that support 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3 V voltages, and VCC_CLKIN on Banks 3B and 8B that support 2.5 V.**

Cyclone® IV Device Family Pin Connection Guidelines
PCG-01008- 1.0

Revision History

Revision	Description of Changes	Date
1.0	Initial release.	10/23/2009