

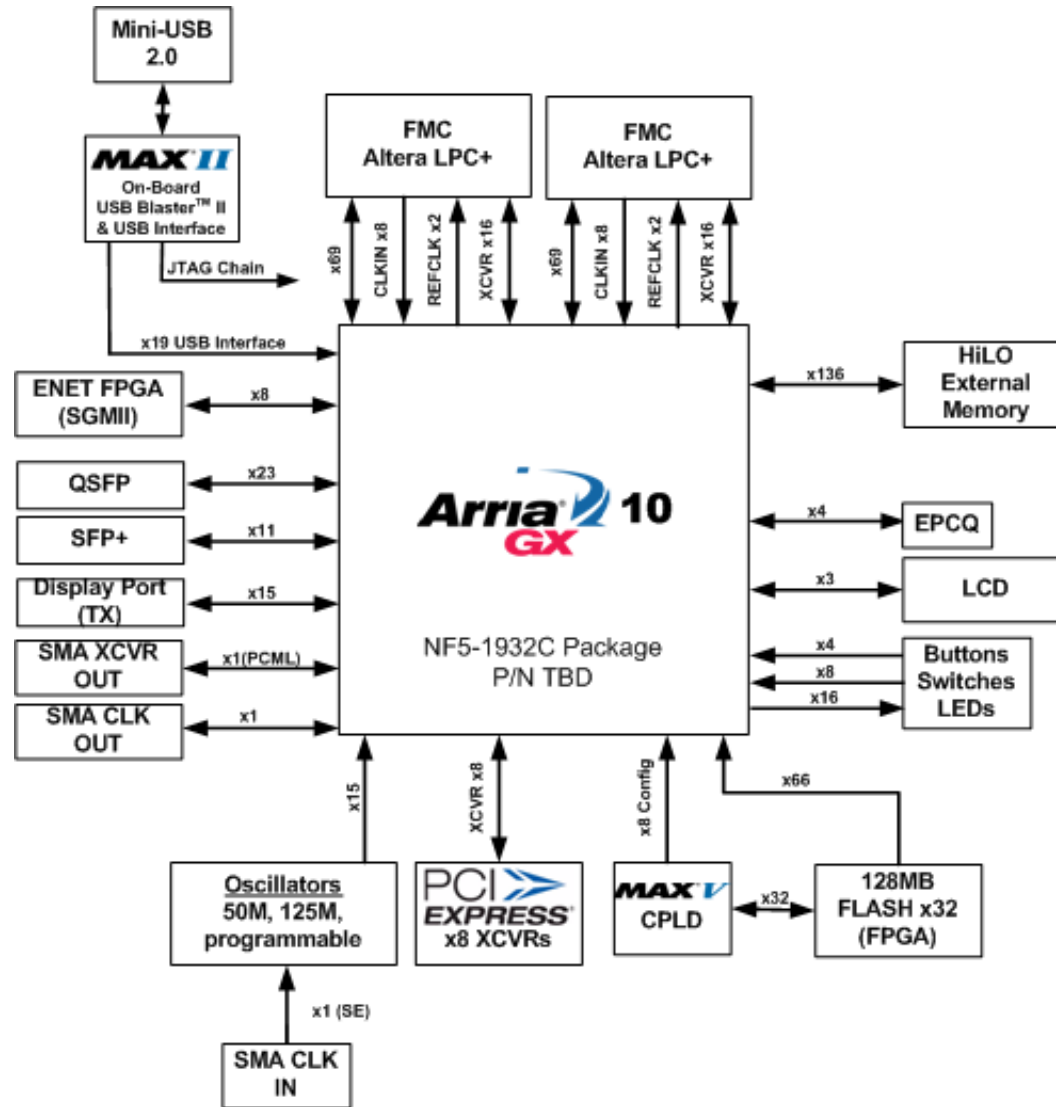
**NOTES:**

- Project Drawing Numbers:
  - Raw PCB 100-0321301-E1
  - Gerber Files 110-0321301-E1
  - PCB Design Files 120-0321301-E1
  - Assembly Drawing 130-0321301-E1
  - Fab Drawing 140-0321301-E1
  - Schematic Drawing 150-0321301-E1
  - PCB Film 160-0321301-E1
  - Bill of Materials 170-0321301-E1
  - Schematic Design Files 180-0321301-E1
  - Functional Specification 210-0321301-E1
  - PCB Layout Guidelines 220-0321301-E1
  - Assembly Rework 320-0321301-E1

2. 1516 Parts, 84 Library Parts, 1524 Nets, 7856 Pins

**Pre-Release Schematic  
DO NOT COPY**

**Arria 10 FPGA Development Kit**

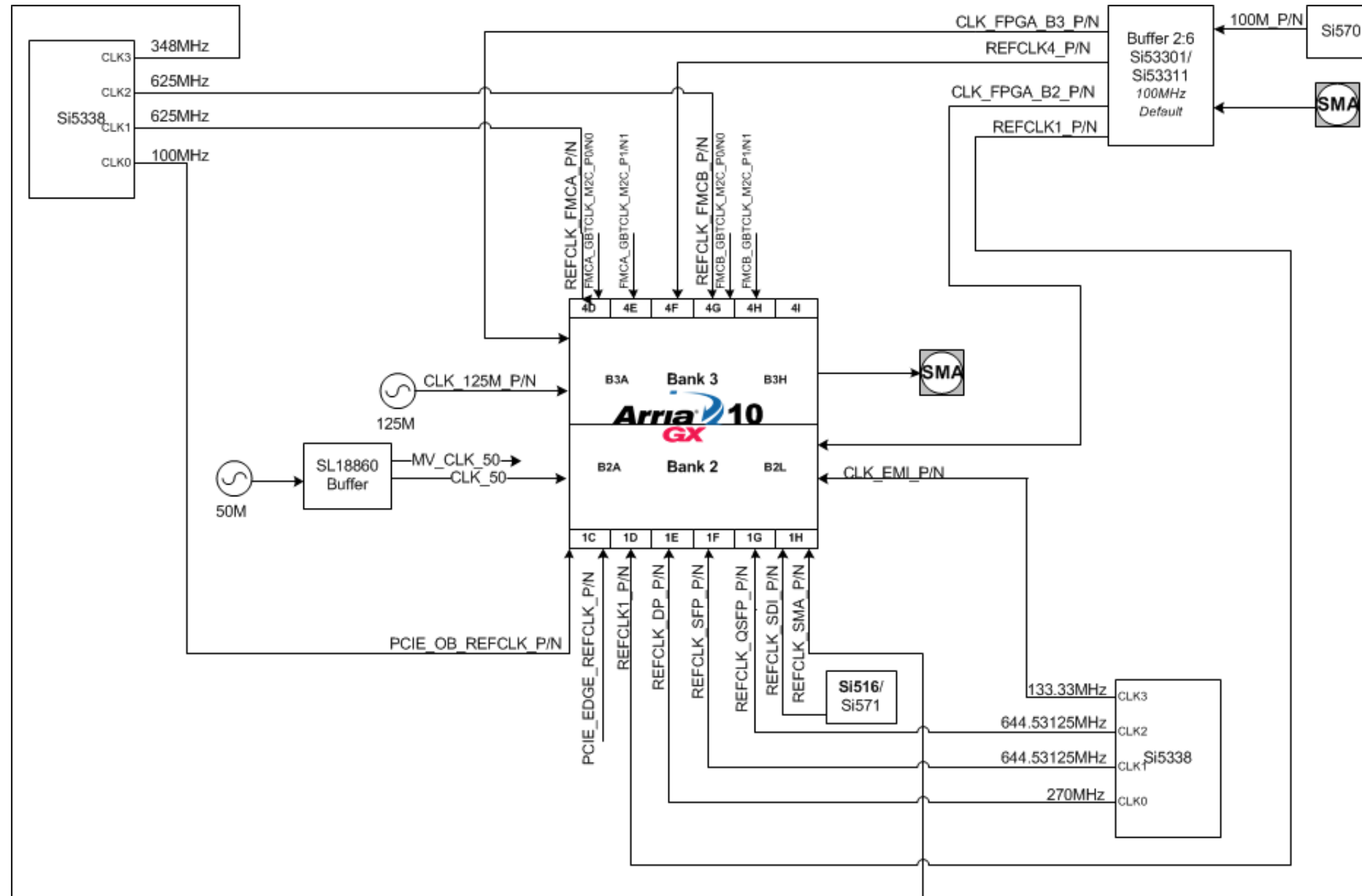


REV	DATE	PAGES	DESCRIPTION
A1	12/26/2013	All	Initial
B1	02/23/2014	All	Rev B bug fixes
C1	07/25/2014	All	Rev C enhancements
D1	11/5/2014	All	Rev D bug fixes
E1	5/5/2015	All	Change from Enpirion 12V power to 5V power
E1.1	5/12/2015	All	Change U85 LDO input from 12V to 5V output from U19 for reduced power dissipation
E1.2	5/15/2015	All	Swap VDD_1.3V_SET and VDD_1.35V_SET. Fix ET4040 SDL and SDA swap

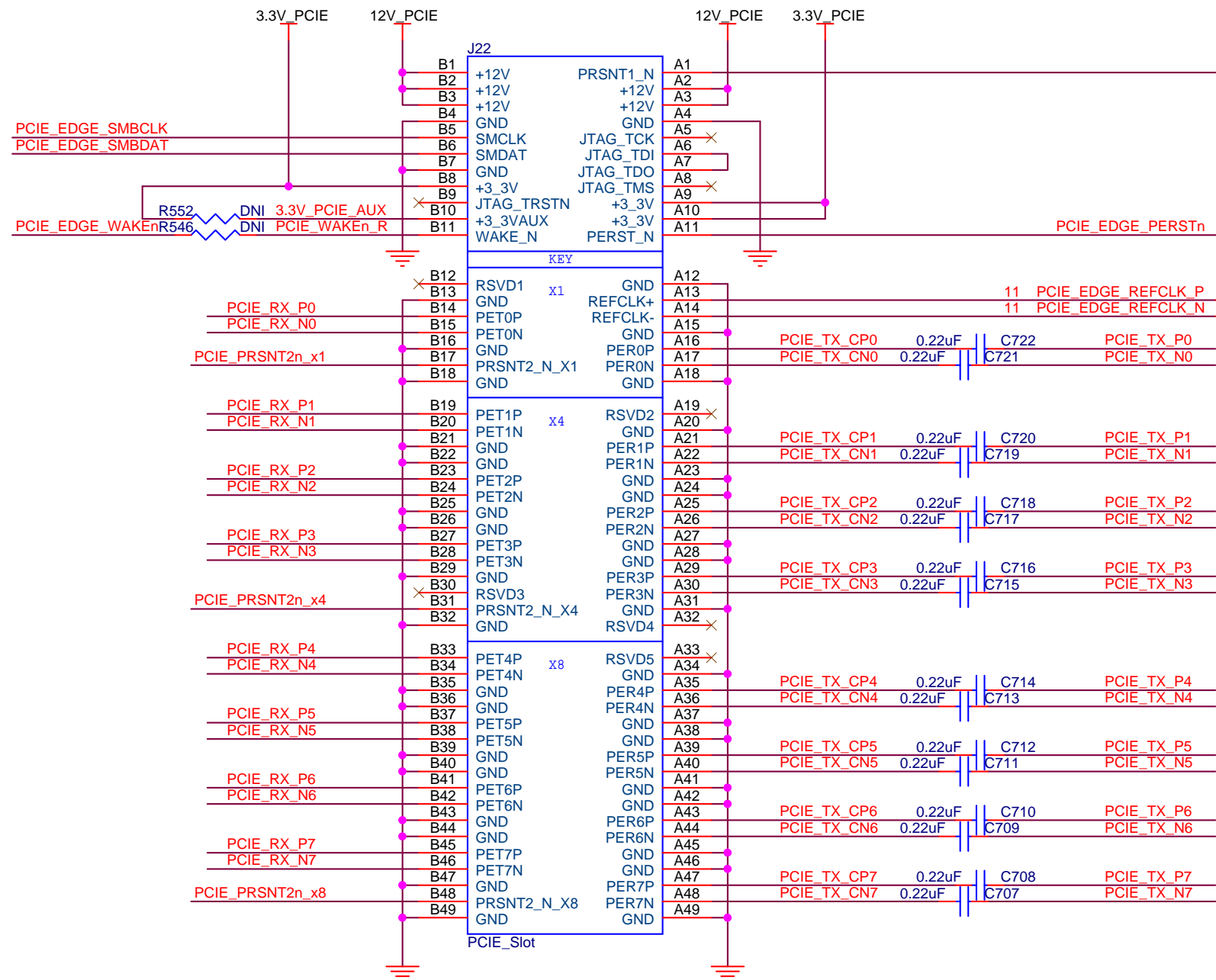
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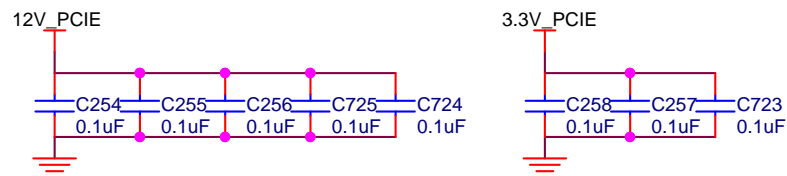
# Clock Diagram



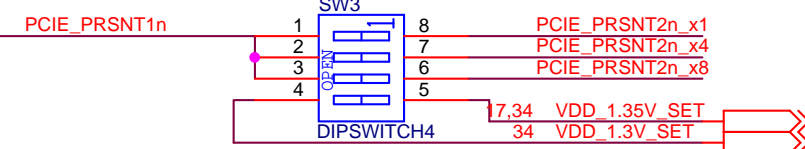
# PCI Express Edge Connector



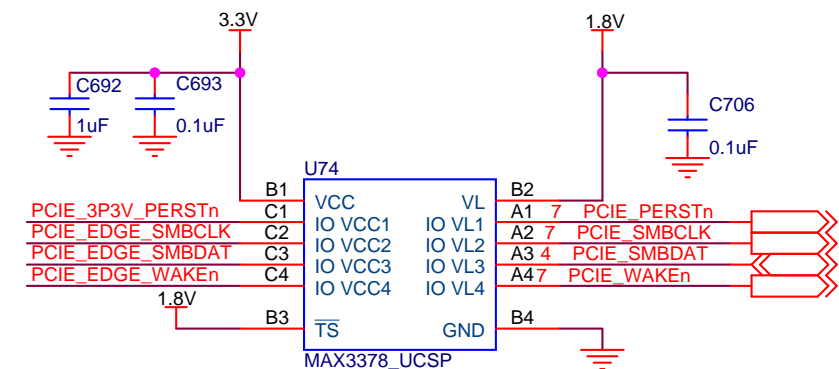
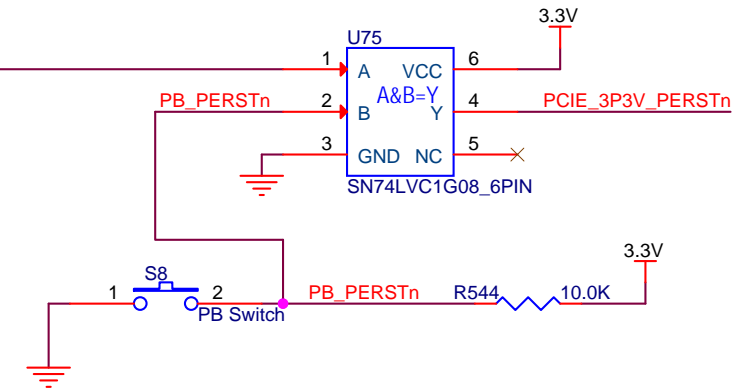
75-ohm to 100-ohm XCVR traces.



## Link Width DIP Switch



QDRIV needs 1.3V VDD. SW3.4 allows changing of 1.35V to 1.3V for QDRIV.



# Arria 10 GX Bank 2

U28C  
ARRIA 10 - BANK 2I-2L

QSFP_LP_MODE	AK34
QSFP_INTERRUPTn	AL34
DP_HOT_PLUG	AM30
CLOCK_SDA	AN30
AL32	AL32
DP_RETURN	AL33
DP_CONFIG2	AK32
DP_CONFIG1	AK31
AM31	AM31
AM32	AM32
AN34	AN34
DP_AUX_CH_P	AM34
DP_AUX_CH_N	AM35
AR32	AR32
AP32	AP32
AT37	AT37
PCIE_SMBDAT	AU37
AP34	AP34
AP33	AP33
AR34	AR34
SFP_TX_DISABLE	AR35
SFP_MOD0_PRSNtn	AT30
SFP_MOD2_SDA	AR31
SFP_RS1	AT34
SFP_TX_FAULT	AT35
SFP_RS0	AN31
SFP_MOD1_SCL	AP31
QSFP_SDA	AU31
SFP_RX_LOS	AU30
QSFP_MOD_PRSn	AU36
QSFP_MOD_SELn	AU35
QSFP_SCL	AV34
QSFP_RSTn	AV35
SDI_MF2_MUTE	AY35
SDI_TX_SD_HDn	AW34
DISP_I2C_SCL	AW33
CLOCK_SCL	AV33
DISP_I2C_SDA	AY34
DISP_SPISS	BA35
SDI_MF0_BYPASS	AW32
SDI_MF1_AUTO_SLEEP	AY32
MEM_DQB0	AC31
MEM_DQB4	AD31
MEM_DQB6	AD33
MEM_DQB5	AD32
MEM_DMB0	AB32
MEM_DQB1	AB31
MEM_DQB3	Y31
MEM_DQB2	W31
MEM_QKB_P0	Y30
MEM_DQB7	AA30
MEM_DQSB_P0	Y32
MEM_DQSB_N0	AA32
MEM_DQB8	AE31
MEM_DQB9	AE32
MEM_DQB10	AE30
MEM_DQB11	AF30
MEM_DQB12	AG33
MEM_DQB14	AH33
MEM_DQB32	AF32
MEM_DQB13	AG32
MEM_DQB18	W32
MEM_DQB17	W33
MEM_DQB21	W35
MEM_DMB2	Y35
MEM_QKB_P1	V33
MEM_DQB23	V34
MEM_DQSB_P2	AA34
MEM_DQSB_N2	AA33
MEM_DQB31	AD34
MEM_DMB3	AC34
MEM_DQB33	AB33
MEM_DQB30	AC33
MEM_DQB28	AD35
MEM_DQB29	AE34
MEM_DQB26	AJ33
MEM_DQB25	AJ34
MEM_DQB27	AH34
MEM_DQB24	AH35
MEM_DQSB_P3	AF33
MEM_DQSB_N3	AF34

IO,LVDS2I_1P,DQ12L	IO,LVDS2I_1N,DQ12L	IO,LVDS2I_2P,DQ12L	IO,LVDS2I_2N,DQ12L	IO,LVDS2I_3P,DQ12L	IO,LVDS2I_3N,DQ12L	IO,LVDS2I_5P,DQ12L	IO,LVDS2I_5N,DQ12L	IO,LVDS2I_6P,DQ12L	IO,LVDS2I_6N,DQ12L	IO,LVDS2I_4P,DQS12L	IO,LVDS2I_4N,DQSN12L	IO,LVDS2I_7P,DQ13L	IO,LVDS2I_7N,DQ13L	IO,LVDS2I_8P,DQ13L	IO,LVDS2I_8N,DQ13L	IO,LVDS2I_9P,DQ13L	IO,LVDS2I_9N,DQ13L	IO,RZQ_2I,LVDS2I_11P,DQ13L	IO,LVDS2I_11N,DQ13L	IO,LVDS2I_14P,DQ14L	IO,LVDS2I_14N,DQ14L	IO,LVDS2I_16P,DQS14L	IO,LVDS2I_16N,DQSN14L	IO,LVDS2I_17P,DQ14L	IO,LVDS2I_17N,DQ14L	IO,LVDS2I_18P,DQ14L	IO,LVDS2I_18N,DQ14L	IO,LVDS2I_19P,DQ15L	IO,LVDS2I_19N,DQ15L	IO,LVDS2I_20P,DQ15L	IO,LVDS2I_20N,DQ15L	IO,LVDS2I_21P,DQ15L	IO,LVDS2I_21N,DQ15L	IO,LVDS2I_23P,DQ15L	IO,LVDS2I_23N,DQ15L	IO,LVDS2I_24P,DQ15L	IO,LVDS2I_24N,DQ15L	IO,LVDS2I_22P,DQS15L	IO,LVDS2I_22N,DQSN15L	IO,LVDS2J_1P,DQ8L	IO,LVDS2J_1N,DQ8L	IO,LVDS2J_2P,DQ8L	IO,LVDS2J_2N,DQ8L	IO,LVDS2J_3P,DQ8L	IO,LVDS2J_3N,DQ8L	IO,LVDS2J_5P,DQ8L	IO,LVDS2J_5N,DQ8L	IO,LVDS2J_6P,DQ8L	IO,LVDS2J_6N,DQ8L	IO,LVDS2J_4P,DQS8L	IO,LVDS2J_4N,DQSN8L	IO,LVDS2J_7P,DQ9L	IO,LVDS2J_7N,DQ9L	IO,LVDS2J_8P,DQ9L	IO,LVDS2J_8N,DQ9L	IO,LVDS2J_9P,DQ9L	IO,LVDS2J_9N,DQ9L	IO,RZQ_2J,LVDS2J_11P,DQ9L	IO,LVDS2J_11N,DQ9L	IO,LVDS2J_14P,DQ10L	IO,LVDS2J_14N,DQ10L	IO,LVDS2J_17P,DQ10L	IO,LVDS2J_17N,DQ10L	IO,LVDS2J_18P,DQ10L	IO,LVDS2J_18N,DQ10L	IO,LVDS2J_16P,DQS10L	IO,LVDS2J_16N,DQSN10L	IO,LVDS2J_19P,DQ11L	IO,LVDS2J_19N,DQ11L	IO,LVDS2J_20P,DQ11L	IO,LVDS2J_20N,DQ11L	IO,LVDS2J_21P,DQ11L	IO,LVDS2J_21N,DQ11L	IO,LVDS2J_23P,DQ11L	IO,LVDS2J_23N,DQ11L	IO,LVDS2J_24P,DQ11L	IO,LVDS2J_24N,DQ11L	IO,LVDS2J_22P,DQS11L	IO,LVDS2J_22N,DQSN11L	IO,LVDS2L_1P,DQ0L	IO,LVDS2L_1N,DQ0L	IO,LVDS2L_2P,DQ0L	IO,LVDS2L_2N,DQ0L	IO,LVDS2L_3P,DQ0L	IO,LVDS2L_3N,DQ0L	IO,LVDS2L_5P,DQ0L	IO,LVDS2L_5N,DQ0L	IO,LVDS2L_6P,DQ0L	IO,LVDS2L_6N,DQ0L	IO,LVDS2L_4P,DQS0L	IO,LVDS2L_4N,DQSN0L	IO,LVDS2L_7P,DQ1L	IO,LVDS2L_7N,DQ1L	IO,LVDS2L_8P,DQ1L	IO,LVDS2L_8N,DQ1L	IO,LVDS2L_9P,DQ1L	IO,LVDS2L_9N,DQ1L	IO,RZQ_2L,LVDS2L_11P,DQ1L	IO,LVDS2L_11N,DQ1L	IO,LVDS2L_14P,DQ2L	IO,LVDS2L_14N,DQ2L	IO,LVDS2L_17P,DQ2L	IO,LVDS2L_17N,DQ2L	IO,LVDS2L_18P,DQ2L	IO,LVDS2L_18N,DQ2L	IO,LVDS2L_16P,DQS2L	IO,LVDS2L_16N,DQSN2L	IO,LVDS2L_19P,DQ3L	IO,LVDS2L_19N,DQ3L	IO,LVDS2L_20P,DQ3L	IO,LVDS2L_20N,DQ3L	IO,LVDS2L_21P,DQ3L	IO,LVDS2L_21N,DQ3L	IO,LVDS2L_23P,DQ3L	IO,LVDS2L_23N,DQ3L	IO,LVDS2L_24P,DQ3L	IO,LVDS2L_24N,DQ3L	IO,LVDS2L_22P,DQS3L	IO,LVDS2L_22N,DQSN3L
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IO,LVDS2K_1P,DQ4L	IO,LVDS2K_1N,DQ4L	IO,LVDS2K_2P,DQ4L	IO,LVDS2K_2N,DQ4L	IO,LVDS2K_3P,DQ4L	IO,LVDS2K_3N,DQ4L	IO,LVDS2K_5P,DQ4L	IO,LVDS2K_5N,DQ4L	IO,LVDS2K_6P,DQ4L	IO,LVDS2K_6N,DQ4L	IO,LVDS2K_4P,DQS4L	IO,LVDS2K_4N,DQSN4L	IO,LVDS2K_7P,DQ5L	IO,LVDS2K_7N,DQ5L	IO,LVDS2K_8P,DQ5L	IO,LVDS2K_8N,DQ5L	IO,LVDS2K_9P,DQ5L	IO,LVDS2K_9N,DQ5L	IO,RZQ_2K,LVDS2K_11P,DQ5L	IO,LVDS2K_11N,DQ5L	IO,LVDS2K_14P,DQ6L	IO,LVDS2K_14N,DQ6L	IO,LVDS2K_17P,DQ6L	IO,LVDS2K_17N,DQ6L	IO,LVDS2K_18P,DQ6L	IO,LVDS2K_18N,DQ6L	IO,LVDS2K_16P,DQS6L	IO,LVDS2K_16N,DQSN6L	IO,LVDS2K_19P,DQ7L	IO,LVDS2K_19N,DQ7L	IO,LVDS2K_20P,DQ7L	IO,LVDS2K_20N,DQ7L	IO,LVDS2K_21P,DQ7L	IO,LVDS2K_21N,DQ7L	IO,LVDS2K_23P,DQ7L	IO,LVDS2K_23N,DQ7L	IO,LVDS2K_24P,DQ7L	IO,LVDS2K_24N,DQ7L	IO,LVDS2K_22P,DQS7L	IO,LVDS2K_22N,DQSN7L	IO,LVDS2L_1P,DQ0L	IO,LVDS2L_1N,DQ0L	IO,LVDS2L_2P,DQ0L	IO,LVDS2L_2N,DQ0L	IO,LVDS2L_3P,DQ0L	IO,LVDS2L_3N,DQ0L	IO,LVDS2L_5P,DQ0L	IO,LVDS2L_5N,DQ0L	IO,LVDS2L_6P,DQ0L	IO,LVDS2L_6N,DQ0L	IO,LVDS2L_4P,DQS0L	IO,LVDS2L_4N,DQSN0L	IO,LVDS2L_7P,DQ1L	IO,LVDS2L_7N,DQ1L	IO,LVDS2L_8P,DQ1L	IO,LVDS2L_8N,DQ1L	IO,LVDS2L_9P,DQ1L	IO,LVDS2L_9N,DQ1L	IO,RZQ_2L,LVDS2L_11P,DQ1L	IO,LVDS2L_11N,DQ1L	IO,LVDS2L_14P,DQ2L	IO,LVDS2L_14N,DQ2L	IO,LVDS2L_17P,DQ2L	IO,LVDS2L_17N,DQ2L	IO,LVDS2L_18P,DQ2L	IO,LVDS2L_18N,DQ2L	IO,LVDS2L_16P,DQS2L	IO,LVDS2L_16N,DQSN2L	IO,LVDS2L_19P,DQ3L	IO,LVDS2L_19N,DQ3L	IO,LVDS2L_20P,DQ3L	IO,LVDS2L_20N,DQ3L	IO,LVDS2L_21P,DQ3L	IO,LVDS2L_21N,DQ3L	IO,LVDS2L_23P,DQ3L	IO,LVDS2L_23N,DQ3L	IO,LVDS2L_24P,DQ3L	IO,LVDS2L_24N,DQ3L	IO,LVDS2L_22P,DQS3L	IO,LVDS2L_22N,DQSN3L
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D32 MEM_DQ_ADDR_CMD3	C33 MEM_DQ_ADDR_CMD4	B32 MEM_DQ_ADDR_CMD2	A32 MEM_DQ_ADDR_CMD0	B33 MEM_DQ_ADDR_CMD5	A33 MEM_DQ_ADDR_CMD1	C35 MEM_DQ_ADDR_CMD7	D34 MEM_DQ_ADDR_CMD6	E35 MEM_ADDR_CMD29	E34 MEM_DQ_ADDR_CMD8	D33 MEM_DQS_ADDR_CMD_P	C34 MEM_DQS_ADDR_CMD_N	G35 MEM_ADDR_CMD17	H35 MEM_ADDR_CMD18	G33 MEM_ADDR_CMD19	F33 MEM_ADDR_CMD16	E32 MEM_ADDR_CMD15	F32 MEM_ADDR_CMD26	J34 24 RZQ B2K	H34 MEM_ADDR_CMD12	J33 MEM_ADDR_CMD8	J32 MEM_ADDR_CMD9	N34 MEM_ADDR_CMD2	M35 MEM_ADDR_CMD3	M32 MEM_ADDR_CMD0	L32 MEM_ADDR_CMD1	L34 MEM_ADDR_CMD4	K34 MEM_ADDR_CMD5	U32 MEM_ADDR_CMD30	T32 MEM_ADDR_CMD31	R30 MEM_CLK_P	R31 MEM_CLK_N	U33 MEM_ADDR_CMD20	T33 MEM_ADDR_CMD21	R34 MEM_ADDR_CMD22	P34 MEM_ADDR_CMD23	T34 MEM_ADDR_CMD28	T35 MEM_ADDR_CMD27	N33 MEM_ADDR_CMD24	P33 MEM_ADDR_CMD25	D26 MEM_DQA6	E26 MEM_DMA0	A28 MEM_DQA1	A27 MEM_DQA2	B28 MEM_DQA0	B27 MEM_DQA3	D27 MEM_DQA4	E27 MEM_DQA5	C28 MEM_QKA_P0	D28 MEM_DQA7	B26 MEM_DQSA_P0	C26 MEM_DQSA_N0	F28 MEM_DQA15	F27 MEM_DQA13	G28 MEM_DQA12	G27 MEM_DMA1	H25 MEM_DQA9	G25 MEM_DQA8	J28 MEM_DQA32	K27 MEM_DQA14	D31 MEM_DQA16	C31 MEM_DQA19	E30 MEM_DQA21	E31 MEM_DQA17	E29 MEM_QKA_P1	D29 MEM_DQA23	C30 MEM_DQSA_P2	C29 MEM_DQSA_N2	F30 MEM_DMA3	F29 MEM_DQA31	K29 MEM_DQA29	J29 MEM_DQA30	K31 MEM_DQA27	K30 MEM_DQA24	G30 MEM_DQA26	G31 MEM_DQA33	H29 MEM_DQA28	H30 MEM_DQA25	L30 MEM_DQSA_P3	L29 MEM_DQSA_N3
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Stratix 5 RZQ  
100-ohm for 50-ohm RT or 25-ohm RS.

## CLOCK INTERFACE

9 CLOCK_SDA
9 CLOCK_SCL

## DISPLAYPORT INTERFACE

18 DP_HOT_PLUG
18 DP_RETURN
18 DP_AUX_CH_P
18 DP_AUX_CH_N
18 DP_CONFIG1
18 DP_CONFIG2
24 DISP_I2C_SCL
24 DISP_I2C_SDA
24 DISP_SPISS

## QSFP INTERFACE

21 QSFP_MOD_SELn
21 QSFP_RSTn
21 QSFP_SCL
21 QSFP_SDA
21 QSFP_INTERRUPTn
21 QSFP_MOD_PRSn
21 QSFP_LP_MODE

## SFP+ INTERFACE

22 SFP_RS0
22 SFP_RS1
22 SFP_TX_DISABLE
22 SFP_RX_LOS
22 SFP_TX_FAULT
22 SFP_MOD0_PRSNtn
22 SFP_MOD1_SCL
22 SFP_MOD2_SDA

## SDI INTERFACE

13,23 SDI_MF2_MUTE
13,23 SDI_MF0_BYPASS
13,23 SDI_MF1_AUTO_SLEEP
13,23 SDI_TX_SD_HDn

## PCIe INTERFACE

3 PCIE_SMBDAT
---------------

## MEMORY INTERFACE

8,17 MEM_ADDR_CMD[31:0]
17 MEM_CLK_P
17 MEM_CLK_N
17 MEM_DQ_ADDR_CMD[8:0]
17 MEM_DQS_ADDR_CMD_P
17 MEM_DQS_ADDR_CMD_N
8,17 MEM_DMA[3:0]
8,17 MEM_DQA[33:0]
8,17 MEM_DQSA_P[3:0]
8,17 MEM_DQSA_N[3:0]
17 MEM_QKA_P[1:0]
8,17 MEM_DMB[3:0]
8,17 MEM_DQB[33:0]
8,17 MEM_DQSB_P[3:0]
8,17 MEM_DQSB_N[3:0]
17 MEM_QKB_P[1:0]

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Title **Arria 10 GX FPGA Development Kit**  
**PRE-RELEASED SCHEMATIC DO NOT COPY**

Size B	Document Number 150-0321301-E1	Rev E1.2
Date: Thursday, May 28, 2015	Sheet 4 of 49	



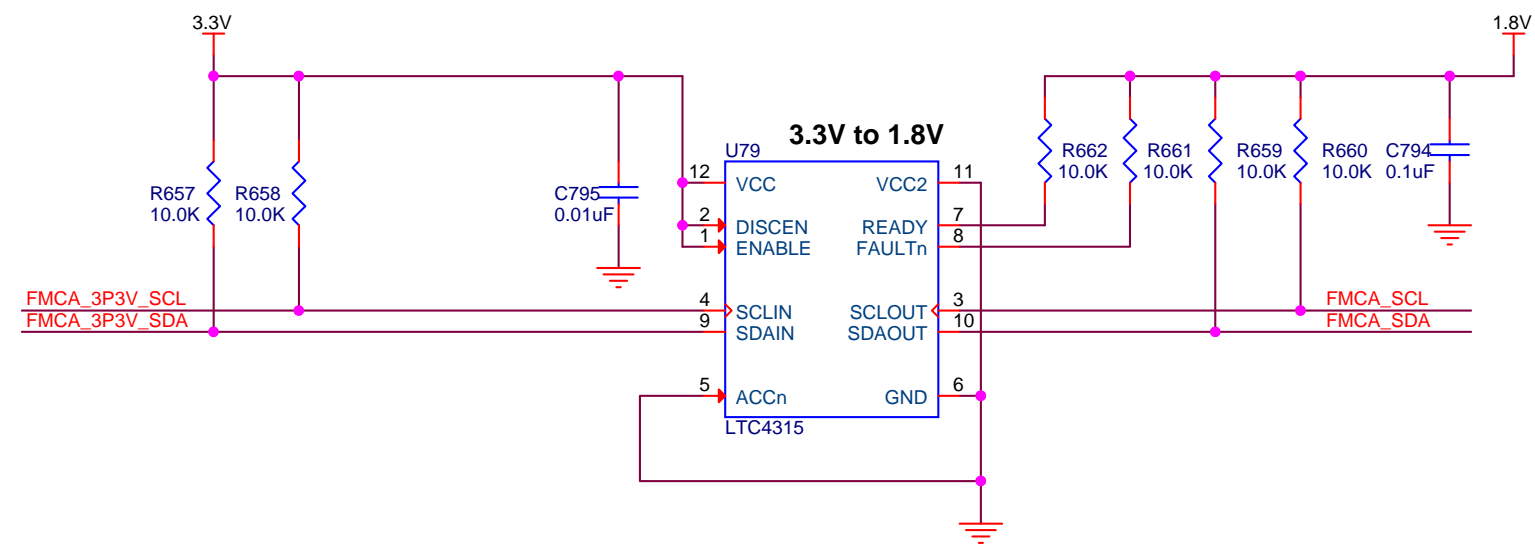
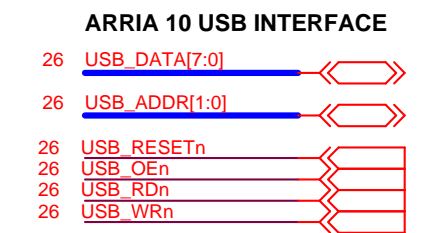
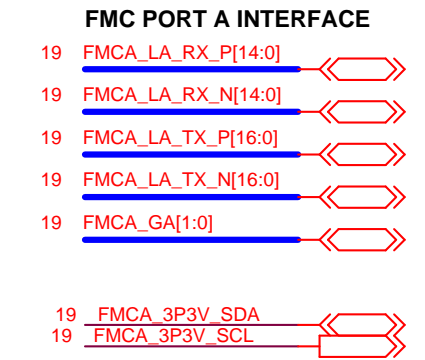
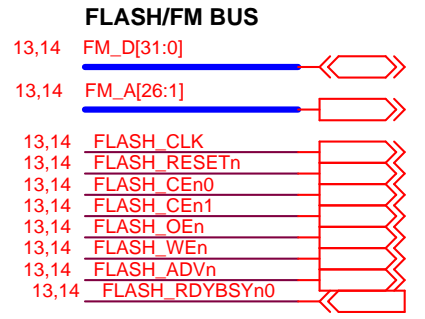
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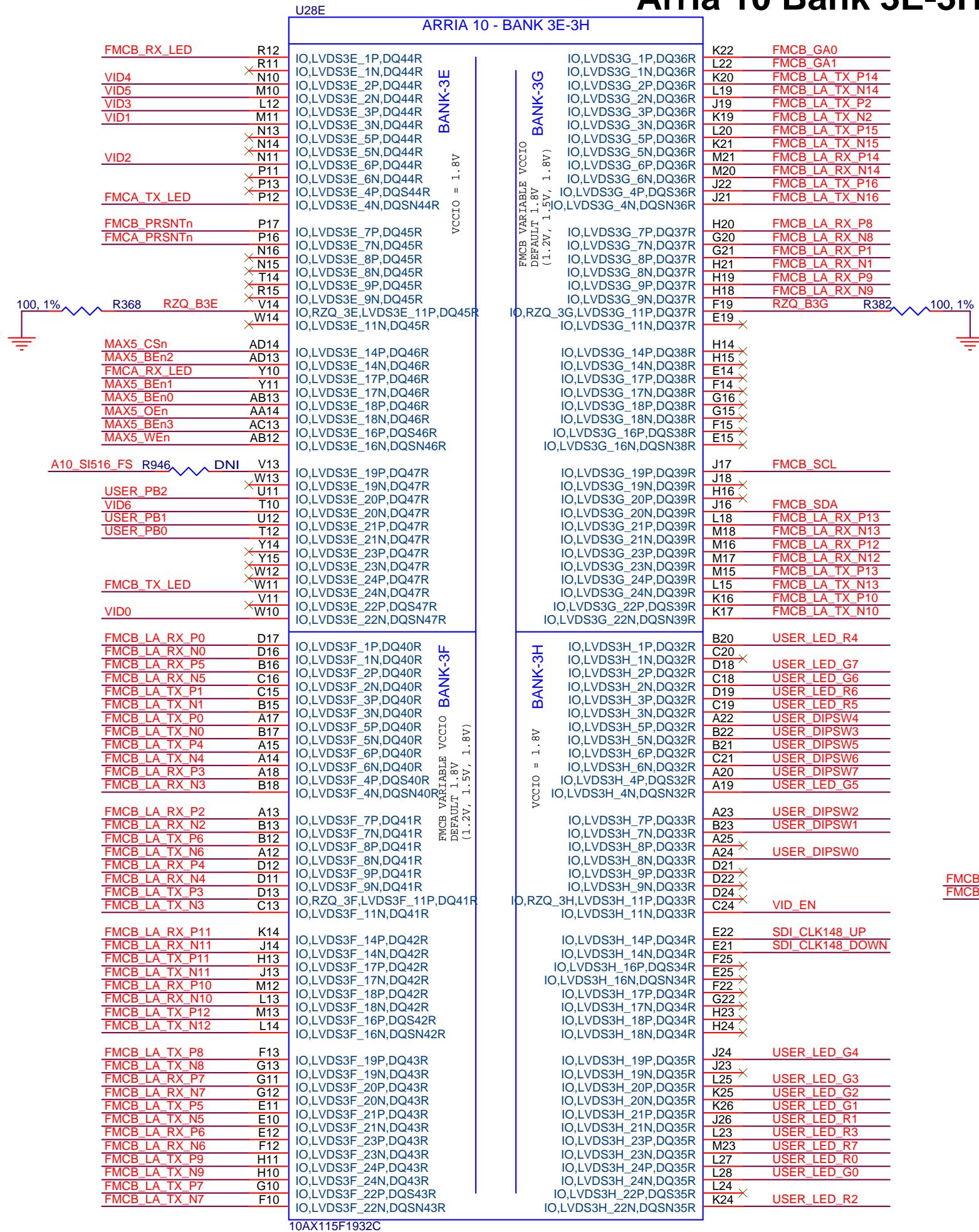
# Arria 10 Bank 3A-3D

U28D		ARRIA 10 - BANK 3A-3D		
FM_D28	AP22	IO,LVDS3A_1P,DQ60R	AU10	FMCA_SCL
FM_D20	AP23	IO,LVDS3A_1N,DQ60R	AV10	FMCA_SDA
FM_D16	AT25	IO,LVDS3A_2P,DQ60R	AU11	FMCA_LA_TX_P9
FM_D27	AR25	IO,LVDS3A_2N,DQ60R	AU12	FMCA_LA_TX_N9
FM_D26	AT23	IO,LVDS3A_3P,DQ60R	AW13	FMCA_LA_TX_P4
FM_D22	AT24	IO,LVDS3A_3N,DQ60R	AV13	FMCA_LA_TX_N4
FM_D12	AP26	IO,LVDS3A_5P,DQ60R	AV11	FMCA_LA_TX_P2
FM_D15	AR26	IO,LVDS3A_5N,DQ60R	AW11	FMCA_LA_TX_N2
FM_D24	AU23	IO,LVDS3A_6P,DQ60R	AY10	FMCA_LA_TX_P10
FM_D30	AU22	IO,LVDS3A_6N,DQ60R	AY11	FMCA_LA_TX_N10
FM_D25	AR24	IO,LVDS3A_4P,DQS60R	AW12	FMCA_LA_RX_P9
FM_D19	AP24	IO,LVDS3A_4N,DQSN60R	AY12	FMCA_LA_RX_N9
FM_D14	BA25	IO,LVDS3A_7P,DQ61R	AR9	FMCA_LA_TX_P7
FM_D4	AY25	IO,LVDS3A_7N,DQ61R	AT9	FMCA_LA_TX_N7
FM_D6	AY24	IO,LVDS3A_8P,DQ61R	AT13	FMCA_LA_RX_P6
FM_D13	BA24	IO,LVDS3A_8N,DQ61R	AU13	FMCA_LA_RX_N6
FM_D2	AU25	IO,LVDS3A_9P,DQ61R	AU8	FMCA_LA_RX_P8
FM_D7	AV25	IO,LVDS3A_9N,DQ61R	AT8	FMCA_LA_RX_N8
FM_D11	AW22	RZQ_3A,LVDS3A_11P,DQ61R	AP14	RZQ_B3C
FLASH_RDYBSYn0	AY22	IO,LVDS3A_11N,DQ61R	AP13	
FLASH_ADVn	BC25	IO,LVDS3A_14P,DQ62R	BD13	
FLASH_CLK	BB25	IO,LVDS3A_14N,DQ62R	BD12	
FLASH_WEn	BD26	IO,LVDS3A_17P,DQ62R	BC14	
FLASH_OEn	BC26	IO,LVDS3A_17N,DQ62R	BD14	
FM_D1	BA22	IO,LVDS3A_18P,DQ62R	BC13	
FLASH_CEn0	BB22	IO,LVDS3A_18N,DQ62R	BB13	
FLASH_CEn1	BB23	IO,LVDS3A_16P,DQS62R	BB12	
FLASH_RESETEn	BA23	IO,LVDS3A_16N,DQSN62R	BB11	
FM_D3	BD21	IO,LVDS3A_19P,DQ63R	BC16	FMCA_GA0
FM_D5	BD22	IO,LVDS3A_19N,DQ63R	BB16	
FM_D29	BC19	IO,LVDS3A_20P,DQ63R	BD17	
FM_D23	BD19	IO,LVDS3A_20N,DQ63R	BD16	FMCA_GA1
FM_D17	BA19	IO,LVDS3A_21P,DQ63R	BA15	FMCA_LA_RX_P12
FM_D18	BA20	IO,LVDS3A_21N,DQ63R	BA14	FMCA_LA_RX_N12
FM_D8	BC21	IO,LVDS3A_23P,DQ63R	BC18	FMCA_LA_TX_P15
FM_D9	BB21	IO,LVDS3A_23N,DQ63R	BD18	FMCA_LA_TX_N15
FM_D10	BC20	IO,LVDS3A_24P,DQ63R	BB17	FMCA_LA_RX_P13
FM_D0	BB20	IO,LVDS3A_24N,DQ63R	BB18	FMCA_LA_RX_N13
FM_D31	BA17	IO,LVDS3A_22P,DQS63R	BB15	FMCA_LA_TX_P12
FM_D21	BA18	IO,LVDS3A_22N,DQSN63R	BC15	FMCA_LA_TX_N12
FMCA_LA_RX_P4	AR16	IO,LVDS3B_1P,DQ56R	AJ11	USB_DATA0
FMCA_LA_RX_N4	AP16	IO,LVDS3B_1N,DQ56R	AK12	USB_DATA1
FMCA_LA_TX_P11	AU18	IO,LVDS3B_2P,DQ56R	AL12	FM_A3
FMCA_LA_TX_N11	AT18	IO,LVDS3B_2N,DQ56R	AL13	FM_A11
FMCA_LA_TX_P3	AT17	IO,LVDS3B_3P,DQ56R	AK14	FM_A25
FMCA_LA_TX_N3	AU17	IO,LVDS3B_3N,DQ56R	AJ14	FM_A20
FMCA_LA_TX_P5	AT14	IO,LVDS3B_5P,DQ56R	AH10	FM_A15
FMCA_LA_TX_N5	AR14	IO,LVDS3B_5N,DQ56R	AH11	FM_A12
FMCA_LA_RX_P3	AR15	IO,LVDS3B_6P,DQ56R	AJ12	FM_A19
FMCA_LA_RX_N3	AT15	IO,LVDS3B_6N,DQ56R	AJ13	FM_A23
FMCA_LA_TX_P6	AR17	IO,LVDS3B_4P,DQS56R	AH13	FM_A21
FMCA_LA_TX_N6	AP17	IO,LVDS3B_4N,DQSN56R	AH14	FM_A18
FMCA_LA_RX_P14	AY17	IO,LVDS3B_7P,DQ57R	AF12	FM_A24
FMCA_LA_RX_N14	AW17	IO,LVDS3B_7N,DQ57R	AE12	FM_A6
FMCA_LA_RX_P1	AV14	IO,LVDS3B_8P,DQ57R	AG12	FM_A22
FMCA_LA_RX_N1	AW14	IO,LVDS3B_8N,DQ57R	AG11	FM_A14
FMCA_LA_TX_P14	AY16	IO,LVDS3B_9P,DQ57R	AF14	FM_A16
FMCA_LA_TX_N14	AW16	IO,LVDS3B_9N,DQ57R	AF15	FM_A17
FMCA_LA_RX_P10	AY15	IO,RZQ_3B,LVDS3B_11P,DQ57R	AE14	USB_RESETEn
FMCA_LA_RX_N10	AY14	IO,LVDS3B_11N,DQ57R	AE15	USB_WRn
FMCA_LA_RX_P5	AW18	IO,LVDS3B_14P,DQ58R	AL15	USB_OEn
FMCA_LA_RX_N5	AV18	IO,LVDS3B_14N,DQ58R	AK15	USB_RDn
FMCA_LA_TX_P8	AV19	IO,LVDS3B_17P,DQ58R	AL19	USB_DATA6
FMCA_LA_TX_N8	AW19	IO,LVDS3B_17N,DQ58R	AL20	USB_DATA7
FMCA_LA_TX_P16	AV20	IO,LVDS3B_18P,DQ58R	AM17	USB_DATA4
FMCA_LA_TX_N16	AU20	IO,LVDS3B_18N,DQ58R	AL17	USB_DATA5
FMCA_LA_RX_P7	AU21	IO,LVDS3B_16P,DQS58R	AM15	USB_ADDR0
FMCA_LA_RX_N7	AV21	IO,LVDS3B_16N,DQSN58R	AL14	USB_ADDR1
FMCA_LA_TX_P13	AT19	IO,LVDS3B_19P,DQ59R	AN11	USB_DATA2
FMCA_LA_TX_N13	AT20	IO,LVDS3B_19N,DQ59R	AN10	USB_DATA3
FMCA_LA_RX_P11	AP21	IO,LVDS3B_20P,DQ59R	AL10	FM_A8
FMCA_LA_RX_N11	AR21	IO,LVDS3B_20N,DQ59R	AK11	FM_A26
FMCA_LA_RX_P2	AP18	IO,LVDS3B_21P,DQ59R	AN13	FM_A4
FMCA_LA_RX_N2	AN19	IO,LVDS3B_21N,DQ59R	AM13	FM_A5
FMCA_LA_RX_P0	AR20	IO,LVDS3B_23P,DQ59R	AP11	FM_A10
FMCA_LA_RX_N0	AR19	IO,LVDS3B_23N,DQ59R	AR10	FM_A9
FMCA_LA_TX_P0	AR22	IO,LVDS3B_24P,DQ59R	AM12	FM_A2
FMCA_LA_TX_N0	AT22	IO,LVDS3B_24N,DQ59R	AM11	FM_A1
FMCA_LA_TX_P1	AN20	IO,LVDS3B_22P,DQS59R	AN15	FM_A7
FMCA_LA_TX_N1	AP19	IO,LVDS3B_22N,DQSN59R	AN14	FM_A13

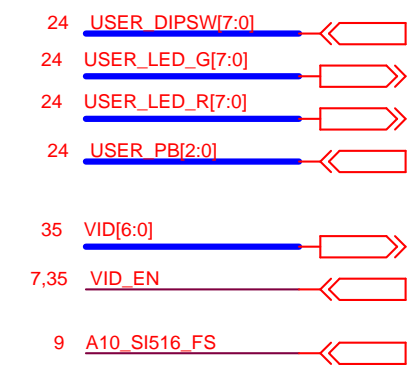
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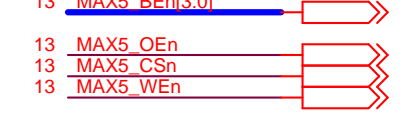
# Arria 10 Bank 3E-3H



## USER IO INTERFACE



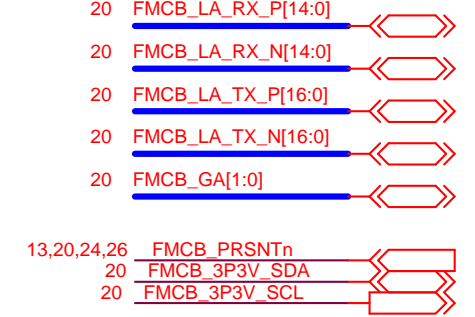
## MAX V INTERFACE



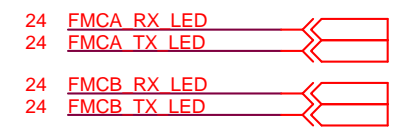
## FMC PORT A INTERFACE



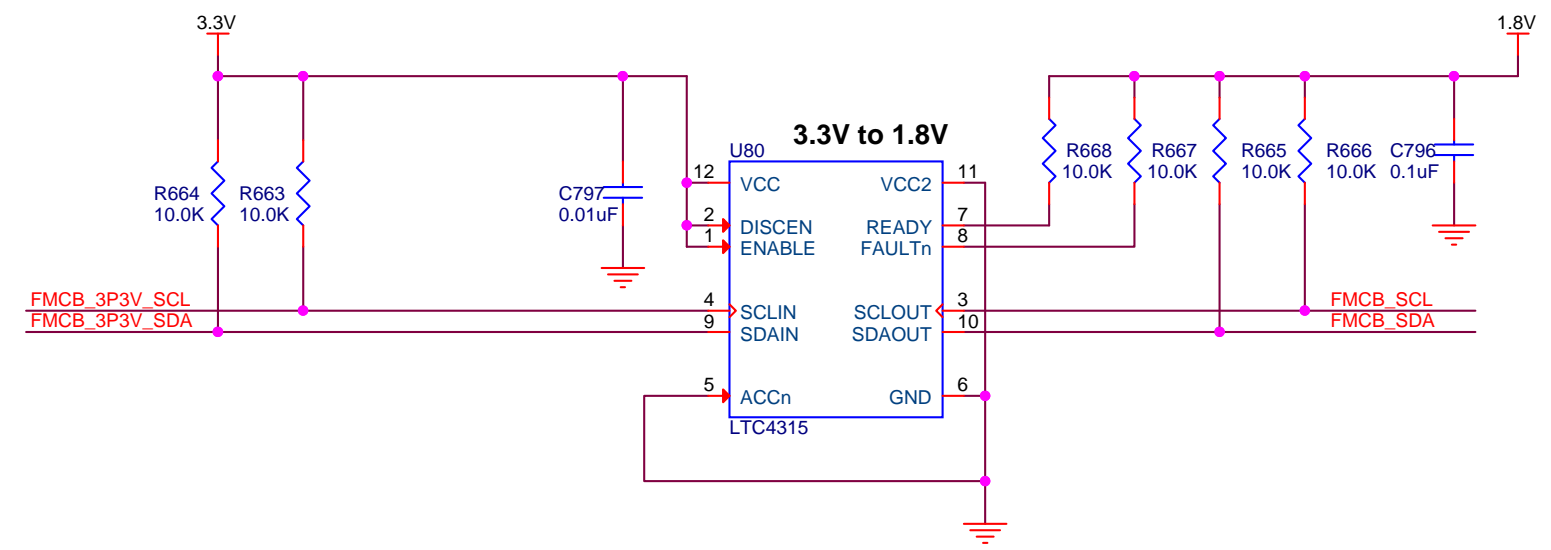
## FMC PORT B INTERFACE



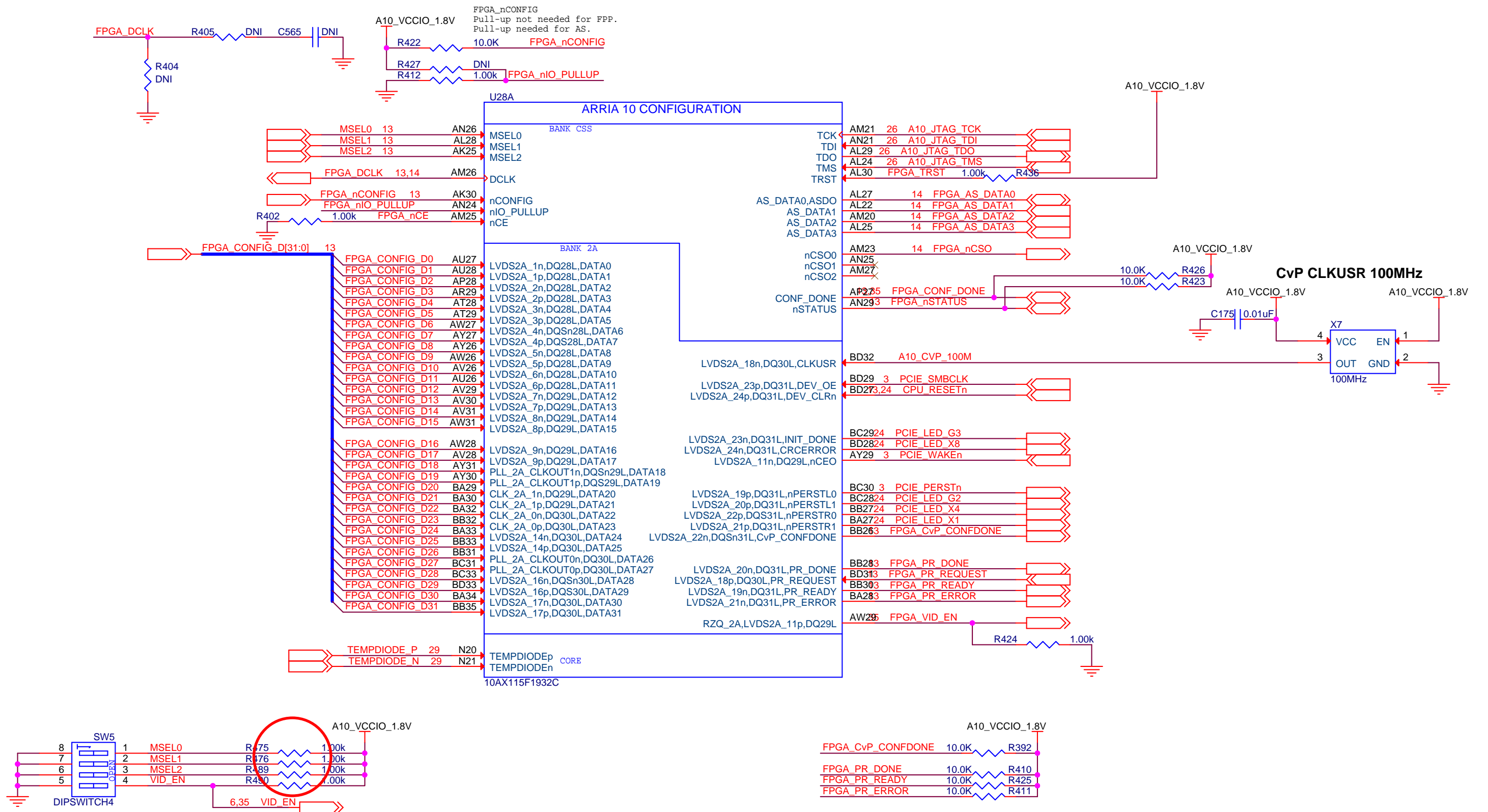
## USER I/O INTERFACE



## ARRIA 10 CLOCKS

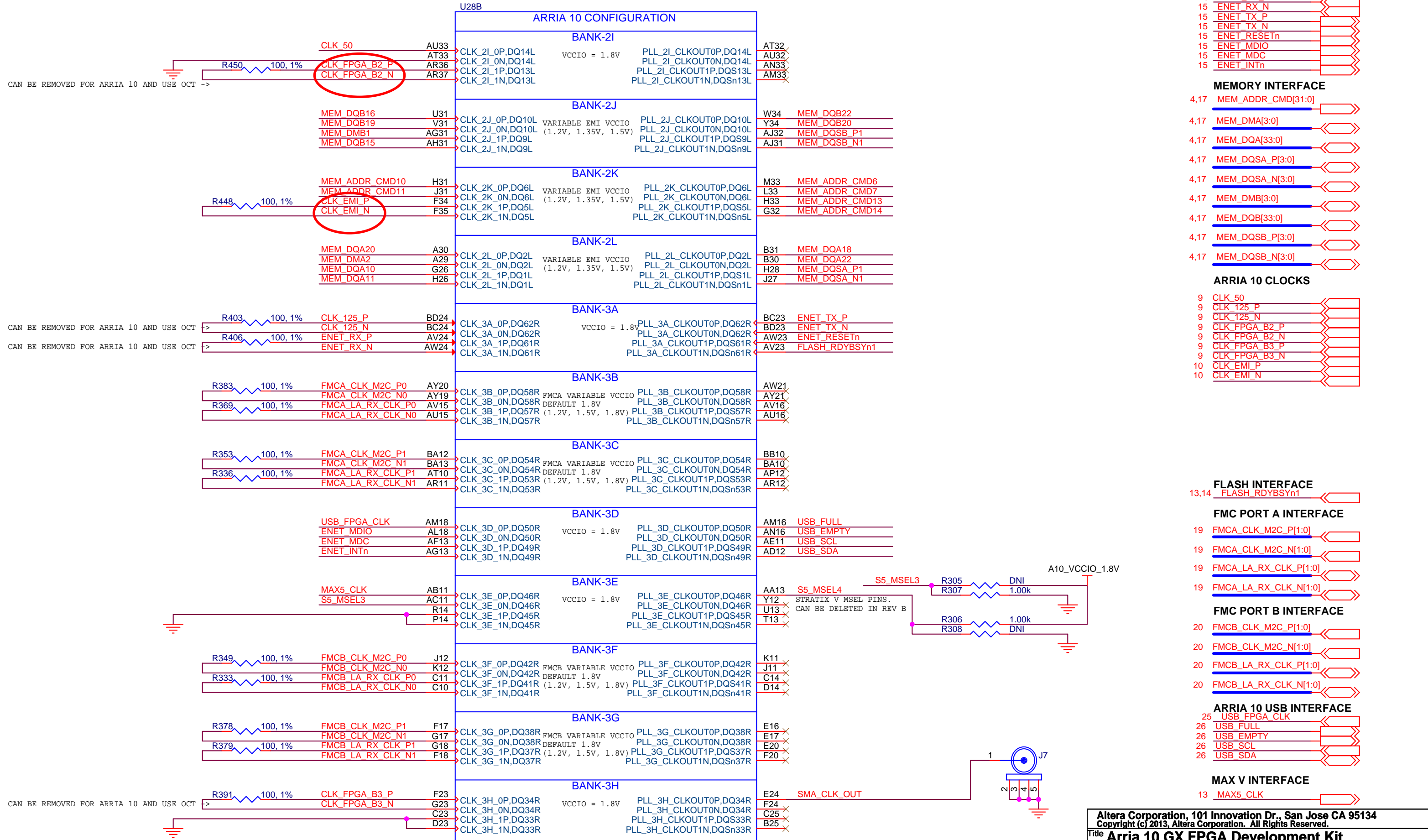


# Arria 10 Configuration





# Arria 10 Clocks



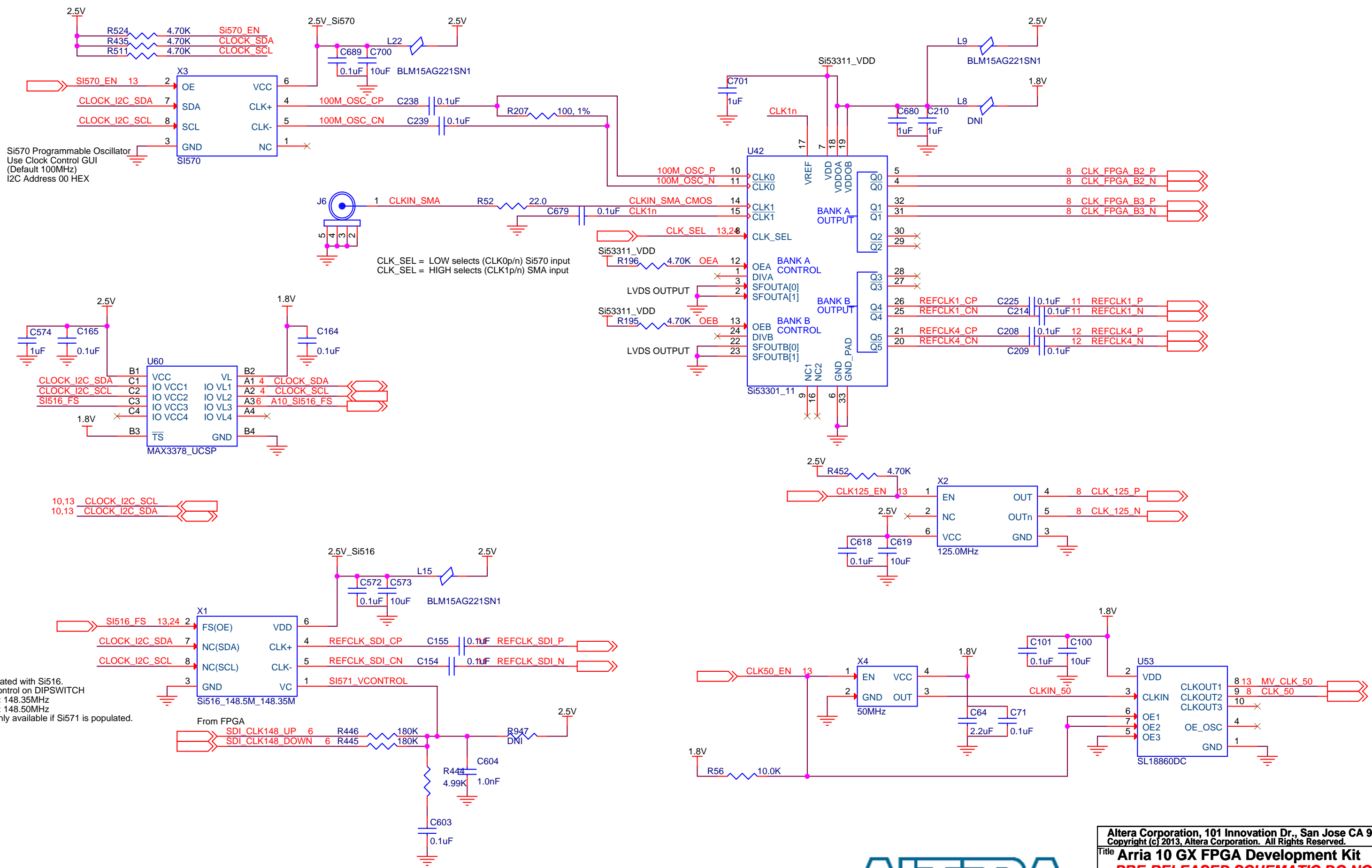
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Size B	Document Number 150-0321301-E1 (6XX-44362R)	Rev E1.2
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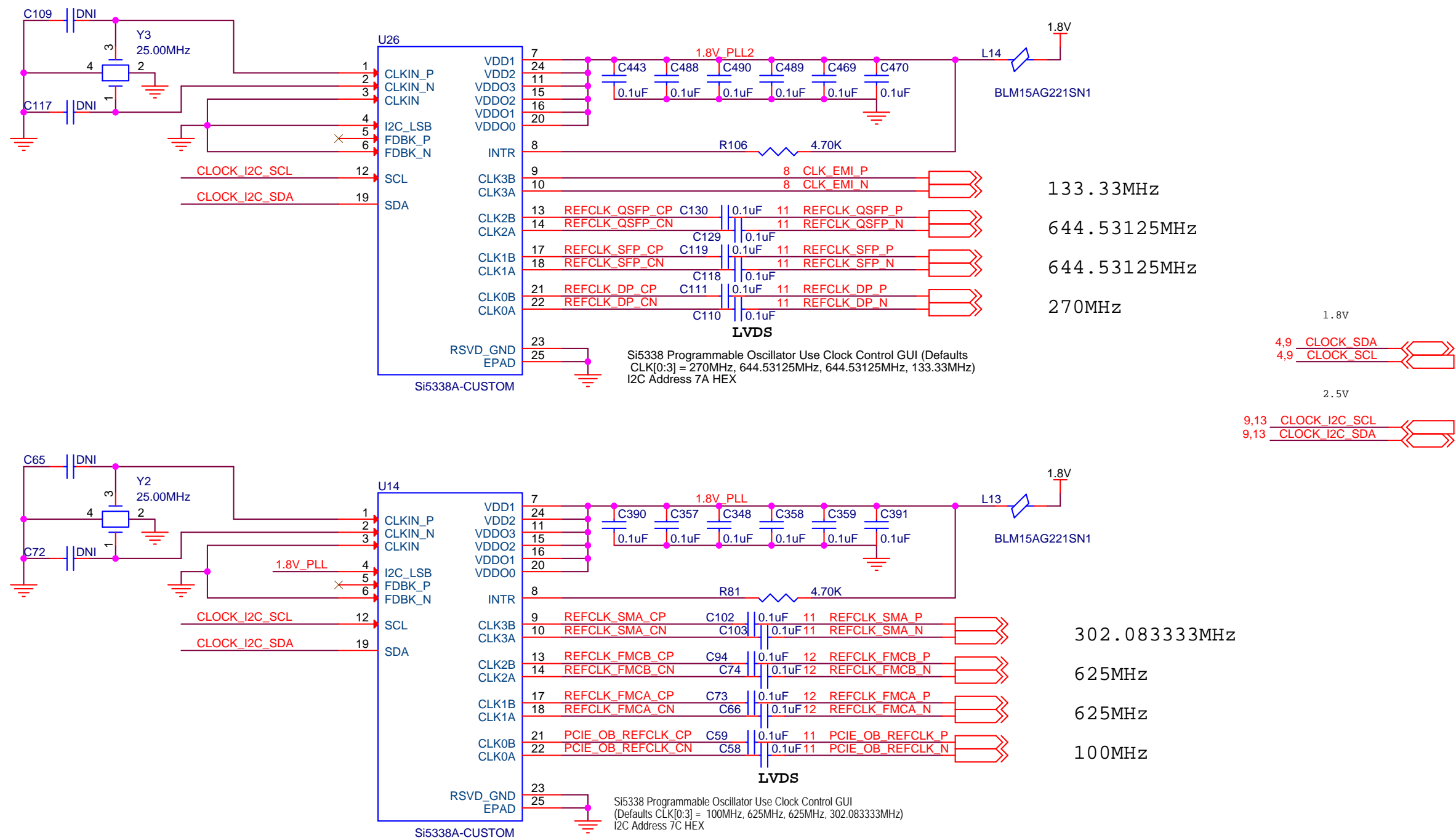


# Clocks

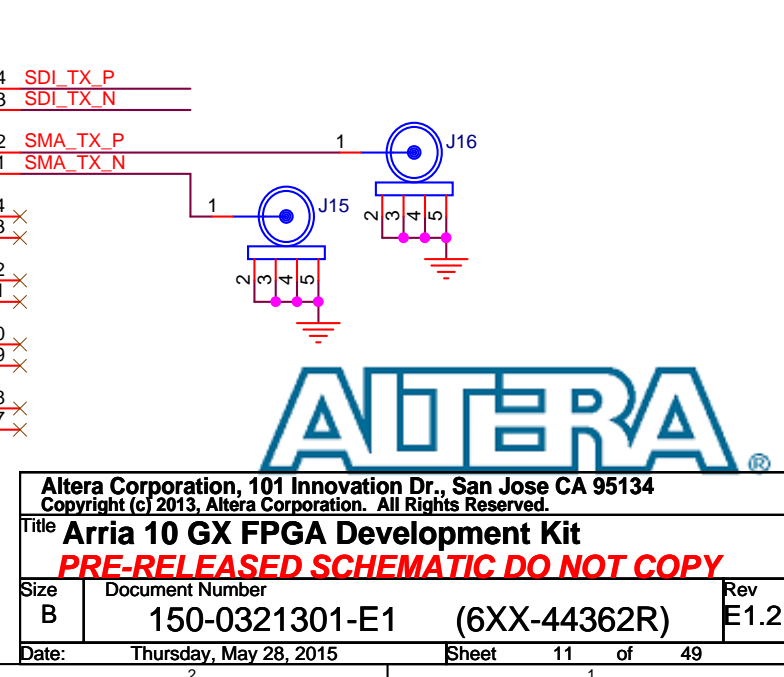
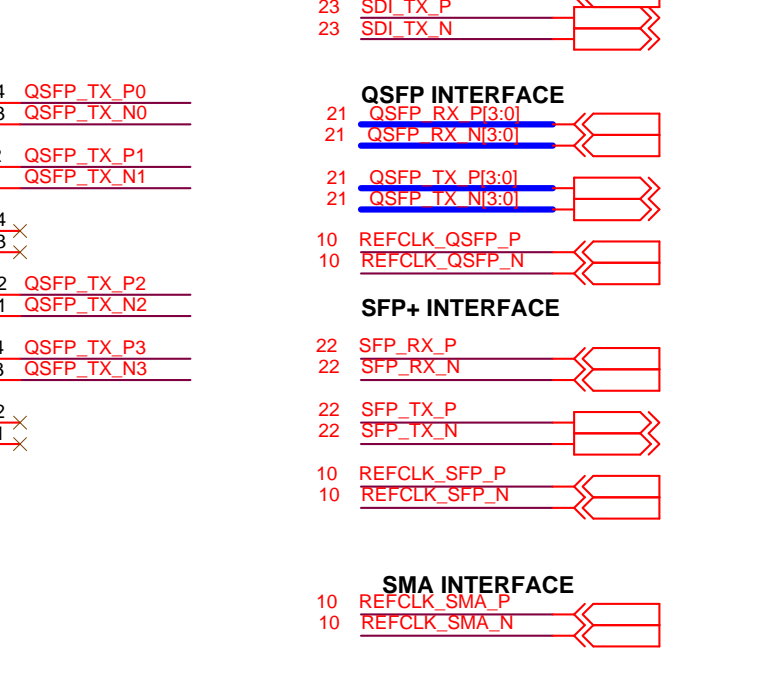
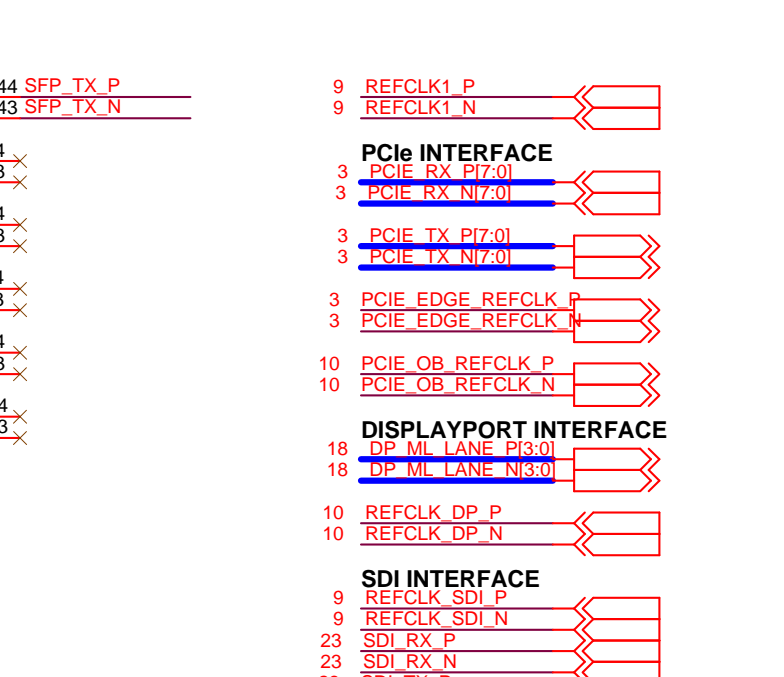
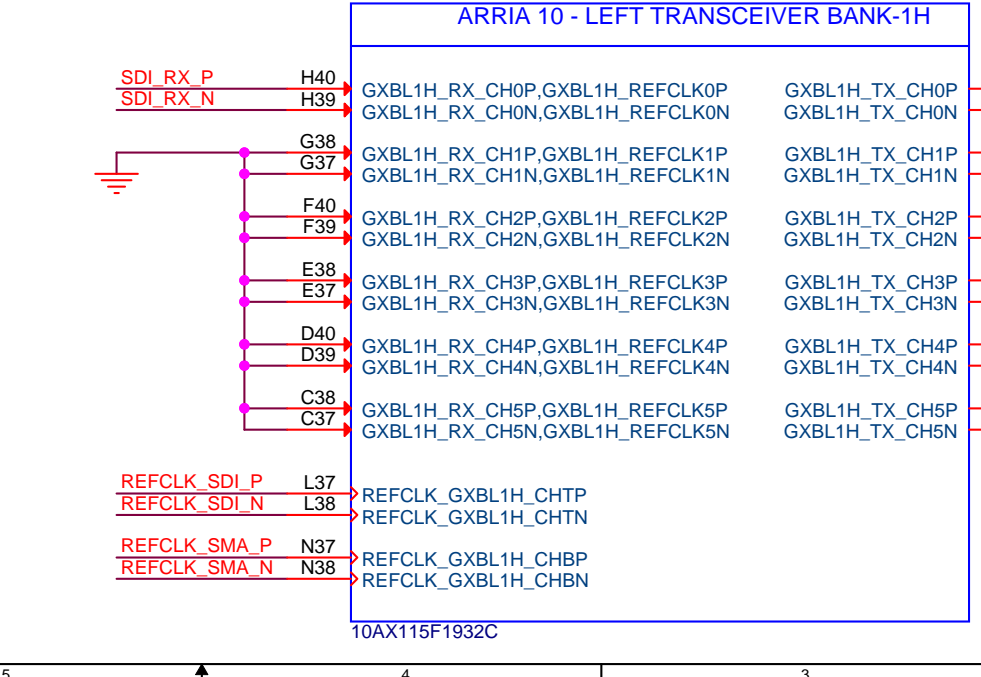
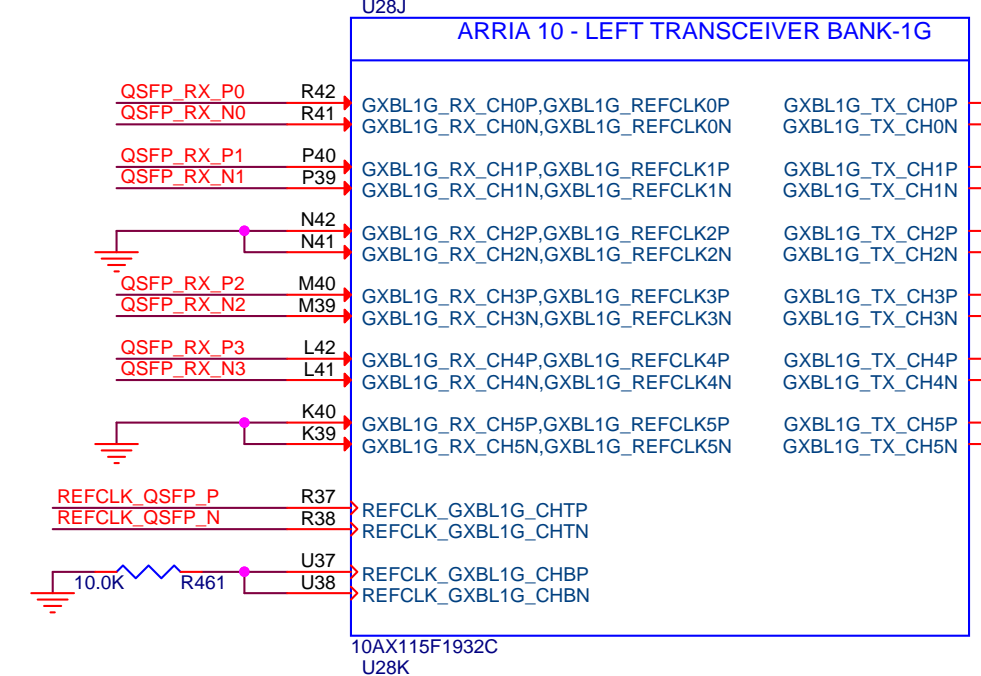
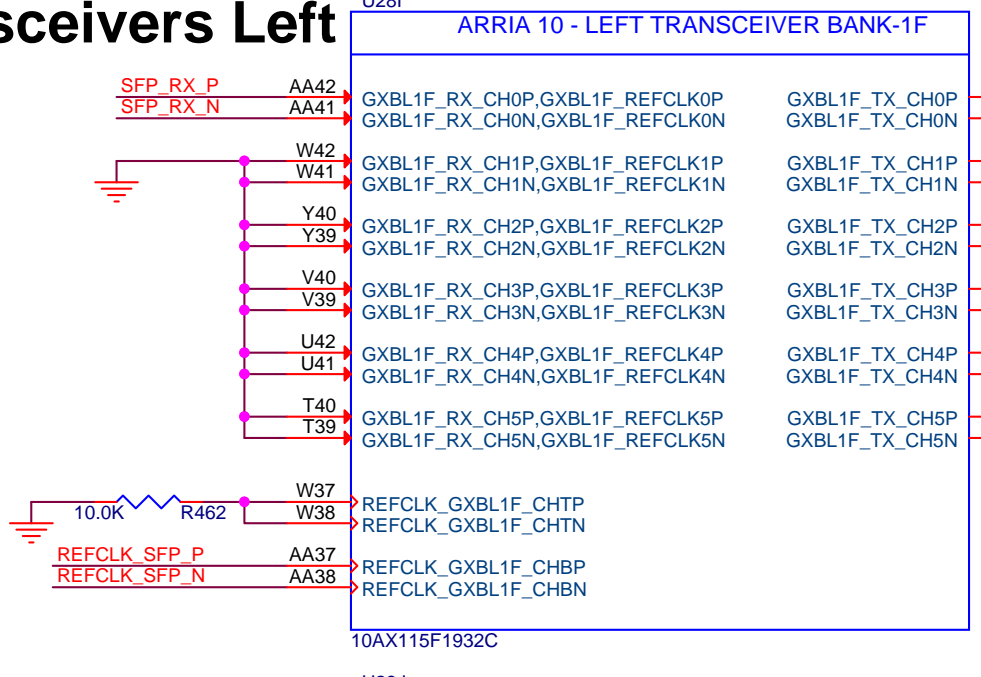
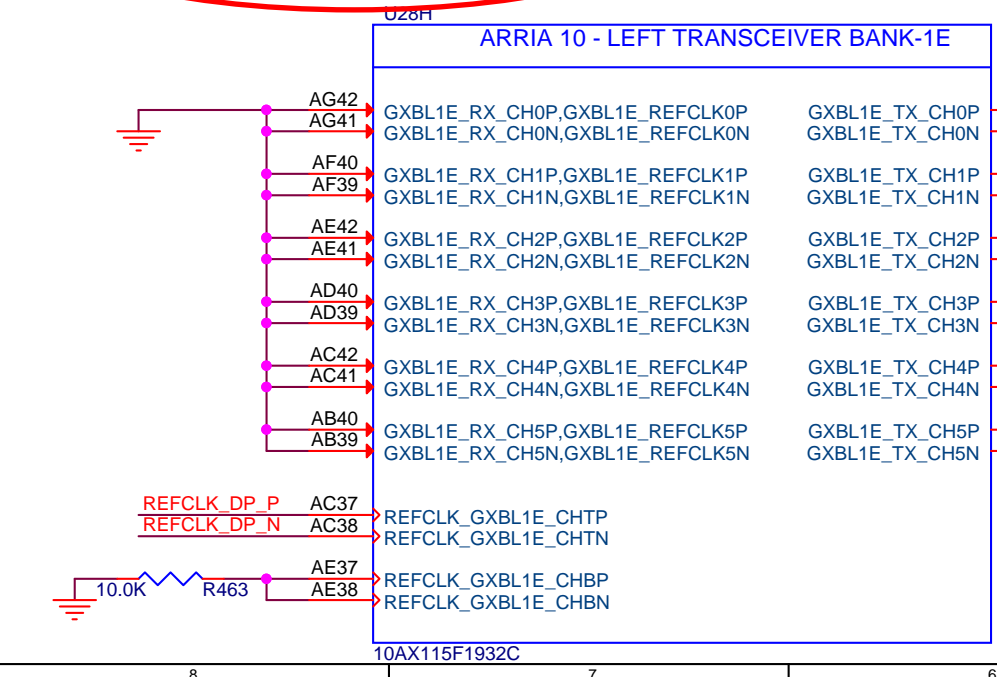
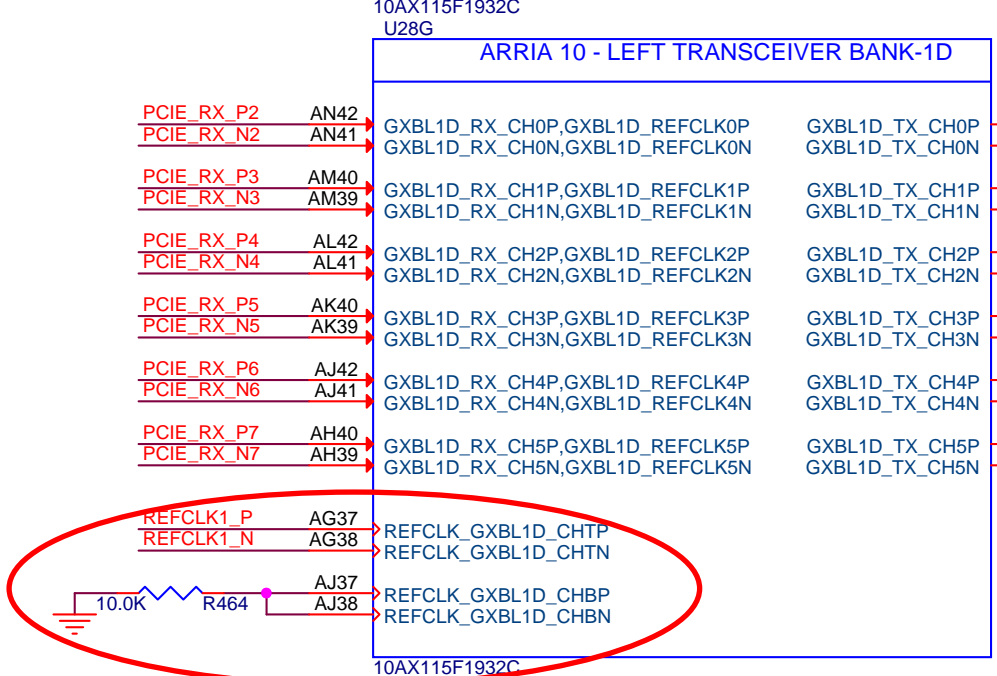
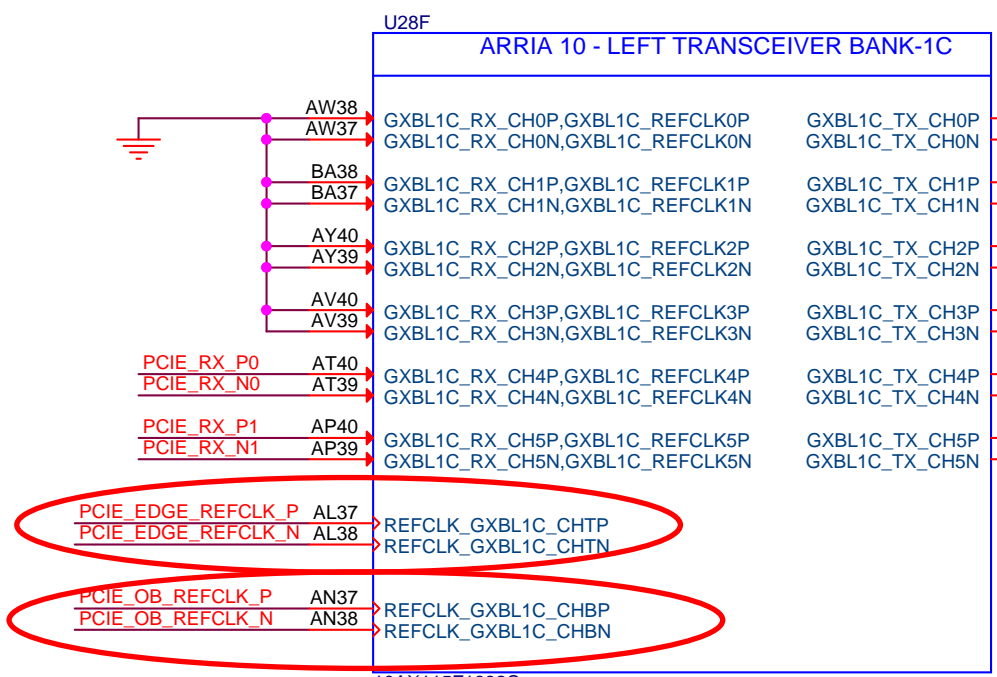


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Title <b>Arria 10 GX FPGA Development Kit</b>		
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Size B	Document Number 150-0321301-E1 (6XX-44362R)	Rev E1.2
Date: Thursday, May 28, 2015	Sheet 9	of 49

# PLL (2)

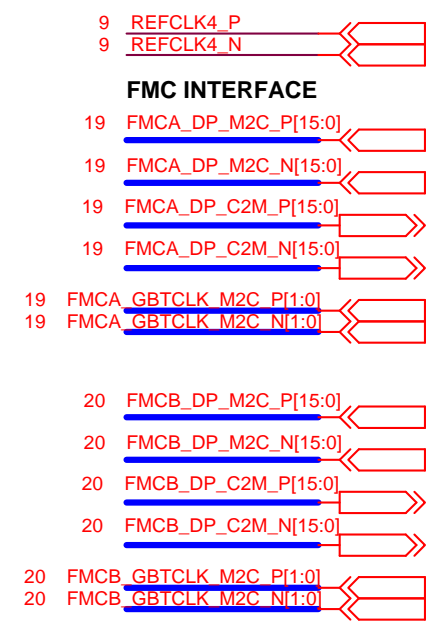
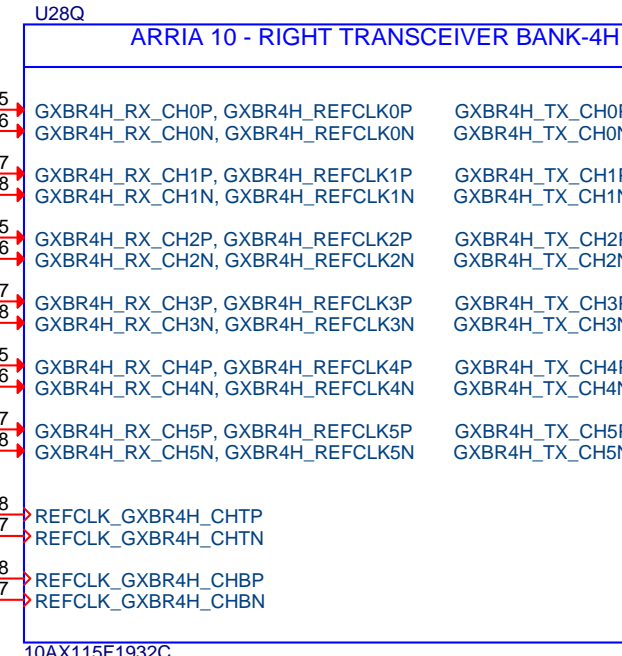
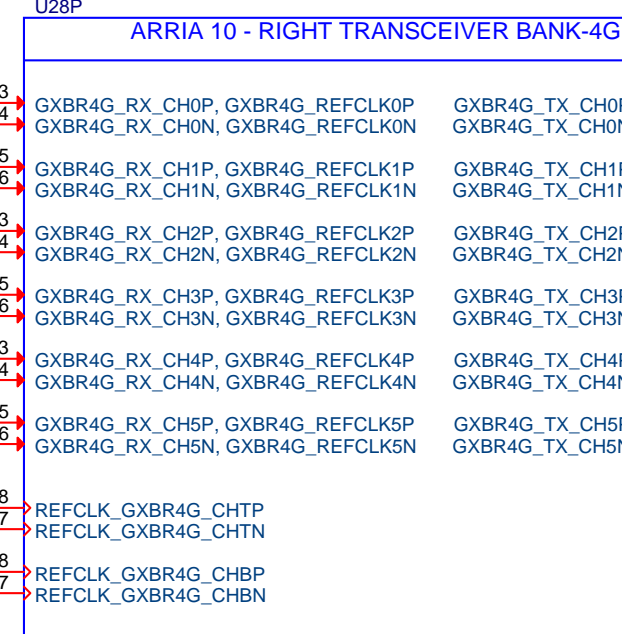
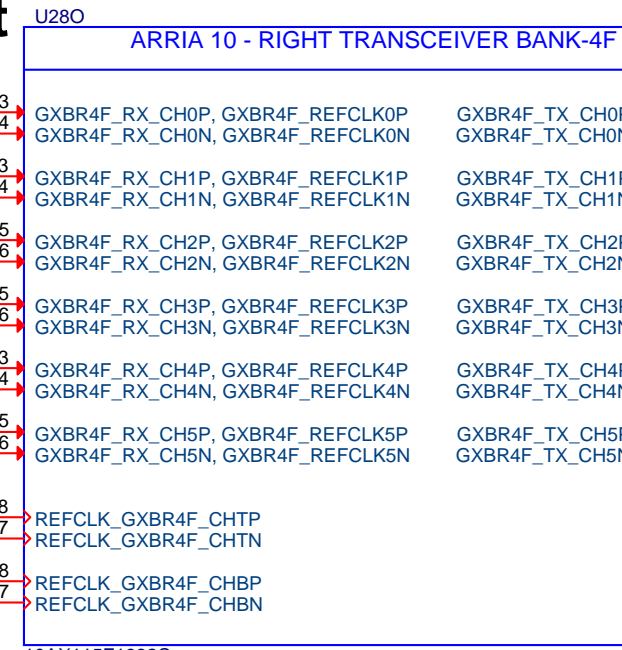
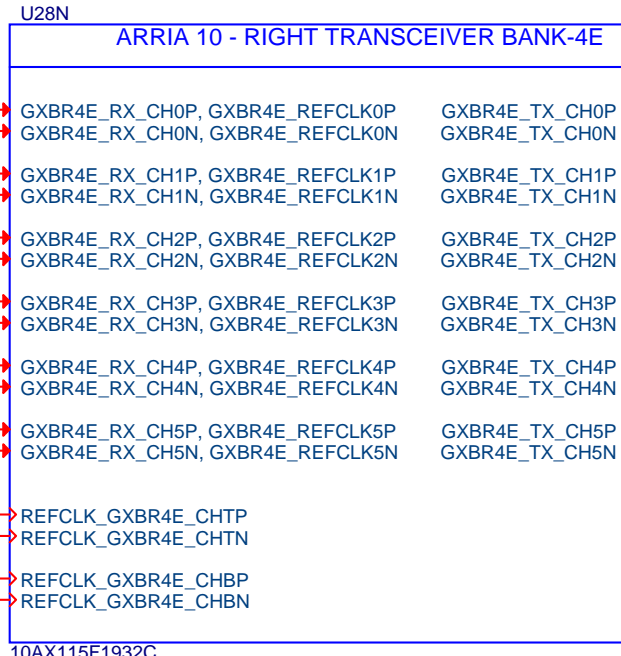
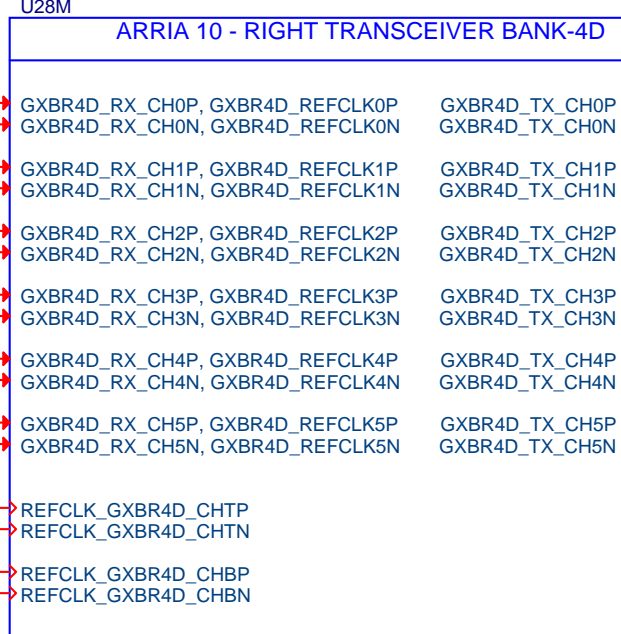
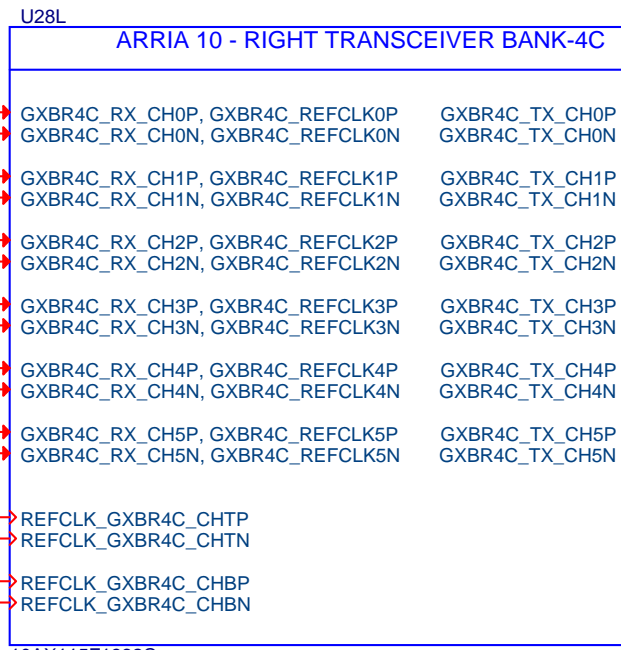


# Arria 10 Transceivers Left





# Arria 10 Transceivers Right

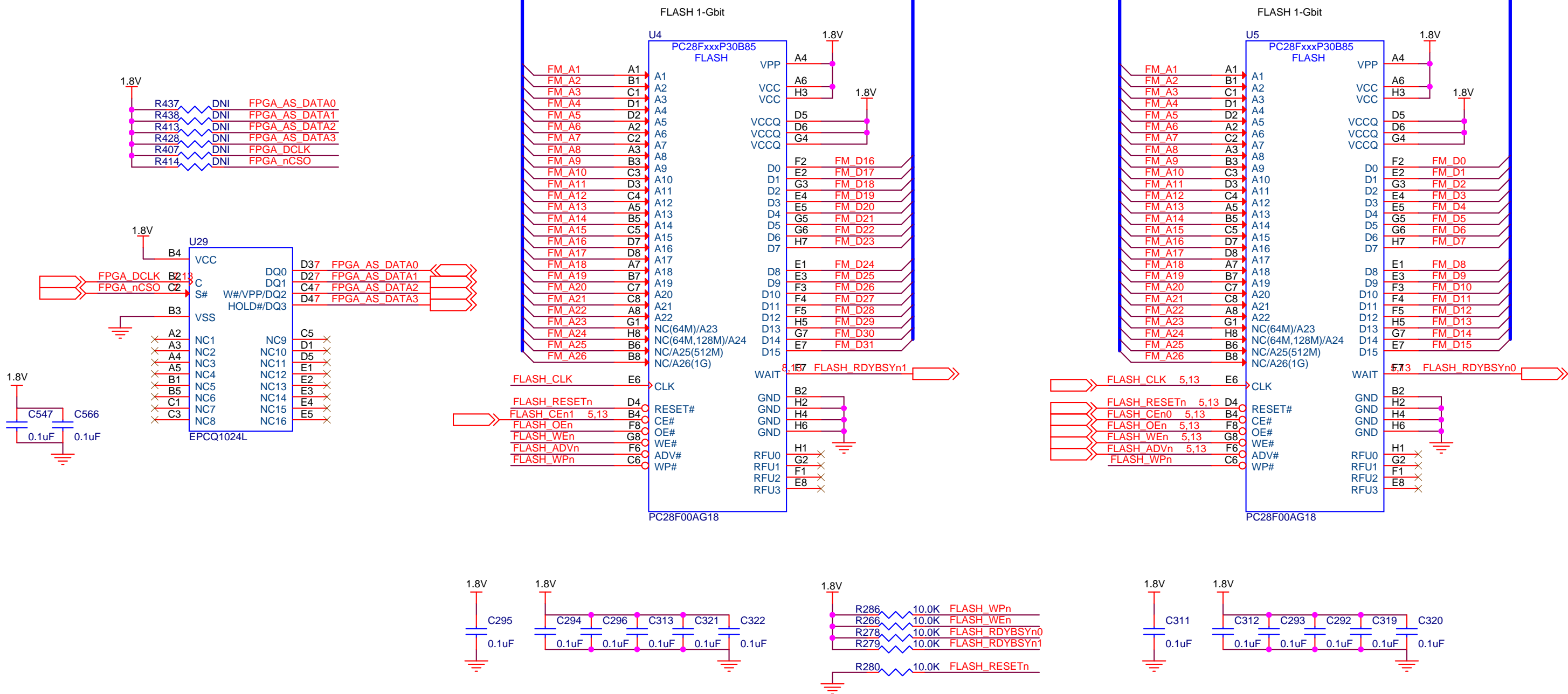




# FLASH

## FM BUS

FM\_D[31:0] 5,13  
FM\_A[26:1] 5,13



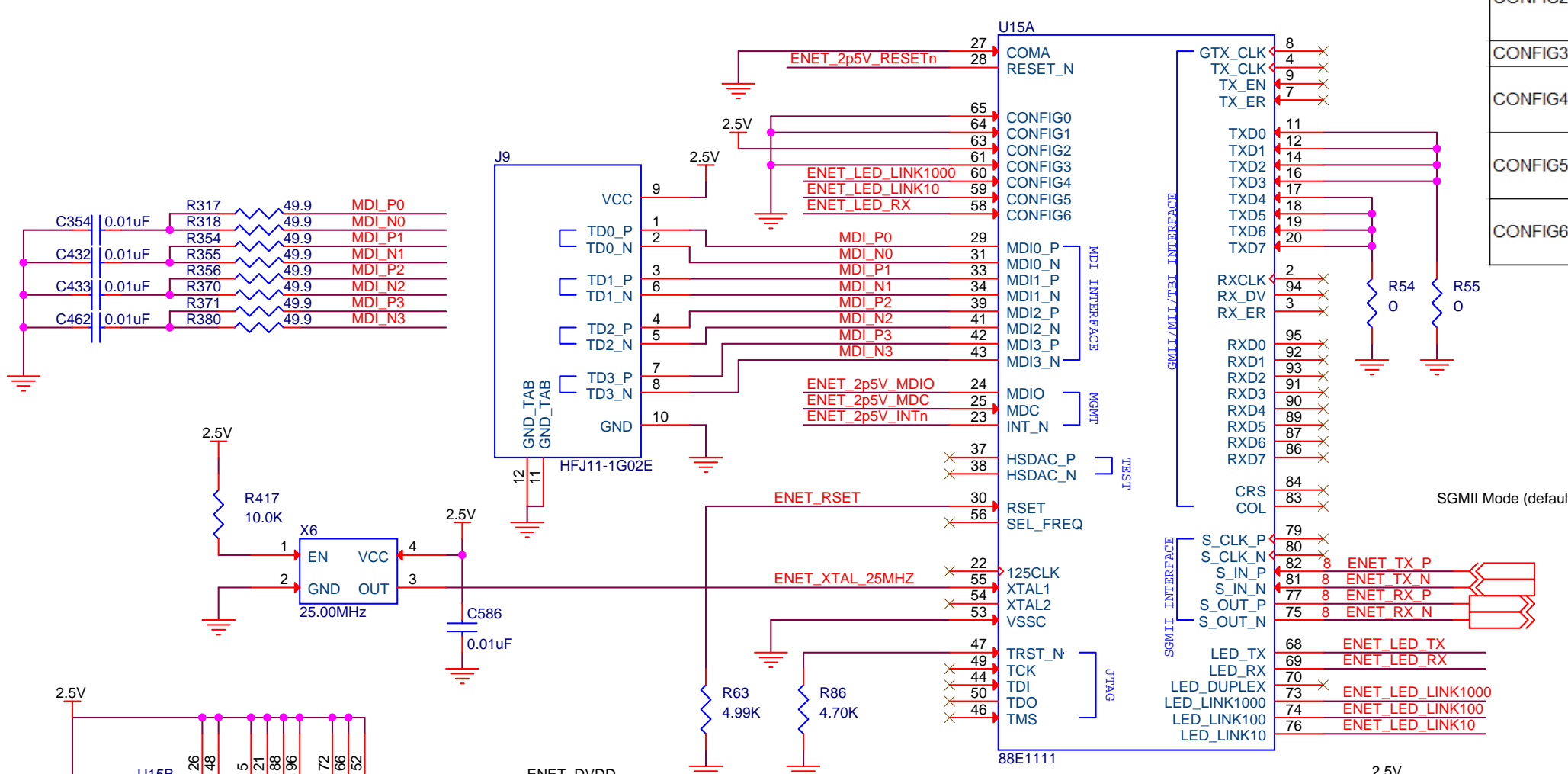
- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM\_A1 mapped to address bit 1 in software.
- When using dual x16 flash devices for an equivalent x32 (x16||x16) flash device a word consists of 32 data bits so addressing starts with FM\_A1 mapped to address bit 2 in software.



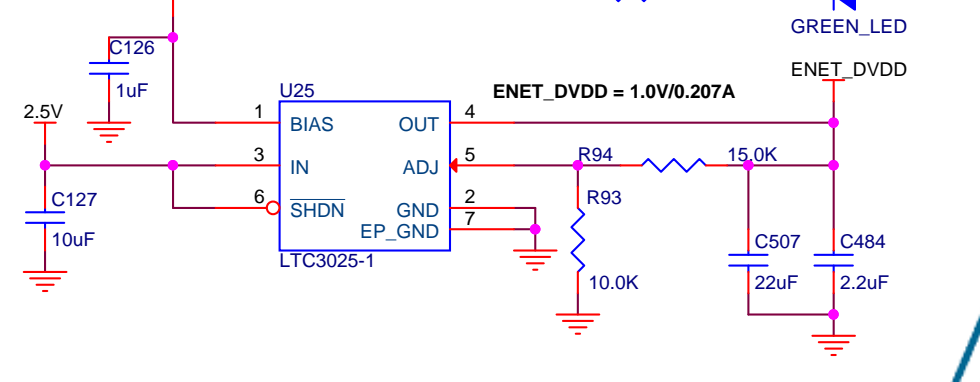
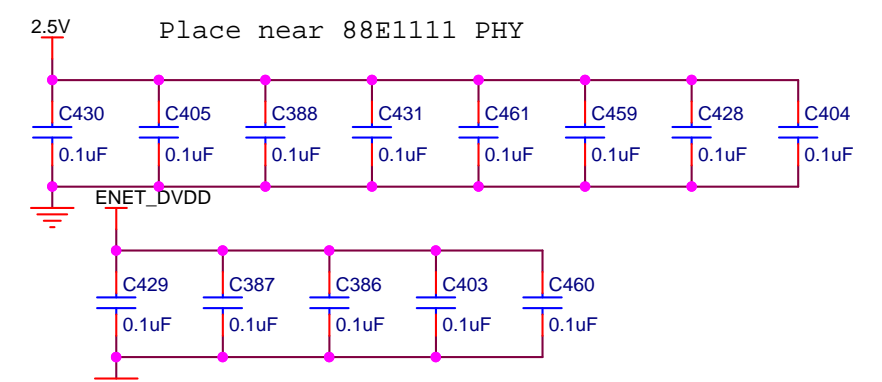
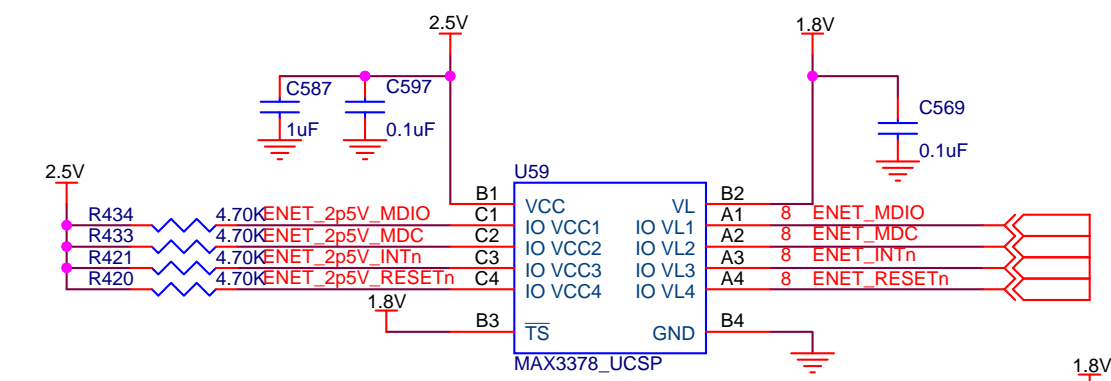
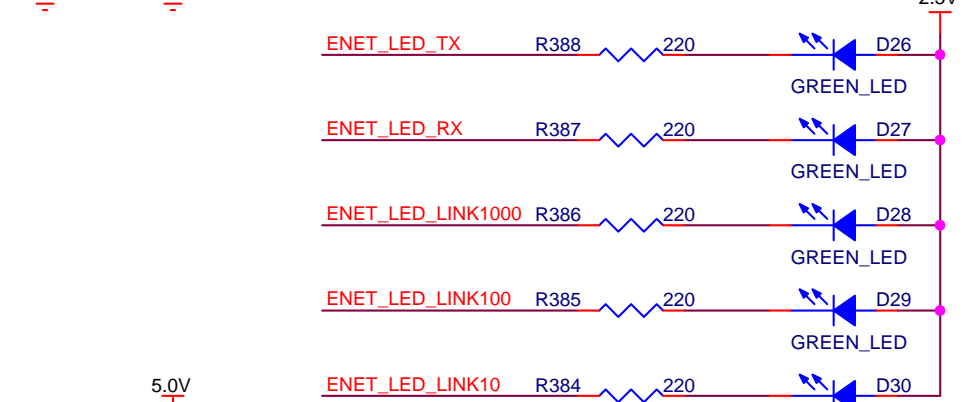
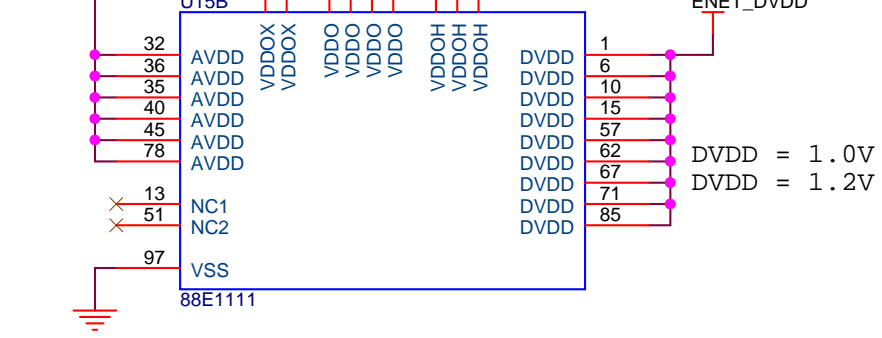


# 10/100/1000 Ethernet

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LINK10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber



**88E1111-B2-CAA1C000 EOL**  
**88E1111-B2-NDC2C000 Replacement**



# External Memory Interface Connector Map

DDR3 x72 (DQ5 x8)	DDR4 x72 (DQ5 x8 Groups)	RLDRAM3 x36 (DQ5 x8/x9 Groups)	QDR IV x36 (DQ5 x18 Groups)	HiLo Pin Name	HiLo Pin Number
				CONFIG0	L6
				CONFIG1	M6
A0	A0	A0	A1	MEM_ADDR_CMD[0]	F1
A1	A1	A1	A2	MEM_ADDR_CMD[1]	H1
A10	A10	A10	A11	MEM_ADDR_CMD[10]	E4
A11	A11	A11	A12	MEM_ADDR_CMD[11]	F4
A12	A12	A12	A13	MEM_ADDR_CMD[12]	G4
A13	A13	A13	A14	MEM_ADDR_CMD[13]	H4
A14	A14	A14	A15	MEM_ADDR_CMD[14]	J4
A15	A15	A15	A16	MEM_ADDR_CMD[15]	K4
BA0	BA0	BA0	A19	MEM_ADDR_CMD[16]	M1
BA1	BA1	BA1	A20	MEM_ADDR_CMD[17]	M2
BA2	BG0	BA2	A21	MEM_ADDR_CMD[18]	N2
CASn	A17	A17	A18	MEM_ADDR_CMD[19]	L4
A2	A2	A2	A3	MEM_ADDR_CMD[2]	F2
CKE0	CKE0	A20	RWAn	MEM_ADDR_CMD[20]	P5
CKE1	CKE1	WE <sub>n</sub>	RWB <sub>n</sub>	MEM_ADDR_CMD[21]	M5
CSn0	CSn0	CSn0	LBKOn	MEM_ADDR_CMD[22]	P1
CSn1	ACT <sub>n</sub>	CSn1	LBK1 <sub>n</sub>	MEM_ADDR_CMD[23]	R4
ODT0	ODT0	A18	LDAn	MEM_ADDR_CMD[24]	M4
ODT1	ODT1	A19	LDB <sub>n</sub>	MEM_ADDR_CMD[25]	R3
RASn	A16	A16	A17	MEM_ADDR_CMD[26]	L2
RESET <sub>n</sub>	RESET <sub>n</sub>	RESET <sub>n</sub>	RESET <sub>n</sub>	MEM_ADDR_CMD[27]	K1
WE <sub>n</sub>	BG1	BA3	CFG <sub>n</sub>	MEM_ADDR_CMD[28]	P2
	ALERT <sub>n</sub>	CSn3	A22	MEM_ADDR_CMD[29]	N4
A3	A3	A3	A4	MEM_ADDR_CMD[3]	G2
	CSn1	CSn2	AINV	MEM_ADDR_CMD[30]	P4
	PAR	REF <sub>n</sub>	A0	MEM_ADDR_CMD[31]	N3
A4	A4	A4	A5	MEM_ADDR_CMD[4]	H2
A5	A5	A5	A6	MEM_ADDR_CMD[5]	J2
A6	A6	A6	A7	MEM_ADDR_CMD[6]	K2
A7	A7	A7	A8	MEM_ADDR_CMD[7]	G3
A8	A8	A8	A9	MEM_ADDR_CMD[8]	J3
A9	A9	A9	A10	MEM_ADDR_CMD[9]	L3
CK_NO	CK_NO	CK_N	CK_N	MEM_CLK_N	V2
CK_PO	CK_PO	CK_P	CK_P	MEM_CLK_P	V1
DM0	LDM_n0		DINVA0	MEM_DMA[0]	B10
DM1	UDM_n0	DM1	QVLDA0	MEM_DMA[1]	C4
DM2	LDM_n1		DINVA1	MEM_DMA[2]	B17
DM3	UDM_n1		QVLDA1	MEM_DMA[3]	F17
DM4	LDM_n2	DQ18	DINVBO	MEM_DMB[0]	M16
DM5	UDM_n2		QVLDB0	MEM_DMB[1]	U16
DM6	LDM_n3	DQ0	DINVB1	MEM_DMB[2]	U11
DM7	UDM_n3		QVLDB1	MEM_DMB[3]	U6
DM8	LDM_n4			MEM_DQ_ADDR_CMD[0]	R6
DQ64	DQ64			MEM_DQ_ADDR_CMD[1]	T1
DQ65	DQ65			MEM_DQ_ADDR_CMD[2]	R2
DQ66	DQ66			MEM_DQ_ADDR_CMD[3]	T2

DDR3 x72 (DQ5 x8)	DDR4 x72 (DQ5 x8 Groups)	RLDRAM3 x36 (DQ5 x8/x9 Groups)	QDR IV x36 (DQ5 x18 Groups)	HiLo Pin Name	HiLo Pin Number
DQ67	DQ67			MEM_DQ_ADDR_CMD[4]	U2
DQ68	DQ68			MEM_DQ_ADDR_CMD[5]	U3
DQ69	DQ69		AP	MEM_DQ_ADDR_CMD[6]	T4
DQ70	DQ70		A24	MEM_DQ_ADDR_CMD[7]	U4
DQ71	DQ71		A23	MEM_DQ_ADDR_CMD[8]	T5
DQ0	DQ0		DQA0	MEM_DQA[0]	A4
DQ1	DQ1		DQA1	MEM_DQA[1]	B4
DQ10	DQ10	DQ11	DQA9	MEM_DQA[10]	C2
DQ11	DQ11	DQ12	DQA10	MEM_DQA[11]	C3
DQ12	DQ12	DQ13	DQA11	MEM_DQA[12]	E3
DQ13	DQ13	DQ14	DQA12	MEM_DQA[13]	D4
DQ14	DQ14	DQ15	DQA13	MEM_DQA[14]	D1
DQ15	DQ15	DQ16	DQA14	MEM_DQA[15]	D2
DQ16	DQ16	QVLD1	DQA18	MEM_DQA[16]	A12
DQ17	DQ17		DQA19	MEM_DQA[17]	B12
DQ18	DQ18		DQA20	MEM_DQA[18]	B13
DQ19	DQ19		DQA21	MEM_DQA[19]	B14
DQ2	DQ2		DQA2	MEM_DQA[2]	B5
DQ20	DQ20		DQA22	MEM_DQA[20]	C15
DQ21	DQ21		DQA23	MEM_DQA[21]	A16
DQ22	DQ22		DQA24	MEM_DQA[22]	B16
DQ23	DQ23		QKA_N1	MEM_DQA[23]	A18
DQ24	DQ24	DQ27	DQA25	MEM_DQA[24]	C16
DQ25	DQ25	DQ28	DQA26	MEM_DQA[25]	D16
DQ26	DQ26	DQ29	DQA27	MEM_DQA[26]	E16
DQ27	DQ27	DQ30	DQA28	MEM_DQA[27]	F16
DQ28	DQ28	DQ31	DQA29	MEM_DQA[28]	D17
DQ29	DQ29	DQ32	DQA30	MEM_DQA[29]	C18
DQ3	DQ3		DQA3	MEM_DQA[3]	B6
DQ30	DQ30	DQ33	DQA31	MEM_DQA[30]	D18
DQ31	DQ31	DQ34	DQA32	MEM_DQA[31]	E18
		DQ17	DQA15	MEM_DQA[32]	E2
		DQ35	DQA33	MEM_DQA[33]	G16
DQ4	DQ4		DQA4	MEM_DQA[4]	A8
DQ5	DQ5		DQA5	MEM_DQA[5]	B8
DQ6	DQ6		DQA6	MEM_DQA[6]	B9
DQ7	DQ7		QKA_NO	MEM_DQA[7]	A10
DQ8	DQ8	DQ9	DQA7	MEM_DQA[8]	B1
DQ9	DQ9	DQ10	DQA8	MEM_DQA[9]	B2
DQ32	DQ32	DQ19	DQB0	MEM_DQB[0]	H16
DQ33	DQ33	DQ20	DQB1	MEM_DQB[1]	J16
DQ42	DQ42		DQB9	MEM_DQB[10]	P17
DQ43	DQ43		DQB10	MEM_DQB[11]	P18
DQ44	DQ44		DQB11	MEM_DQB[12]	R18
DQ45	DQ45		DQB12	MEM_DQB[13]	T16
DQ46	DQ46		DQB13	MEM_DQB[14]	T17
DQ47	DQ47		DQB14	MEM_DQB[15]	T18
DQ48	DQ48	DQ1	DQB18	MEM_DQB[16]	U15

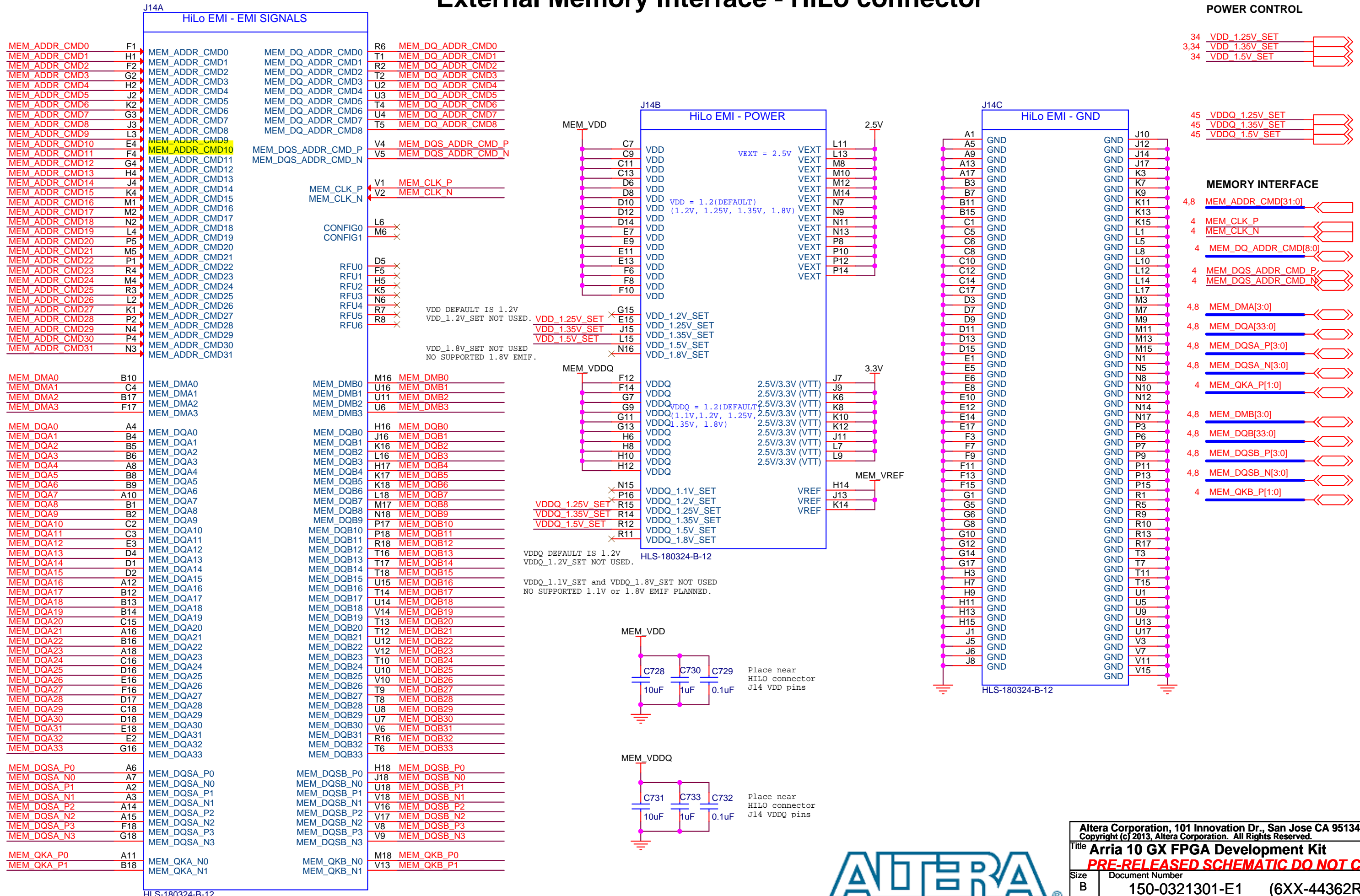
DDR3 x72 (DQ5 x8)	DDR4 x72 (DQ5 x8 Groups)	RLDRAM3 x36 (DQ5 x8/x9 Groups)	QDR IV x36 (DQ5 x18 Groups)	HiLo Pin Name	HiLo Pin Number
DQ49	DQ49	DQ2	DQB19	MEM_DQB[17]	T14
DQ50	DQ50	DQ3	DQB20	MEM_DQB[18]	U14
DQ51	DQ51	DQ4	DQB21	MEM_DQB[19]	V14
DQ34	DQ34	DQ21	DQB2	MEM_DQB[2]	K16
DQ52	DQ52	DQ5	DQB22	MEM_DQB[20]	T13
DQ53	DQ53	DQ6	DQB23	MEM_DQB[21]	T12
DQ54	DQ54	DQ7	DQB24	MEM_DQB[22]	U12
DQ55	DQ55	DQ8	QKB_N1	MEM_DQB[23]	V12
DQ56	DQ56		DQB25	MEM_DQB[24]	T10
DQ57	DQ57		DQB26	MEM_DQB[25]	U10
DQ58	DQ58		DQB27	MEM_DQB[26]	V10
DQ59	DQ59		DQB28	MEM_DQB[27]	T9
DQ60	DQ60		DQB29	MEM_DQB[28]	T8
DQ61	DQ61		DQB30	MEM_DQB[29]	U8
DQ35	DQ35	DQ22	DQB3	MEM_DQB[3]	L16
DQ62	DQ62		DQB31	MEM_DQB[30]	U7
DQ63	DQ63		DQB32	MEM_DQB[31]	V6
			DQB15	MEM_DQB[32]	R16
			DQB33	MEM_DQB[33]	T6
DQ36	DQ36	DQ23	DQB4	MEM_DQB[4]	H17
DQ37	DQ37	DQ24	DQB5	MEM_DQB[5]	K17
DQ38	DQ38	DQ25	DQB6	MEM_DQB[6]	K18
DQ39	DQ39	DQ26	QKB_NO	MEM_DQB[7]	L18
DQ40	DQ40	QVLD0	DQB7	MEM_DQB[8]	M17
DQ41	DQ41		DQB8	MEM_DQB[9]	N18
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DQS_P8	DQSL_P4		PE <sub>n</sub>	MEM_DQS_ADDR_CMD_P	V4
DQS_NO	DQSL_NO		DQA17	MEM_DQSA_N[0]	A7
DQS_N1	DQSU_NO	QK1#	DQA_NO	MEM_DQSA_N[1]	A3
DQS_N2	DQSL_N1	DK1#	DQA35	MEM_DQSA_N[2]	A15
DQS_N3	DQSU_N1	QK3#	DQA_N1	MEM_DQSA_N[3]	G18
DQS_PO	DQSL_PO		DQA16	MEM_DQSA_P[0]	A6
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DQS_P2	DQSL_P1	DK1	DQA34	MEM_DQSA_P[2]	A14
DQS_P3	DQSU_P1	QK3	DQA_P1	MEM_DQSA_P[3]	F18
DQS_N4	DQSL_N2	QK2#	DQB17	MEM_DQSB_N[0]	J18
DQS_N5	DQSU_N2	DK0#	DKB_NO	MEM_DQSB_N[1]	V18
DQS_N6	DQSL_N3	QK0#	DQB35	MEM_DQSB_N[2]	V17
DQS_N7	DQSU_N3		DKB_N1	MEM_DQSB_N[3]	V9
DQS_P4	DQSL_P2	QK2	DQB16	MEM_DQSB_P[0]	H18
DQS_P5	DQSU_P2	DK0	DKB_PO	MEM_DQSB_P[1]	U18
DQS_P6	DQSL_P3	QK0	DQB34	MEM_DQSB_P[2]	V16
DQS_P7	DQSU_P3		DKB_P1	MEM_DQSB_P[3]	V8
			QKA_PO	MEM_QKA_P[0]	A11
			QKA_P1	MEM_QKA_P[1]	B18
			QKB_PO	MEM_QKB_P[0]	M18
		DM0	QKB_P1	MEM_QKB_P[1]	V13

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 Date: Thursday, May 28, 2015 Sheet 16 of 49





# External Memory Interface - HiLo connector



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**Title** Arria 10 GX FPGA Development Kit  
**PRE-RELEASED SCHEMATIC DO NOT COPY**

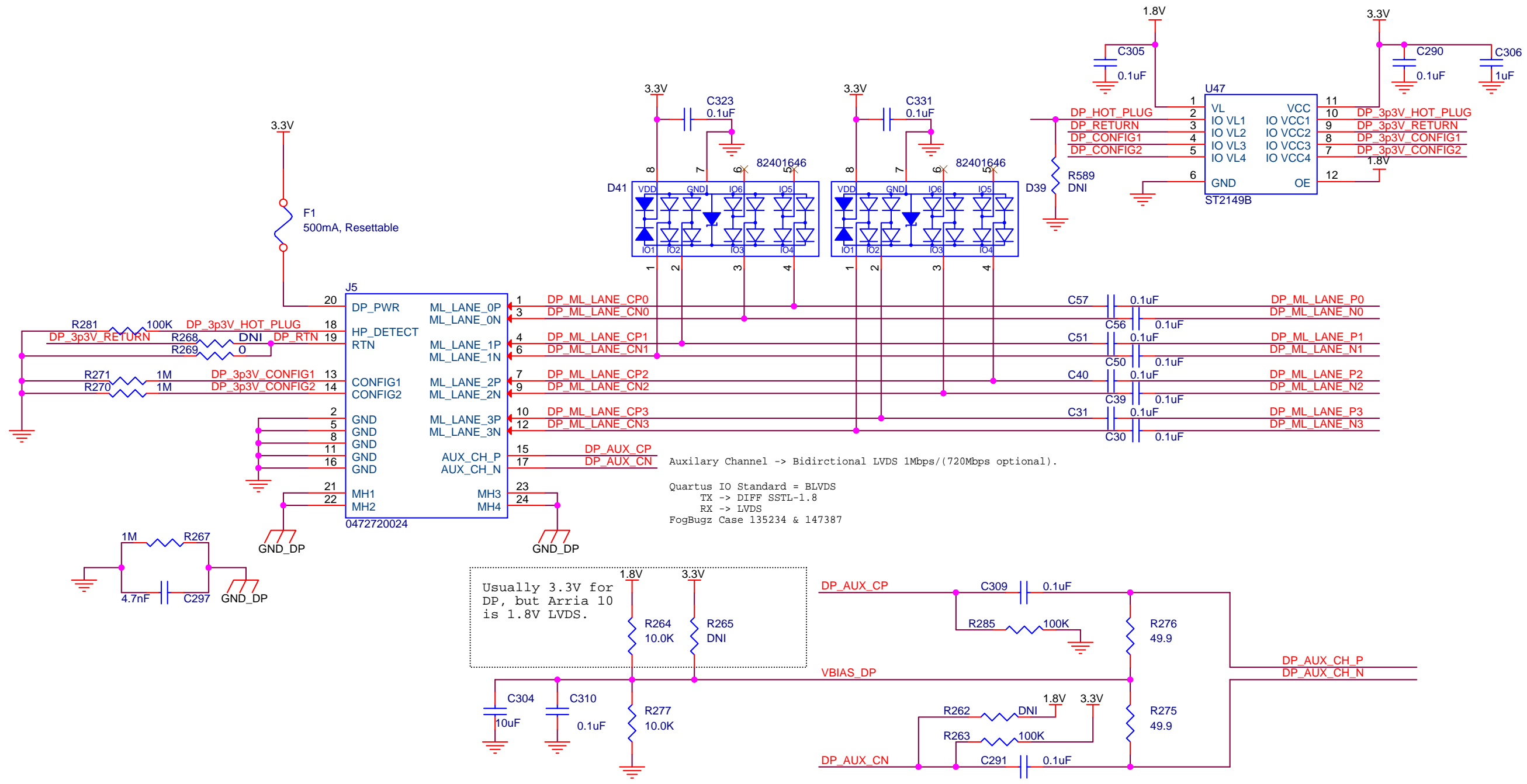
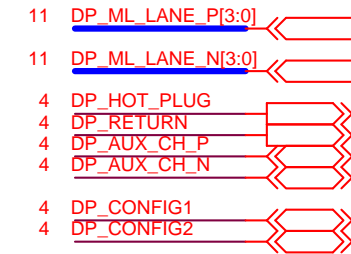
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<b>Date:</b> Thursday, May 28, 2015		<b>Sheet</b> 17 of 49



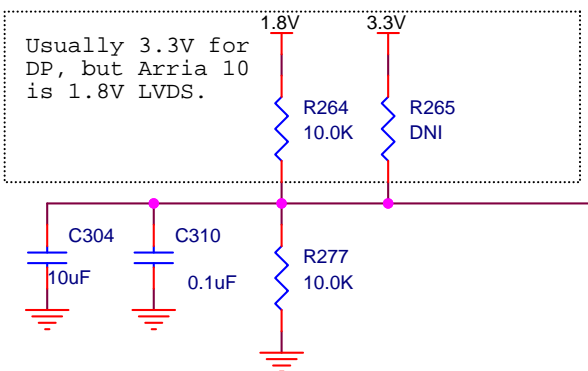


# Display Port (x4)

## DISPLAYPORT INTERFACE



Auxiliary Channel -> Bidirectional LVDS 1Mbps/(720Mbps optional).  
 Quartus IO Standard = BLVDS  
 TX -> DIFF SSTL-1.8  
 RX -> LVDS  
 FogBugz Case 135234 & 147387

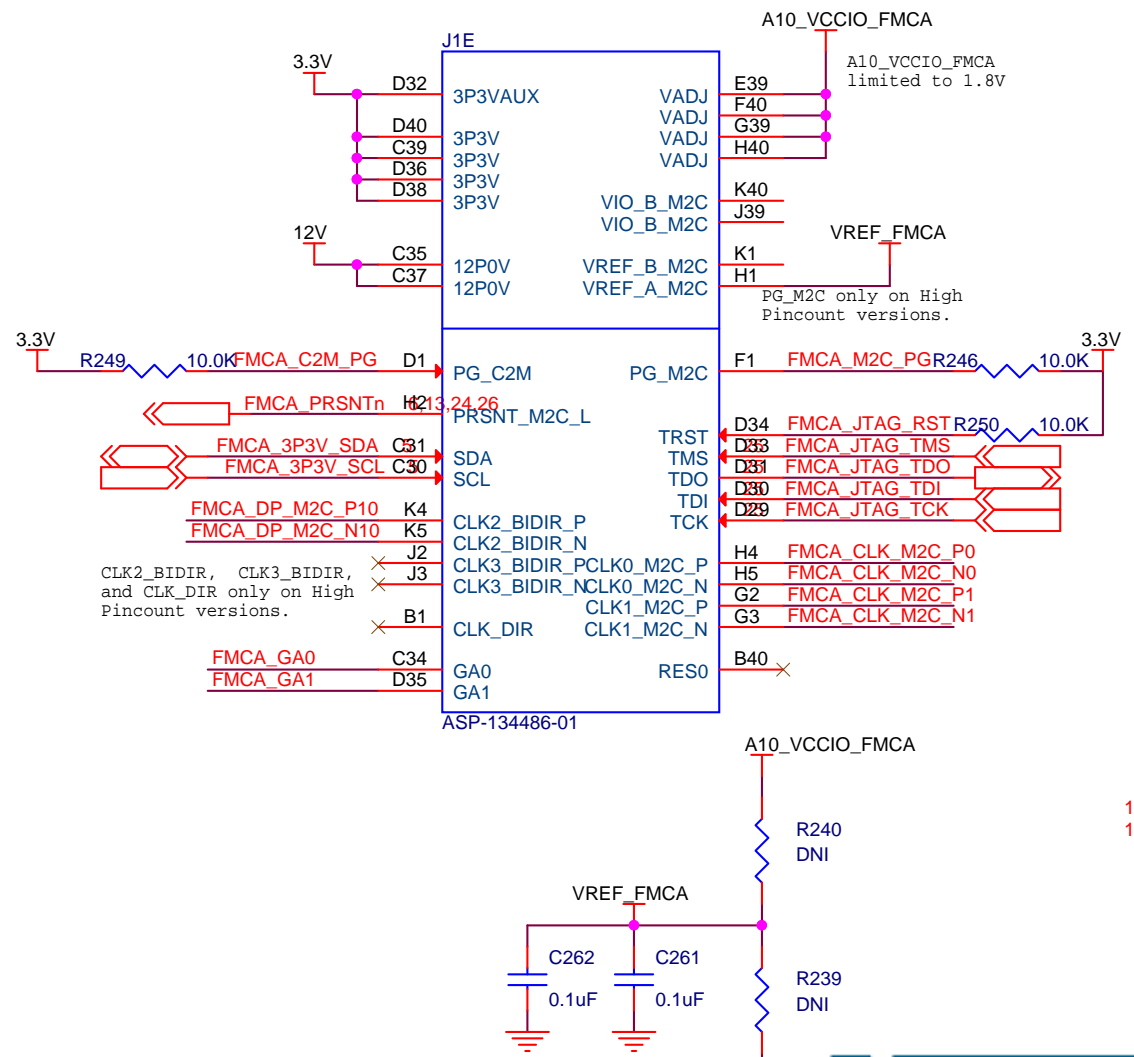
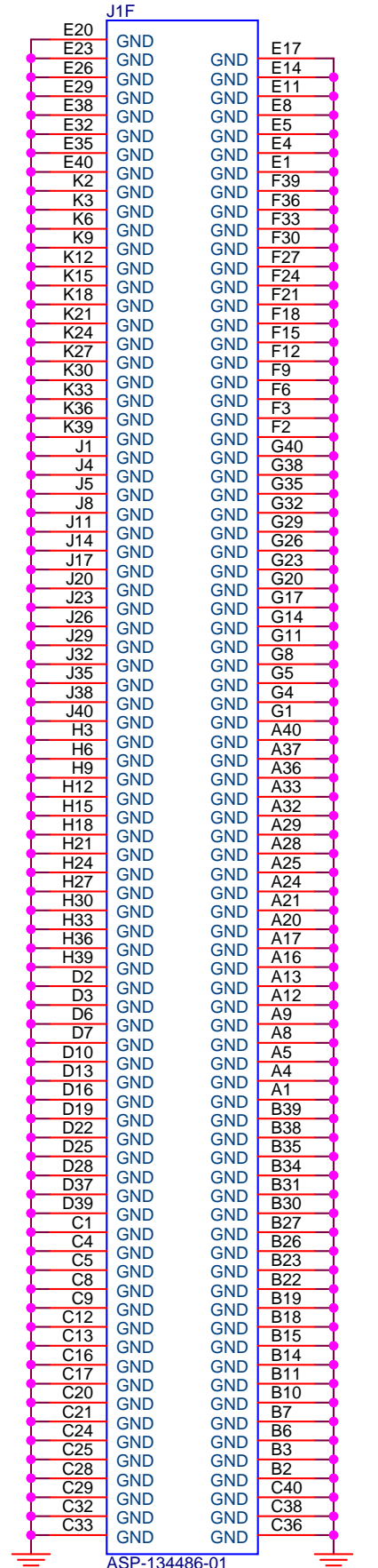
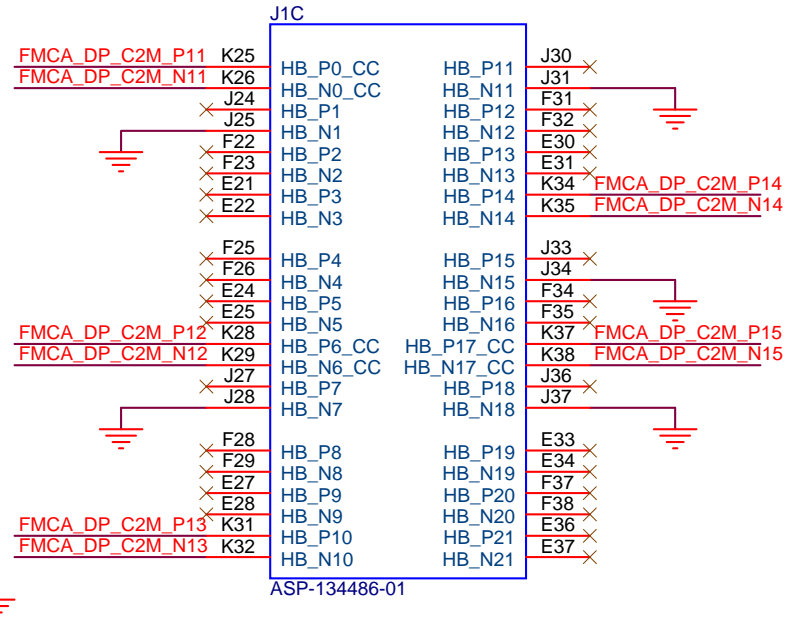
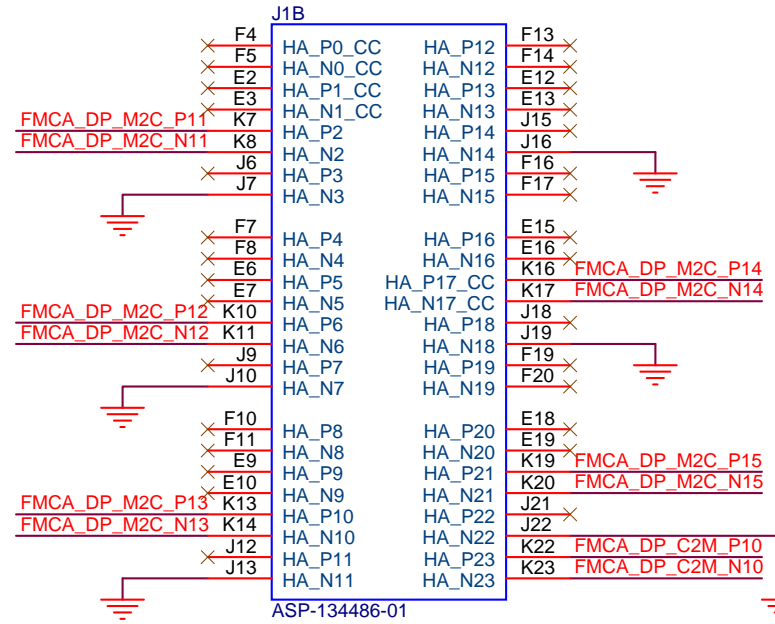
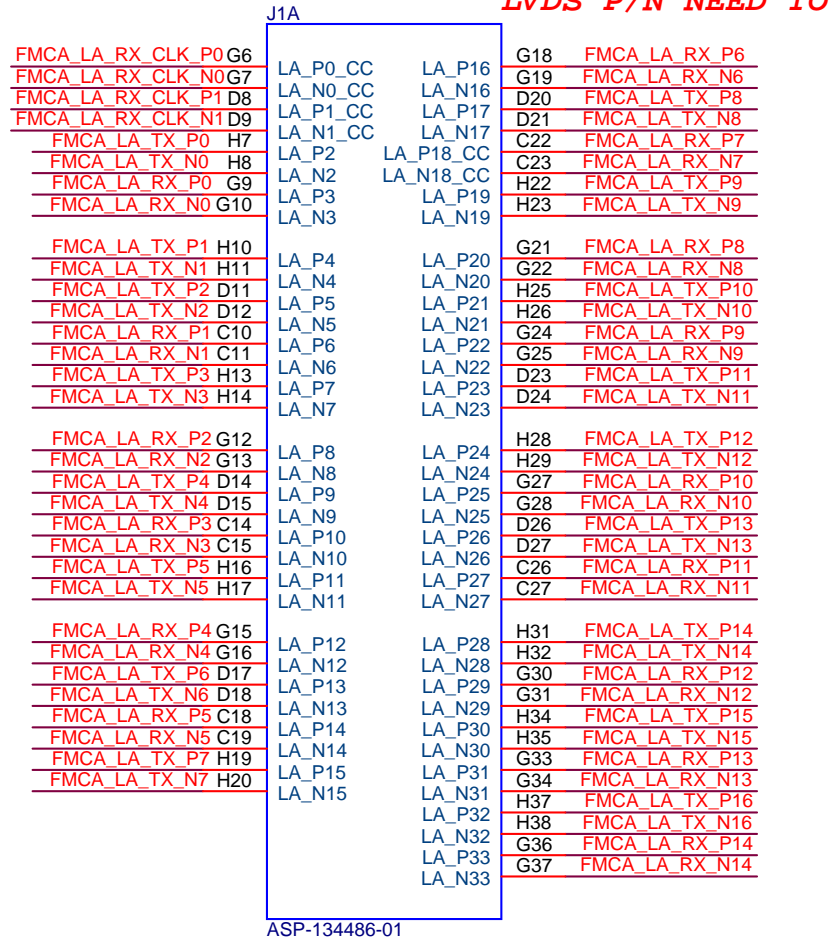


- 1) TX uses diff sstl18 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
- 2) RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9v.
  - a. If the channel is AC couple, then user need to choose the correct Vbias\_RX so that Vpin < 1.9v. The spec is 0 - 2v, which is quite wide. Selecting Vbias\_Rx at 2v region will cause NF device to have reliability issue.
  - b. If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.

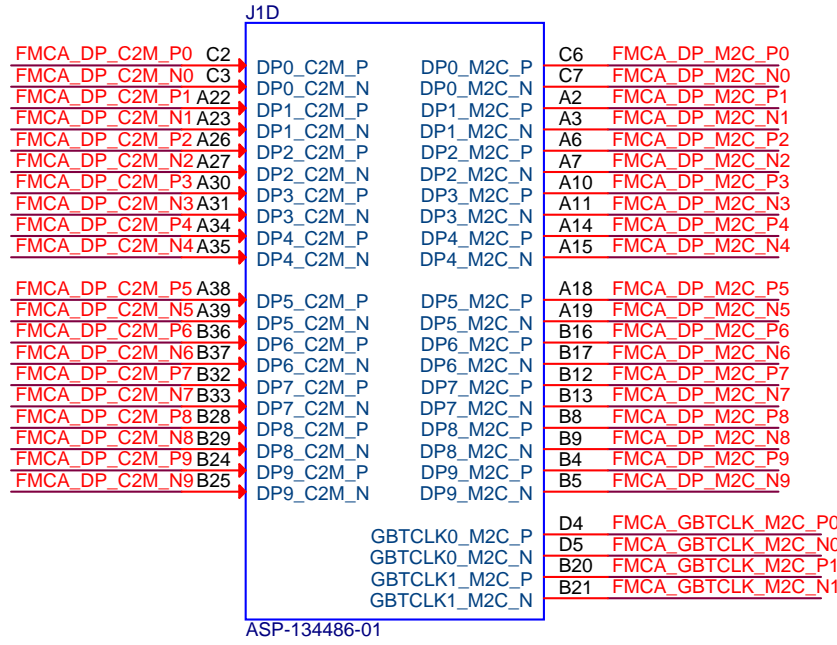


# FMC Port A

**LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.**

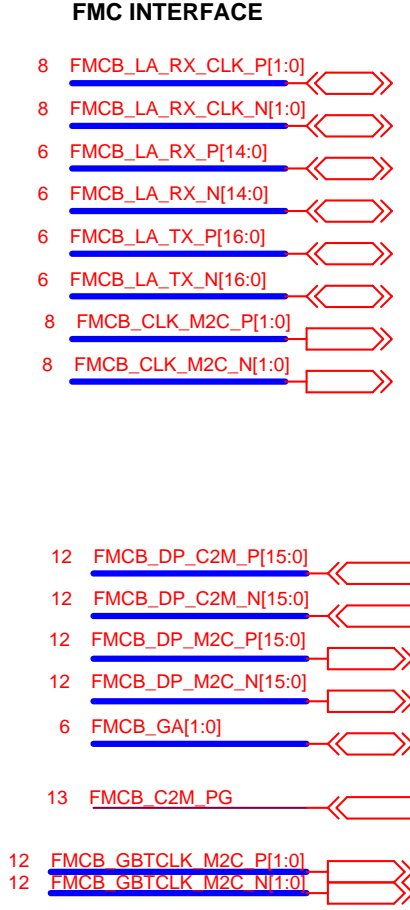
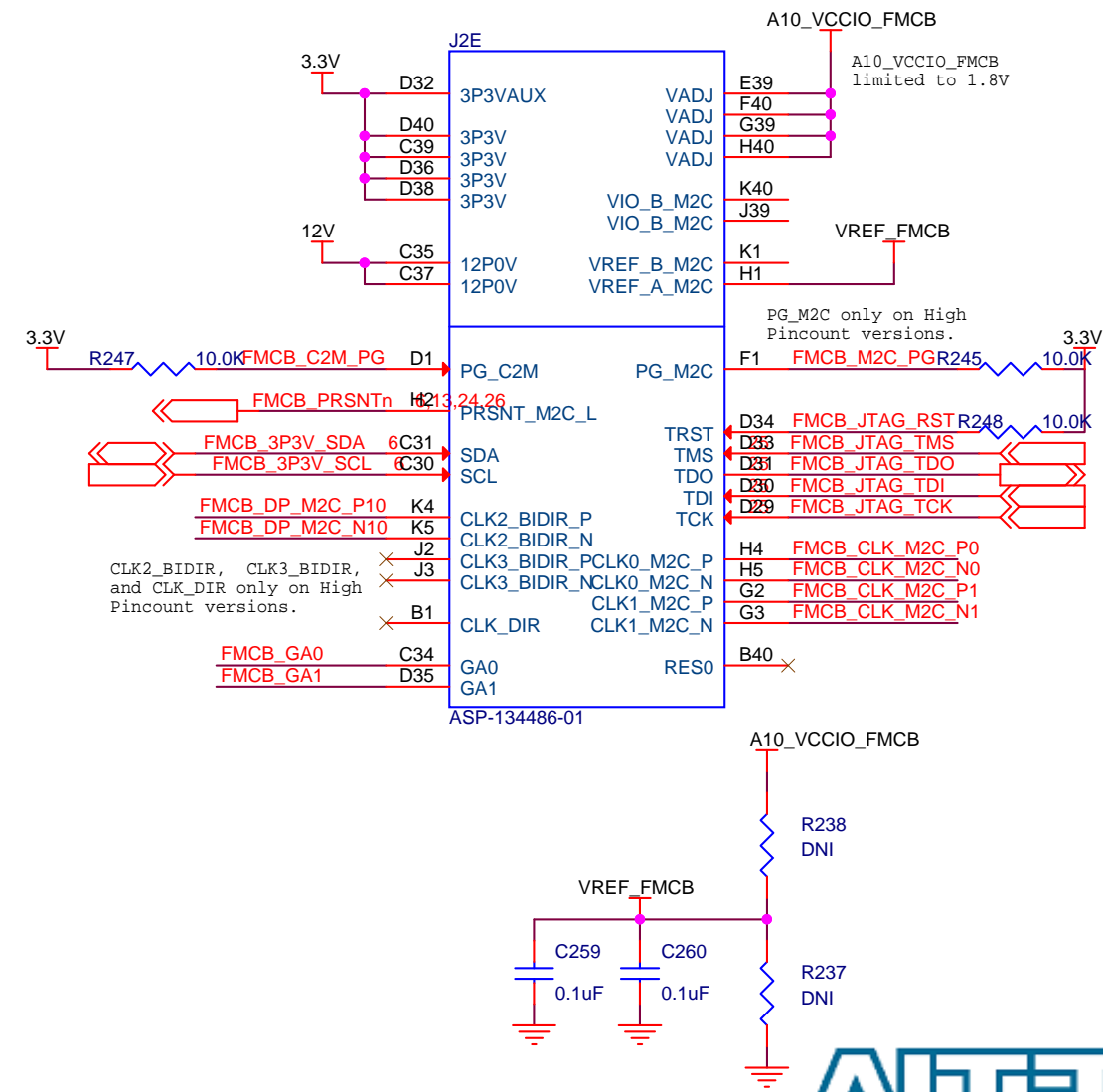
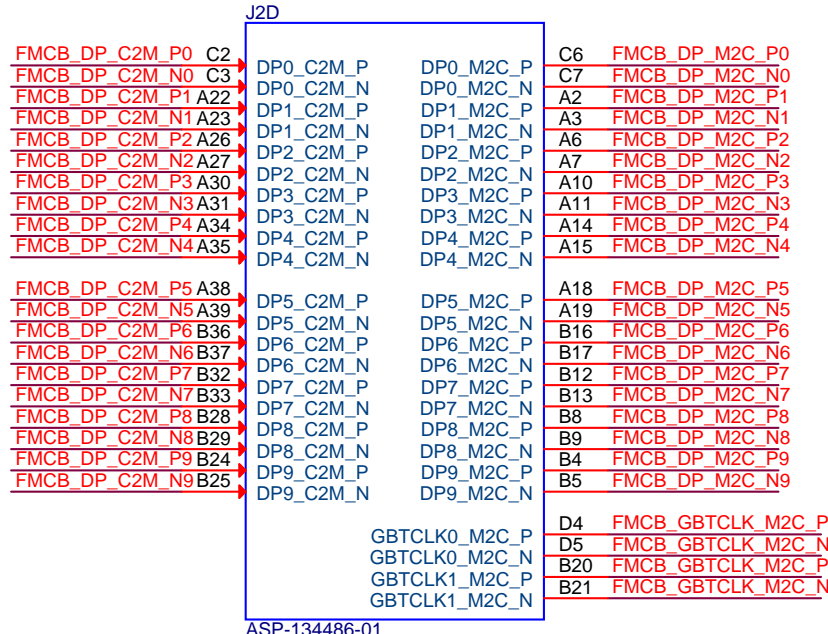
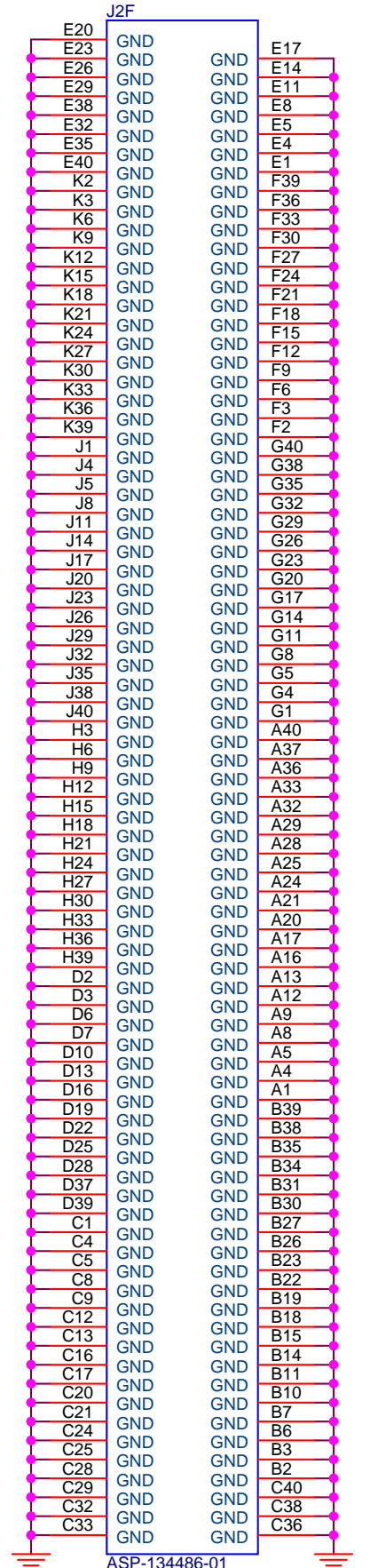
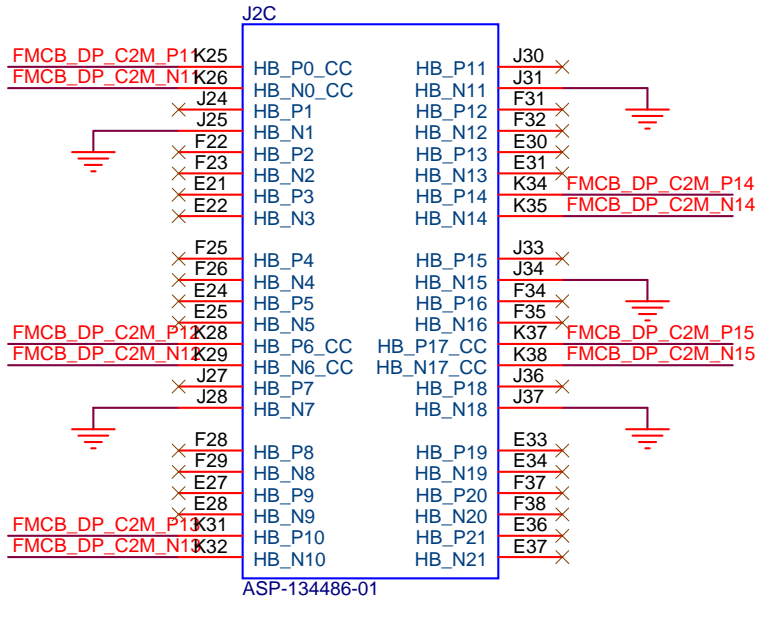
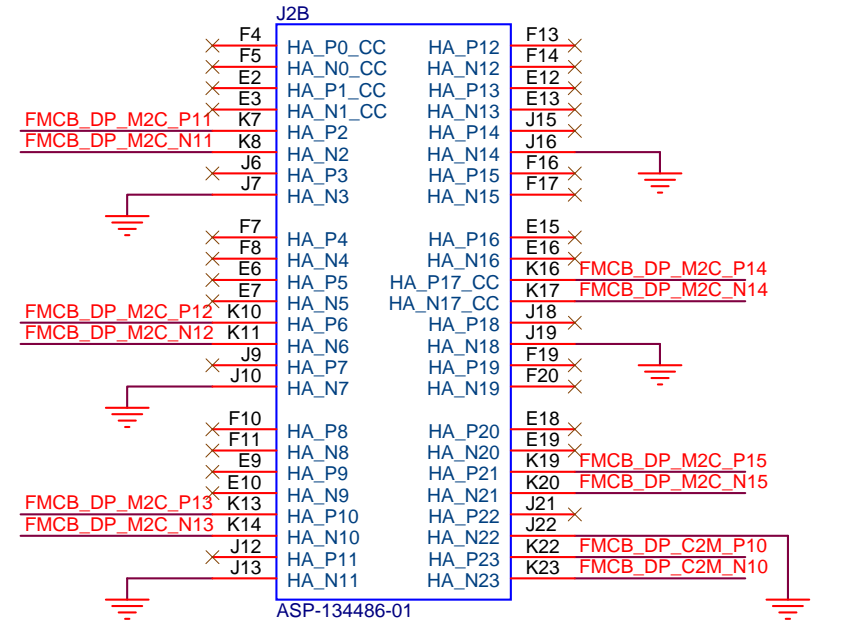
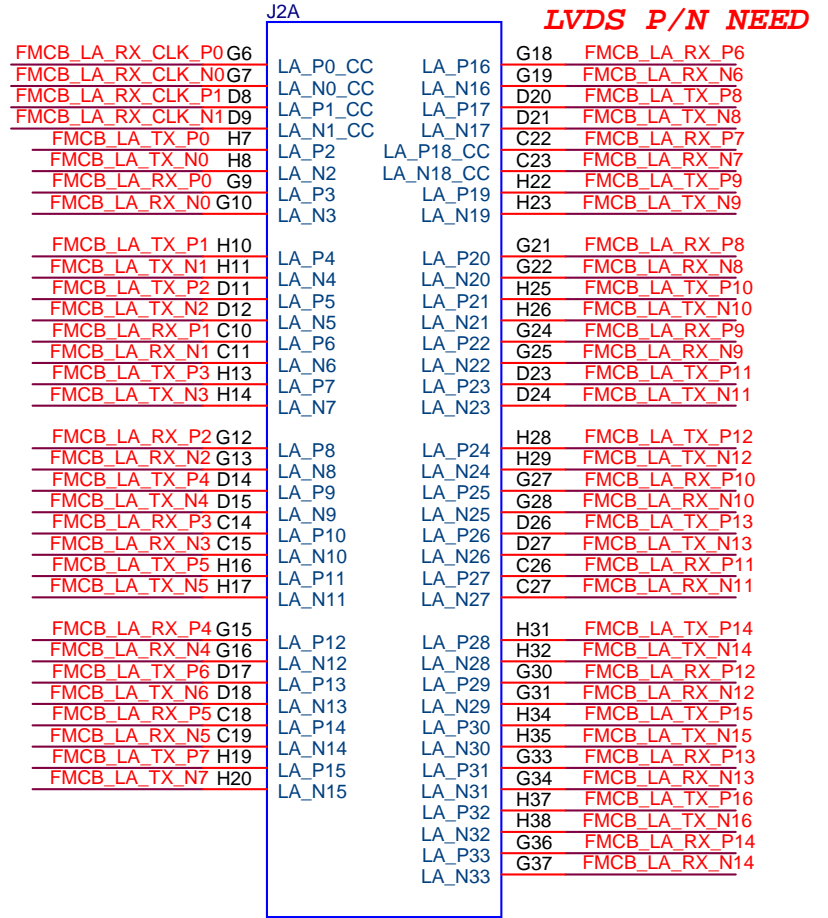


- FMC INTERFACE**
- 8 FMCA\_LA\_RX\_CLK\_P[1:0]
  - 8 FMCA\_LA\_RX\_CLK\_N[1:0]
  - 5 FMCA\_LA\_RX\_P[14:0]
  - 5 FMCA\_LA\_RX\_N[14:0]
  - 5 FMCA\_LA\_TX\_P[16:0]
  - 5 FMCA\_LA\_TX\_N[16:0]
  - 8 FMCA\_CLK\_M2C\_P[1:0]
  - 8 FMCA\_CLK\_M2C\_N[1:0]
  - 12 FMCA\_DP\_C2M\_P[15:0]
  - 12 FMCA\_DP\_C2M\_N[15:0]
  - 12 FMCA\_DP\_M2C\_P[15:0]
  - 12 FMCA\_DP\_M2C\_N[15:0]
  - 5 FMCA\_GA[1:0]
  - 13 FMCA\_C2M\_PG
  - 12 FMCA\_GBTCLK\_M2C\_P[1:0]
  - 12 FMCA\_GBTCLK\_M2C\_N[1:0]



# FMC Port B

**LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.**





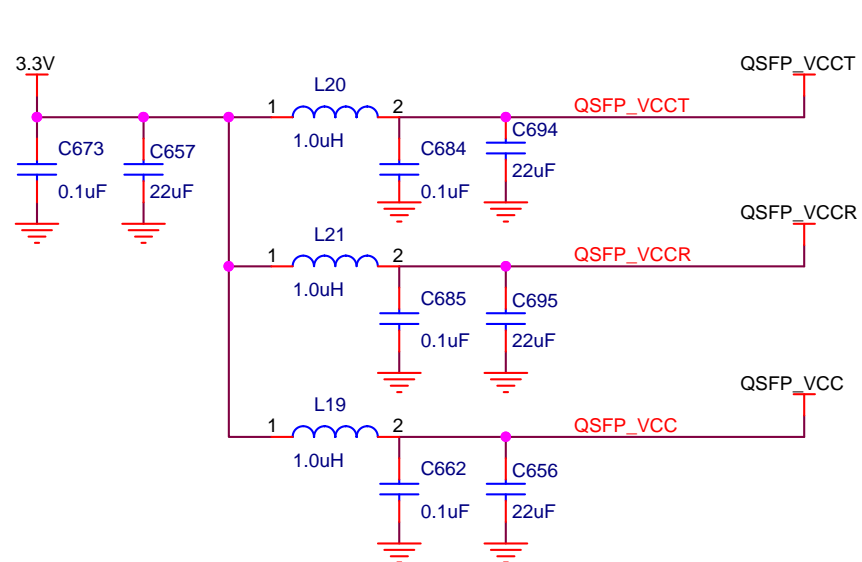
# Quad Small Form-factor Pluggable (QSFP) Interface

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

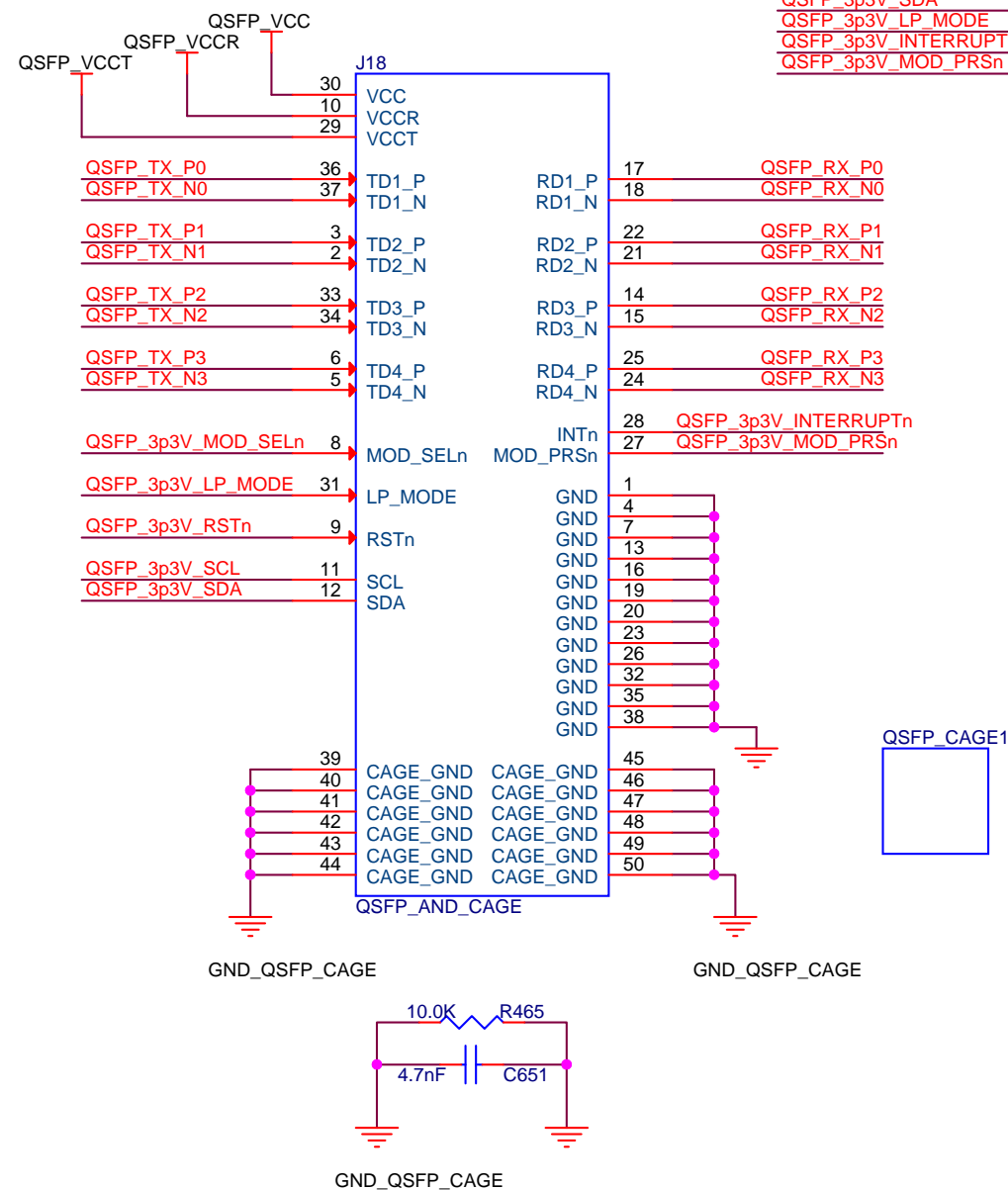
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

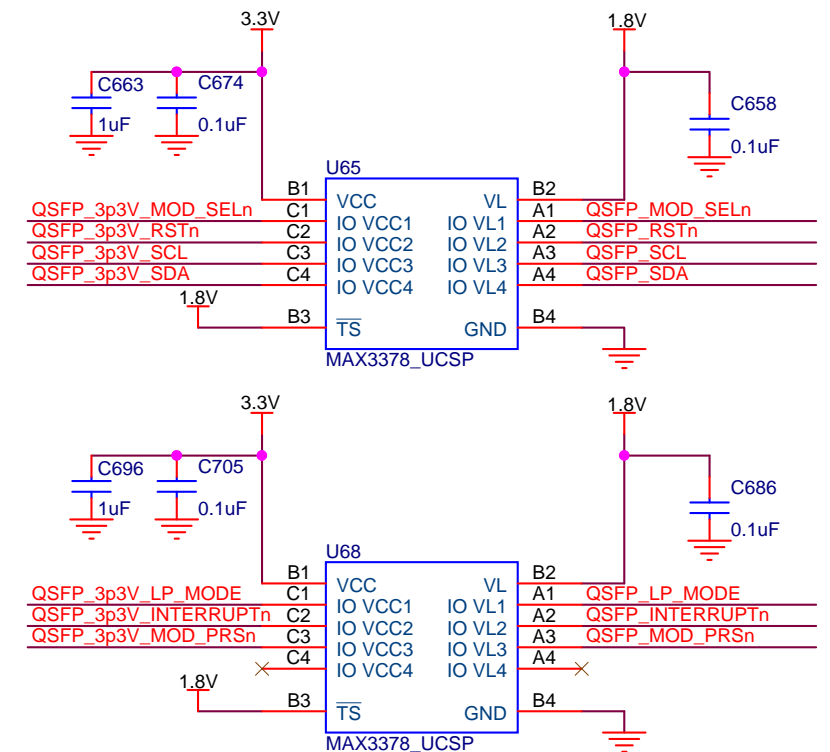
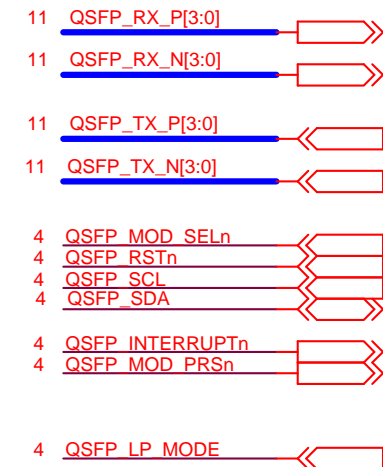


Maximum power is  $\leq 3.5W$  (1.06 A)  
Maximum inrush current = 1.3A



QSFP_3p3V_MOD_SELn	R486	4.70K	3.3V
QSFP_3p3V_RSTn	R500	4.70K	
QSFP_3p3V_SCL	R516	4.70K	
QSFP_3p3V_SDA	R528	4.70K	
QSFP_3p3V_LP_MODE	R485	4.70K	
QSFP_3p3V_INTERRUPTn	R501	4.70K	
QSFP_3p3V_MOD_PRSn	R517	4.70K	

## QSFP INTERFACE

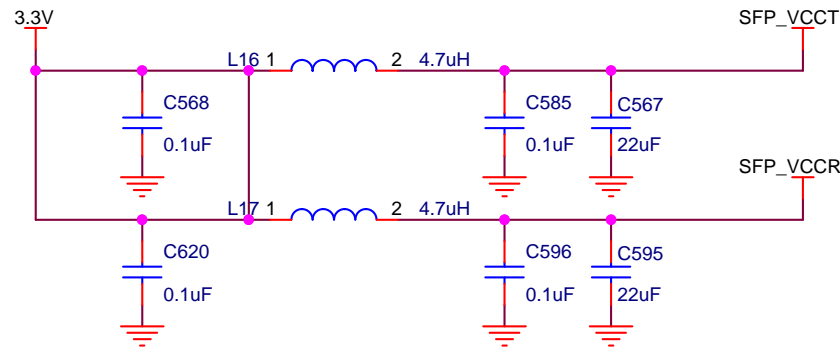


# Small Form Factor Pluggable Plus (SFP+) Connector

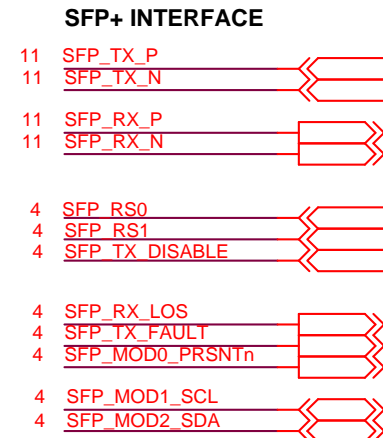
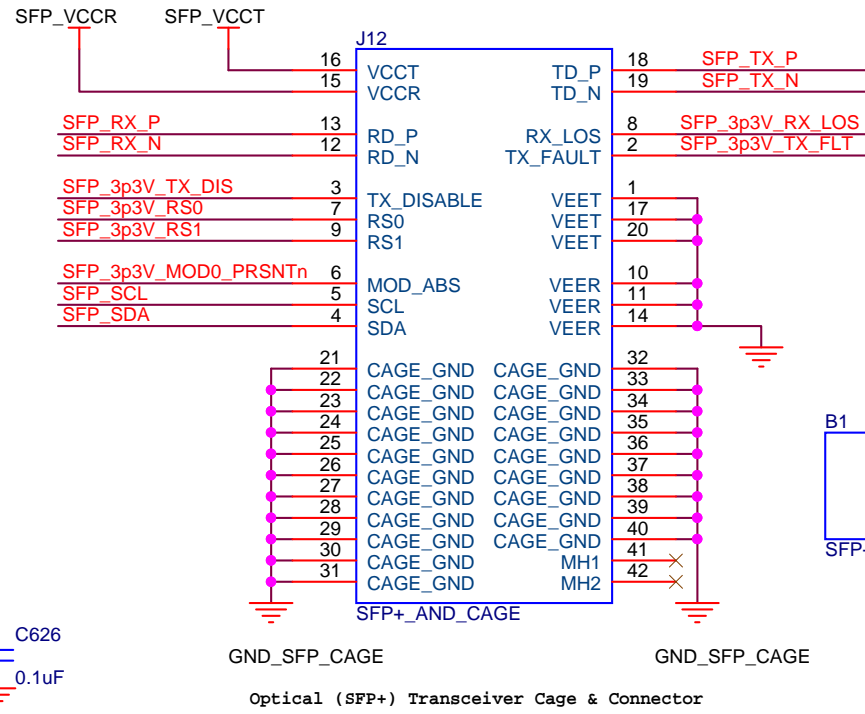
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

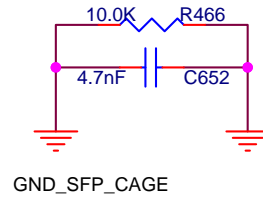
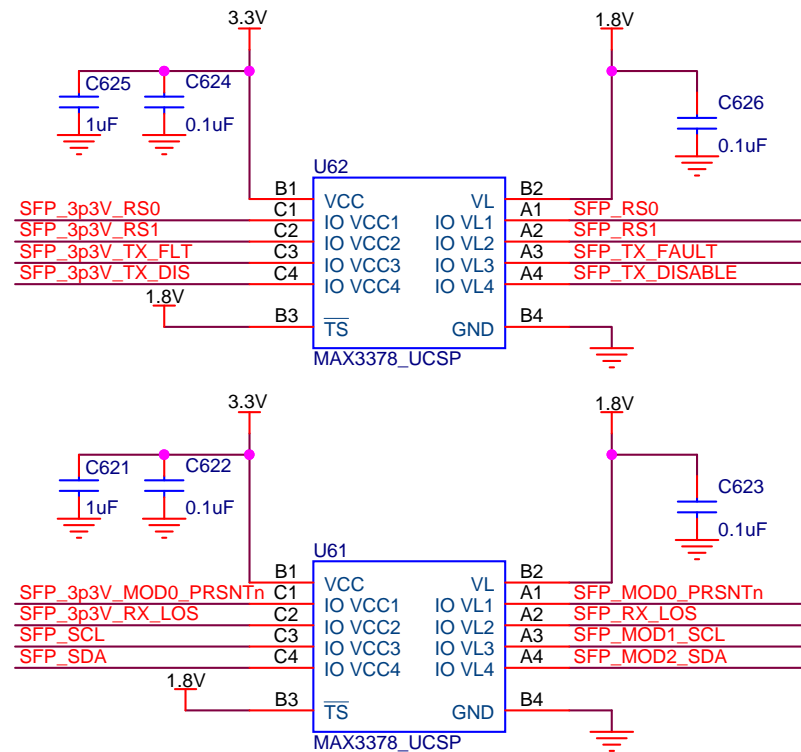
NOTE 3: DC blocking capacitors are in the module for RX and TX.



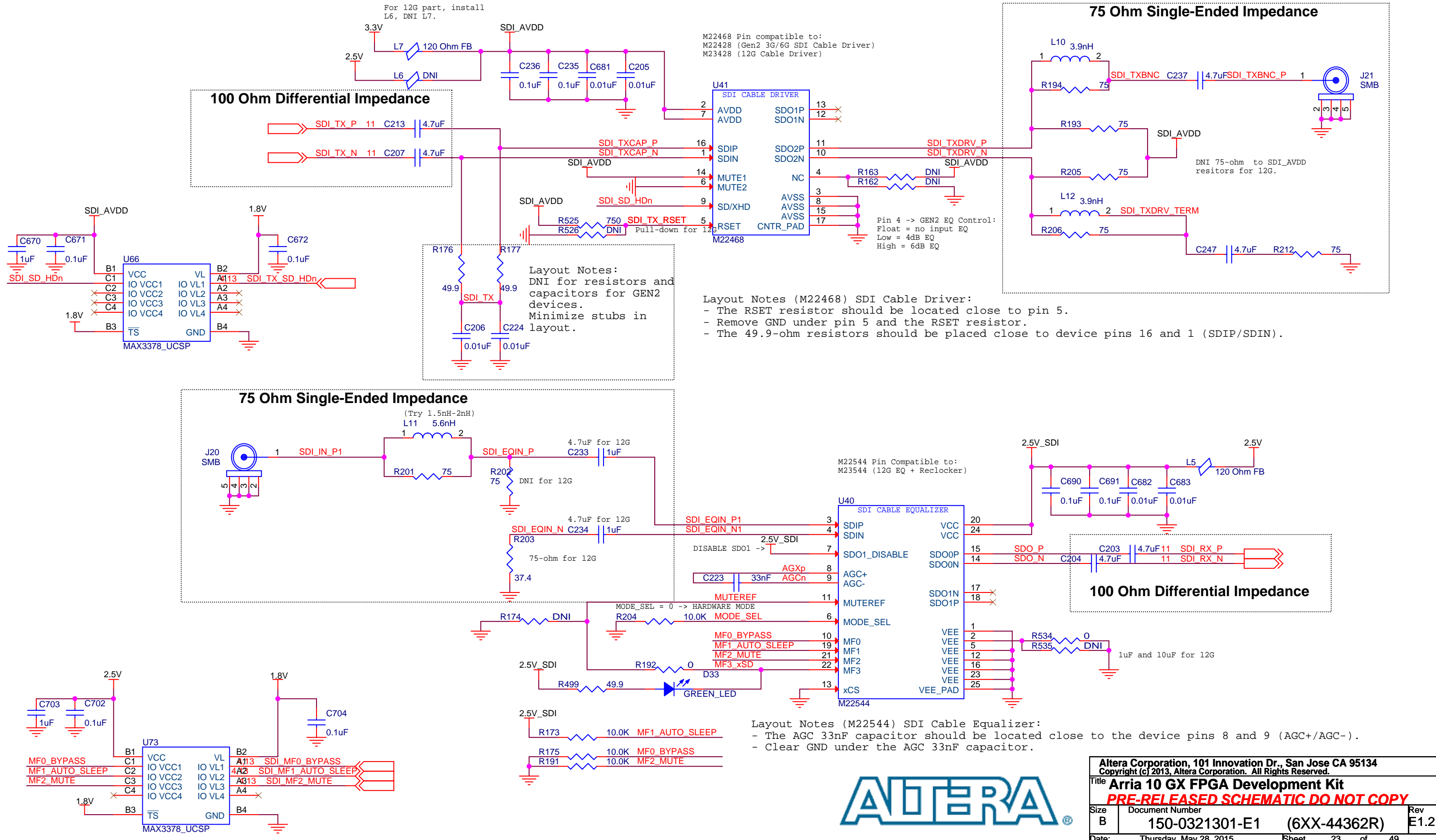
Level I power is < 1W (0.3 A)  
 Level II power is < 1.5W (0.45 A)  
 Level II Instantaneous peak current per rail 600mA



SFP modules have RS1 connected to GND.  
 If using SFP+ Rate Select pin are defined as:  
 RS1=0 -> TX datarates <= 4.25GB/s  
 RS1=1 -> TX datarates > 4.25GB/s  
 RS0=0 -> RX datarates <= 4.25GB/s  
 RS0=1 -> RX datarates > 4.25GB/s

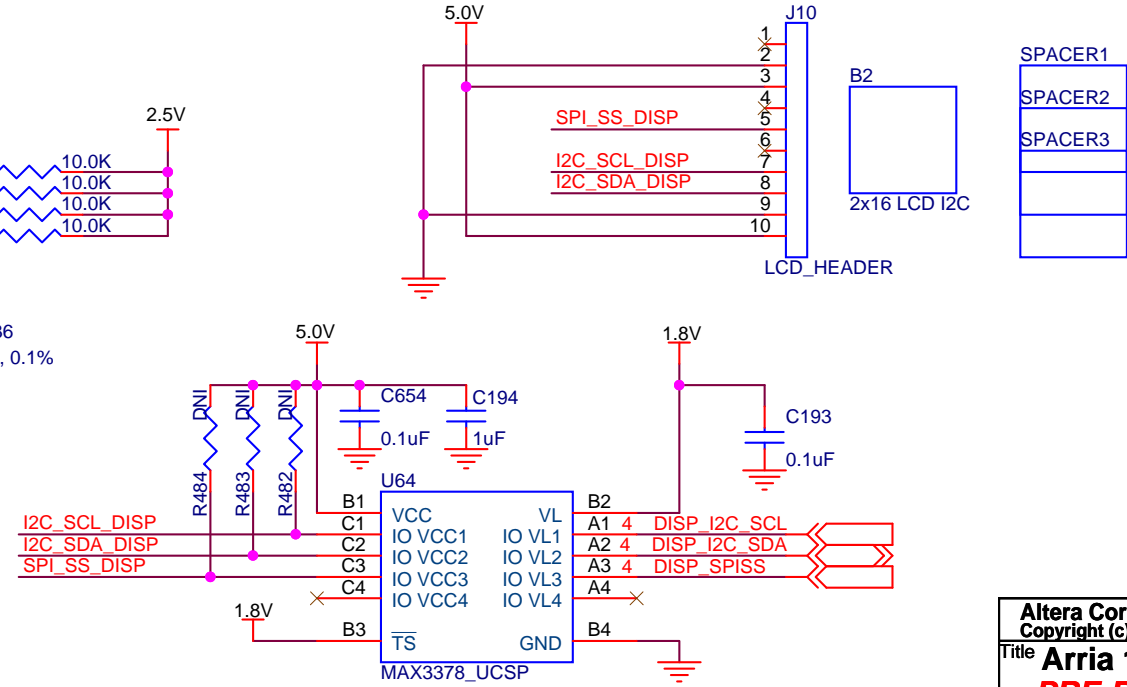
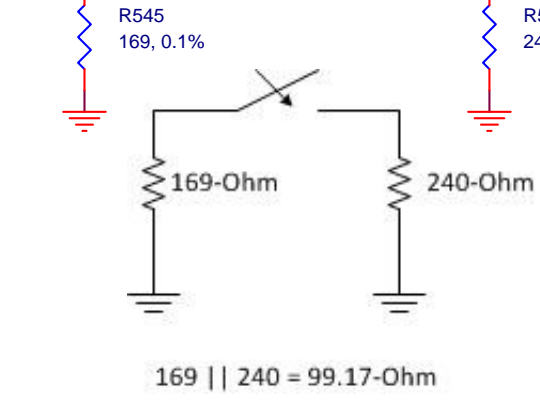
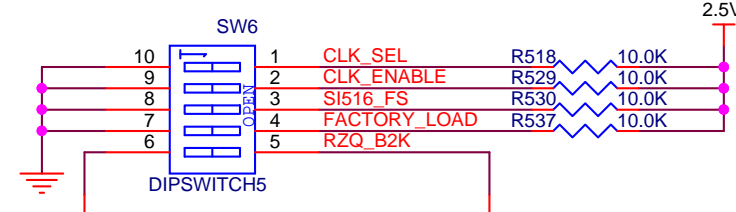
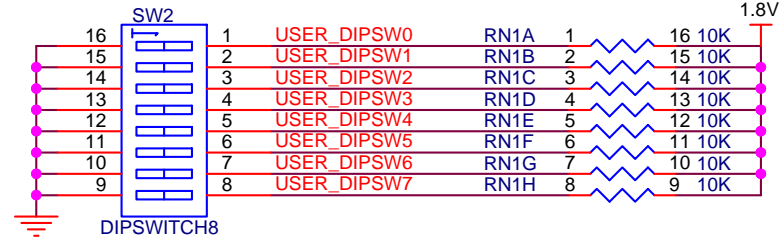
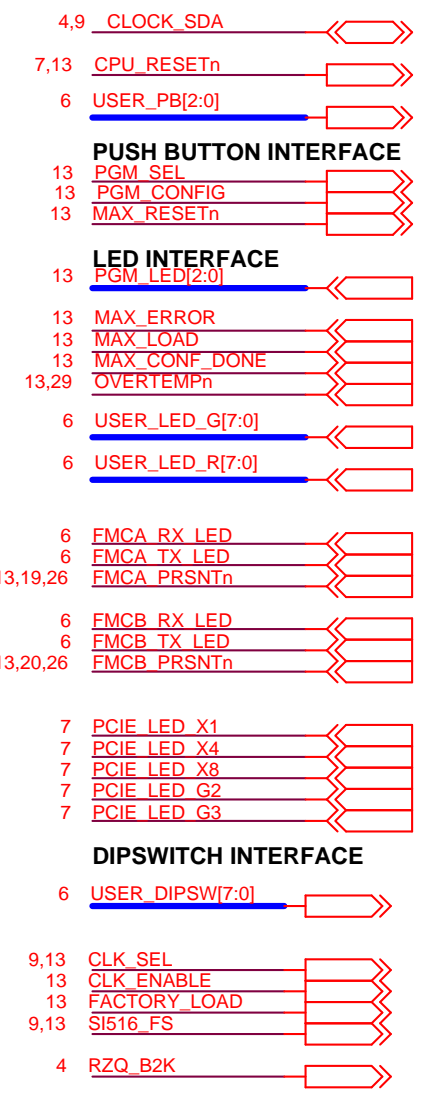
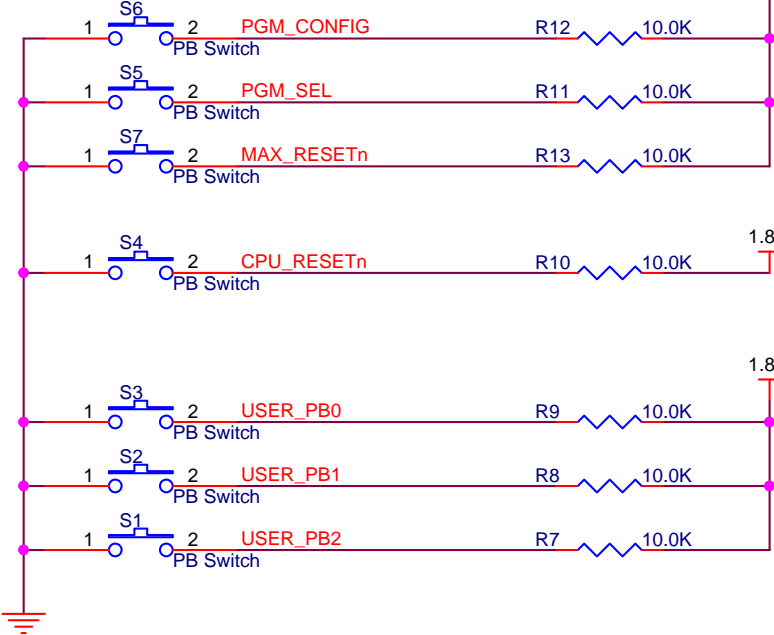
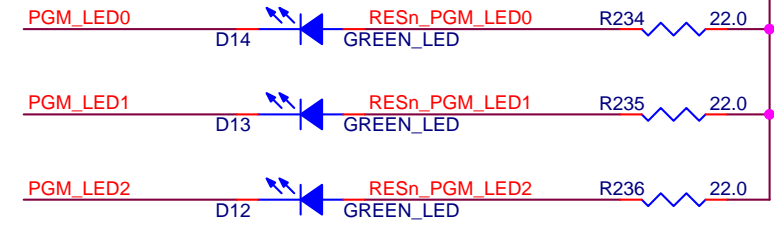
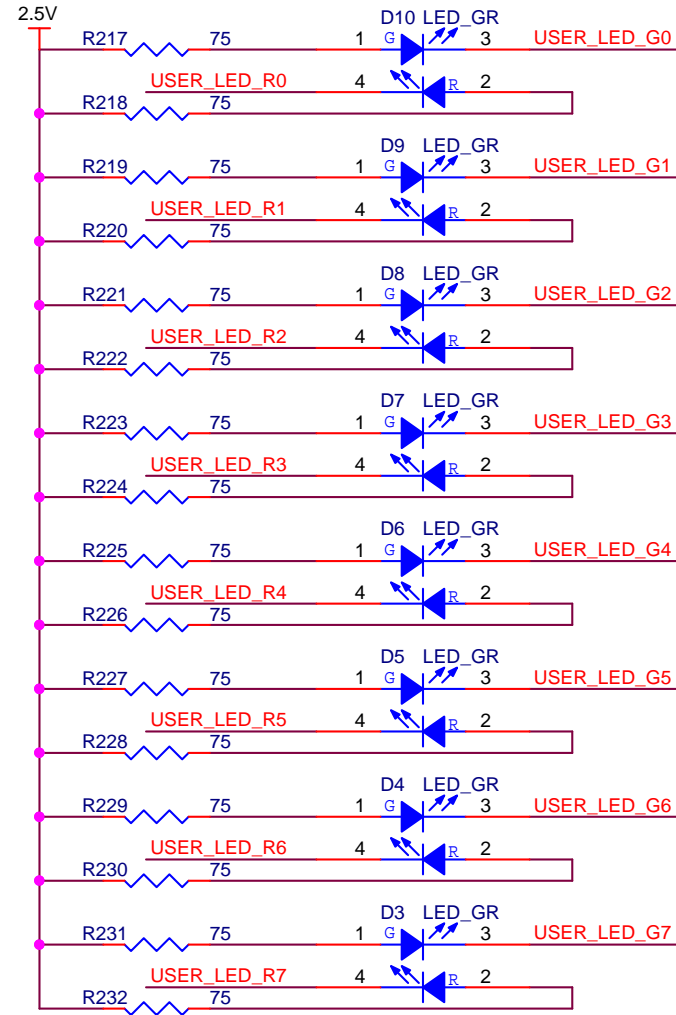
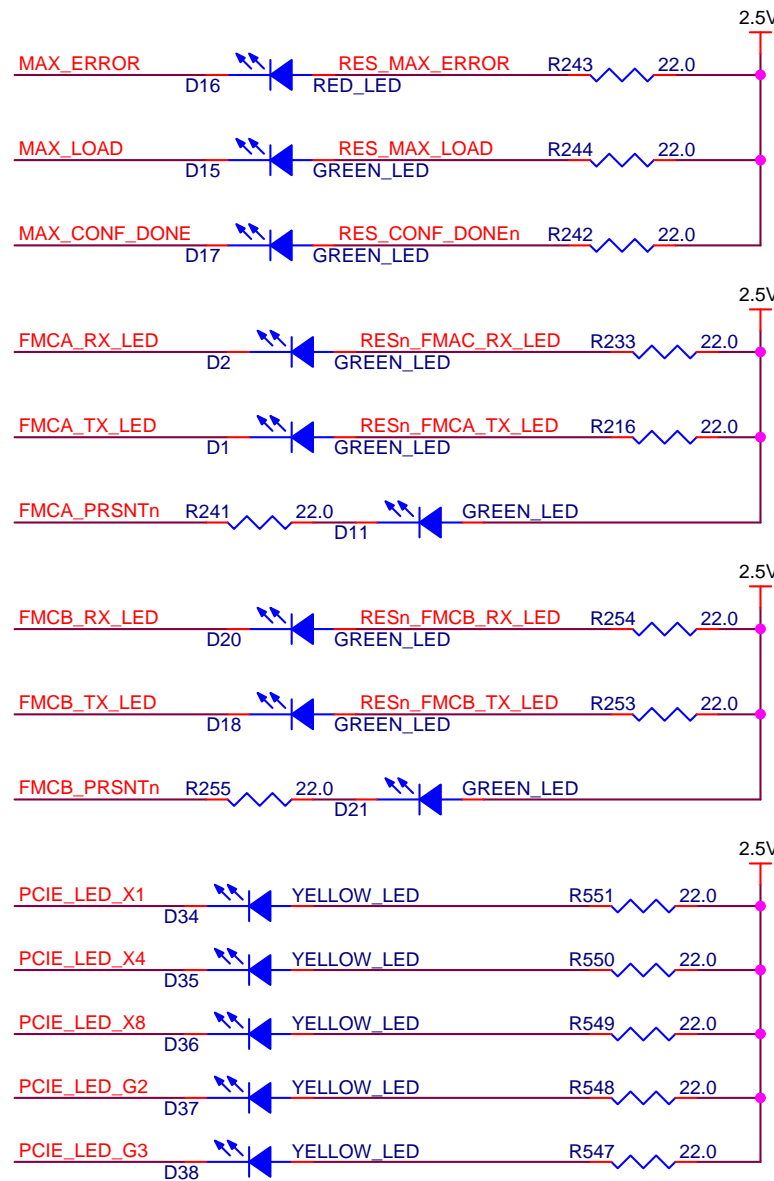


# SDI Cable Driver, Equalizer, and SMB

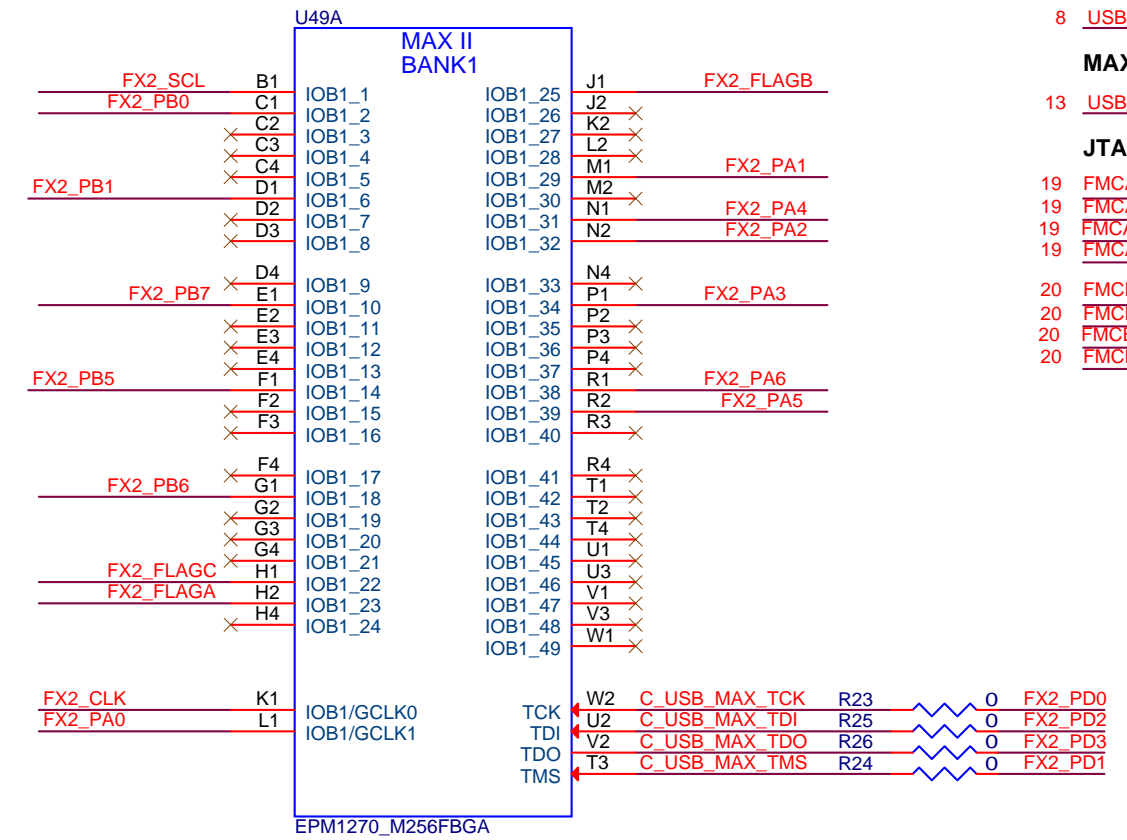
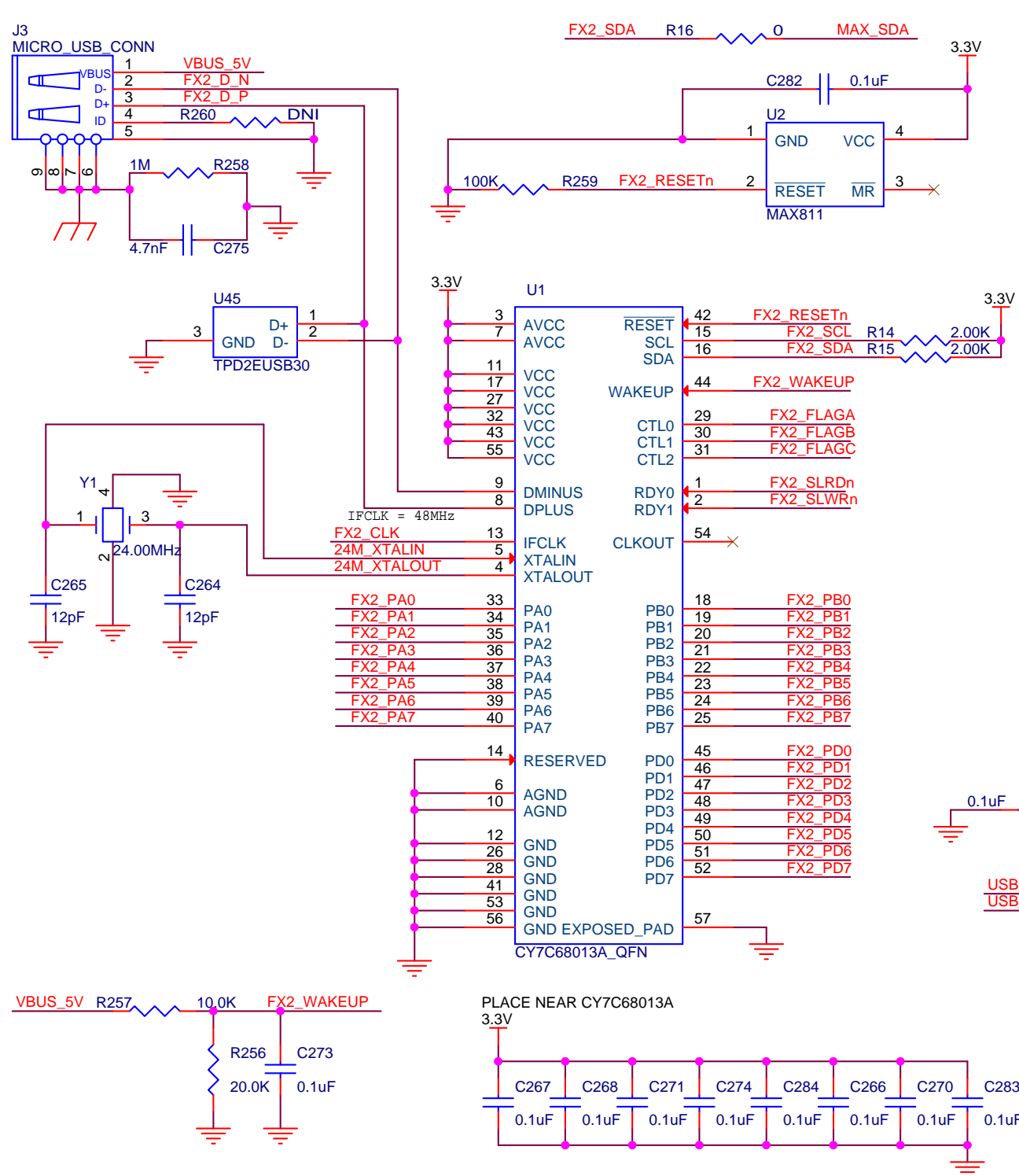




# User I/O

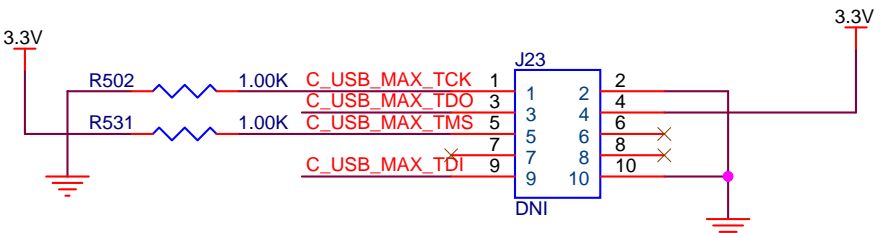
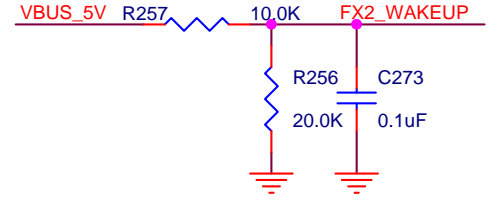
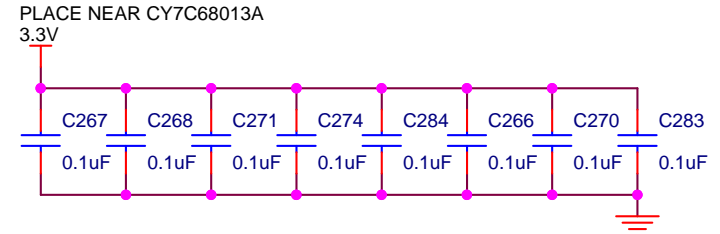
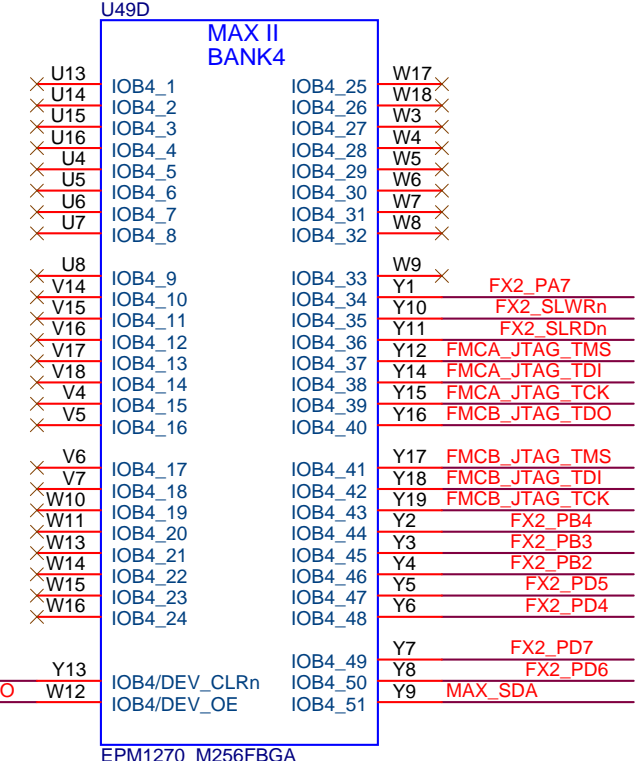
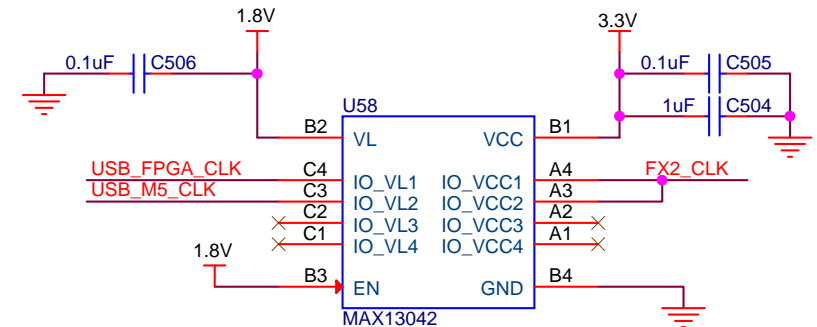


# On-Board USB Blaster II - Part 1

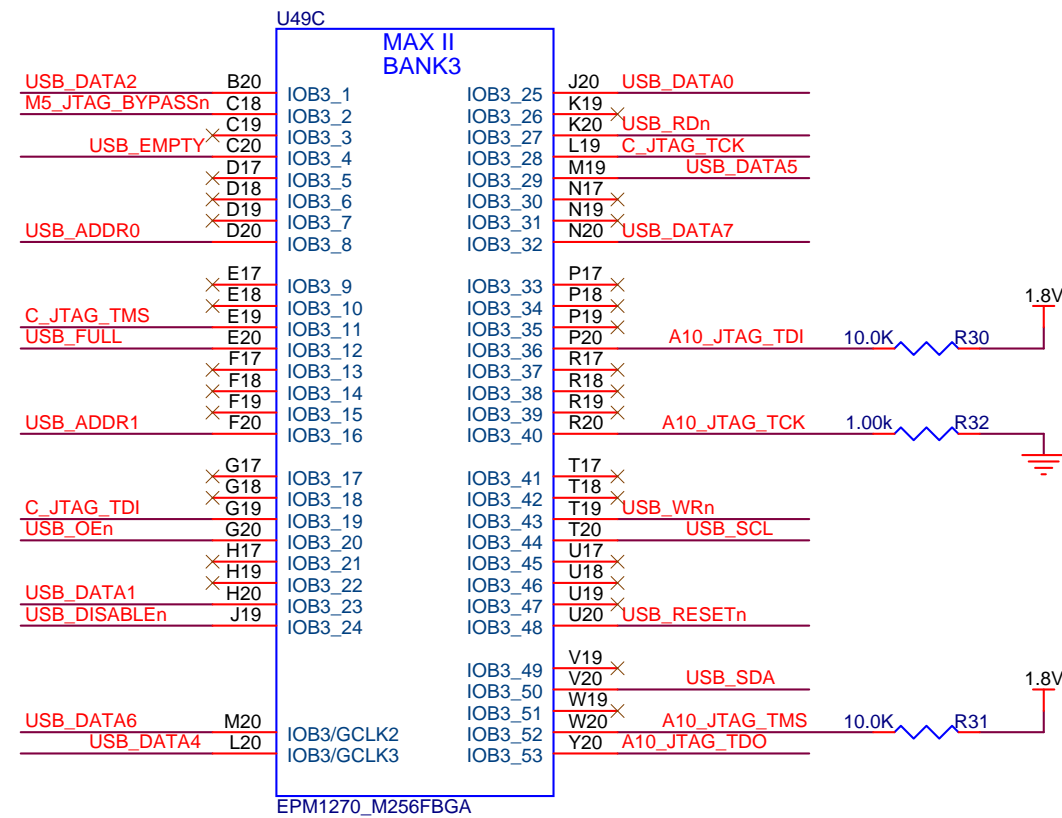
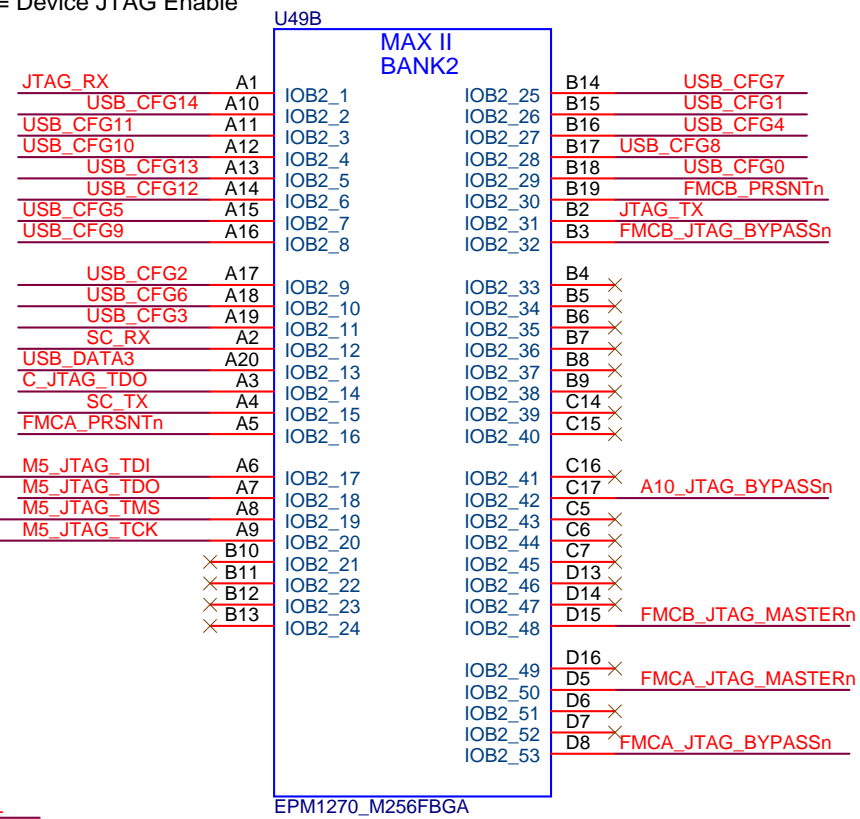
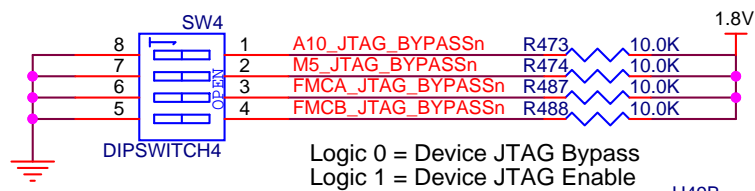


- ARRIA 10 USB INTERFACE**
- 8 USB\_FPGA\_CLK
- MAX V USB INTERFACE**
- 13 USB\_M5\_CLK
- JTAG INTERFACE**
- 19 FMCA\_JTAG\_TCK
- 19 FMCA\_JTAG\_TMS
- 19 FMCA\_JTAG\_TDO
- 19 FMCA\_JTAG\_TDI
- 20 FMCB\_JTAG\_TCK
- 20 FMCB\_JTAG\_TMS
- 20 FMCB\_JTAG\_TDO
- 20 FMCB\_JTAG\_TDI

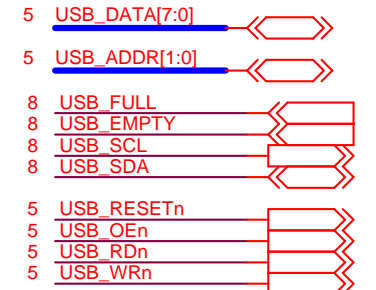
CAN WE USE MAX II TO LEVEL TRANSLATE USB\_CLK?



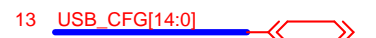
# On-Board USB Blaster II - Part 2



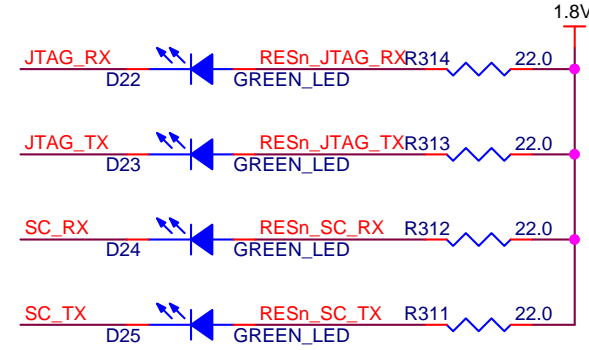
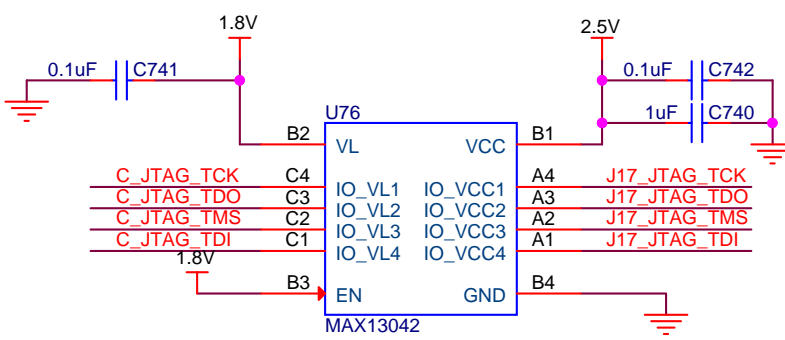
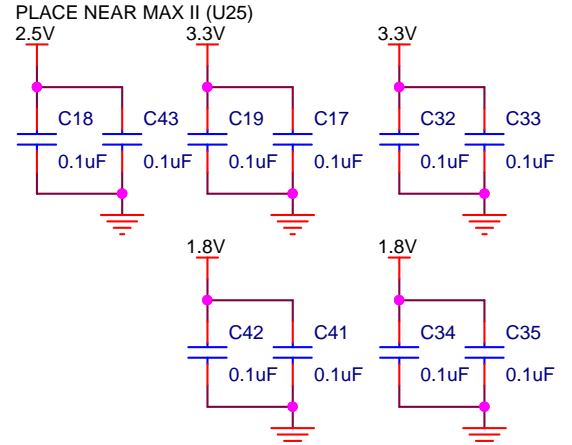
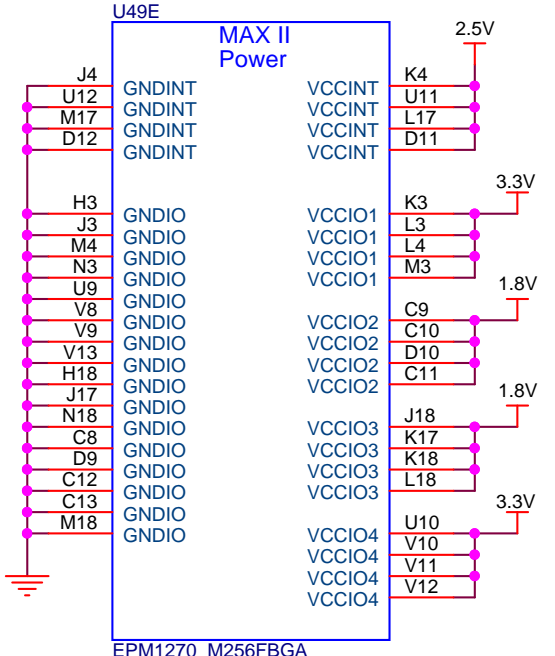
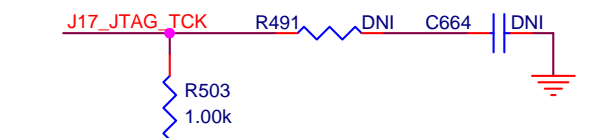
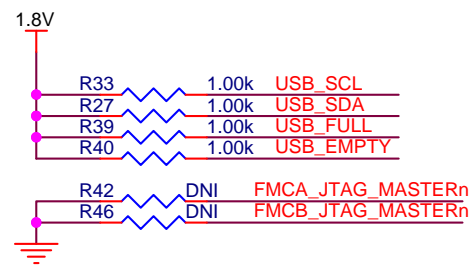
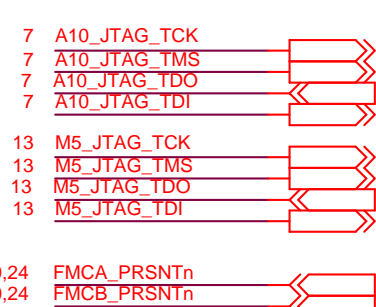
## ARRIA 10 USB INTERFACE



## MAX V USB INTERFACE

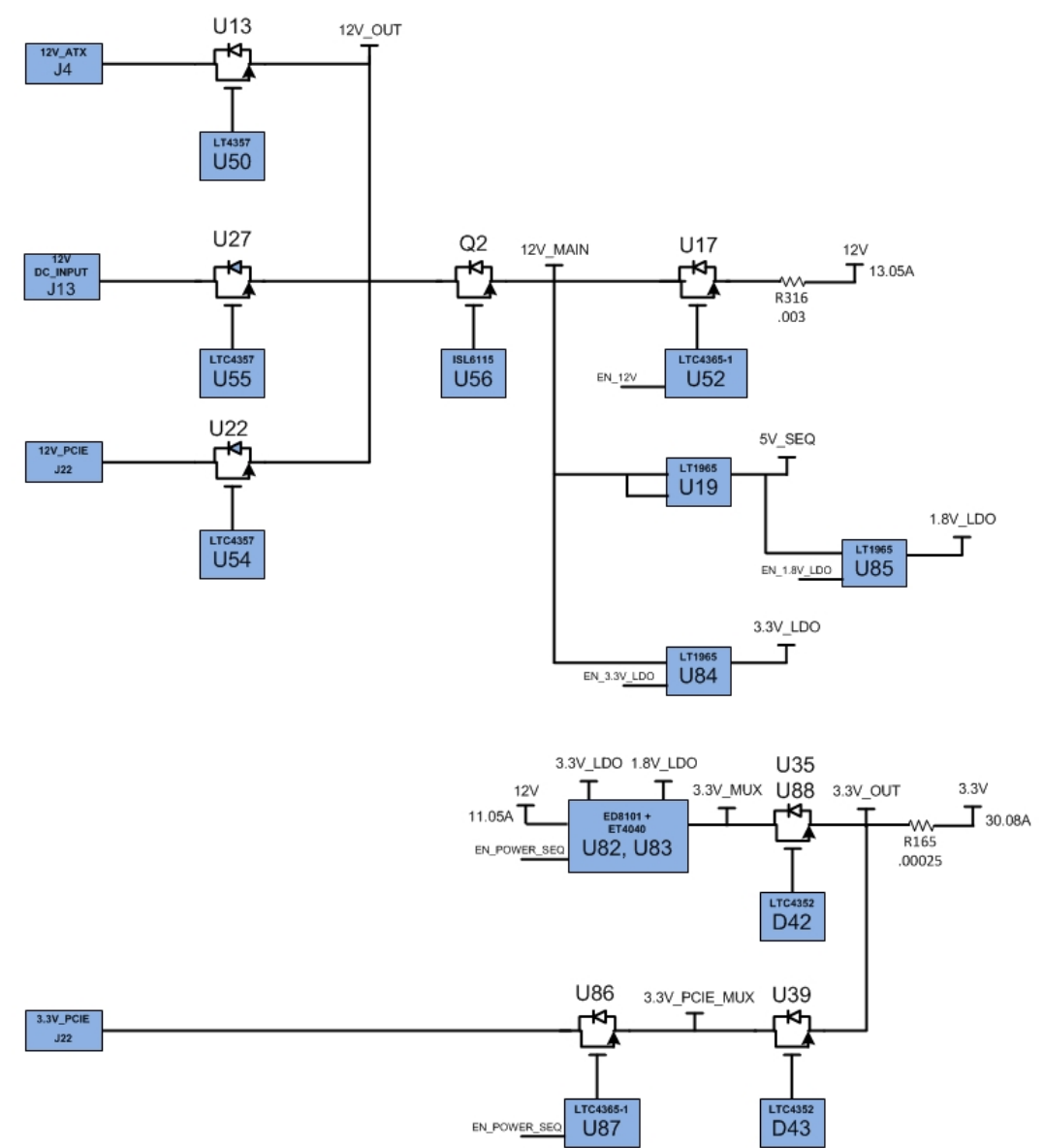


## JTAG INTERFACE





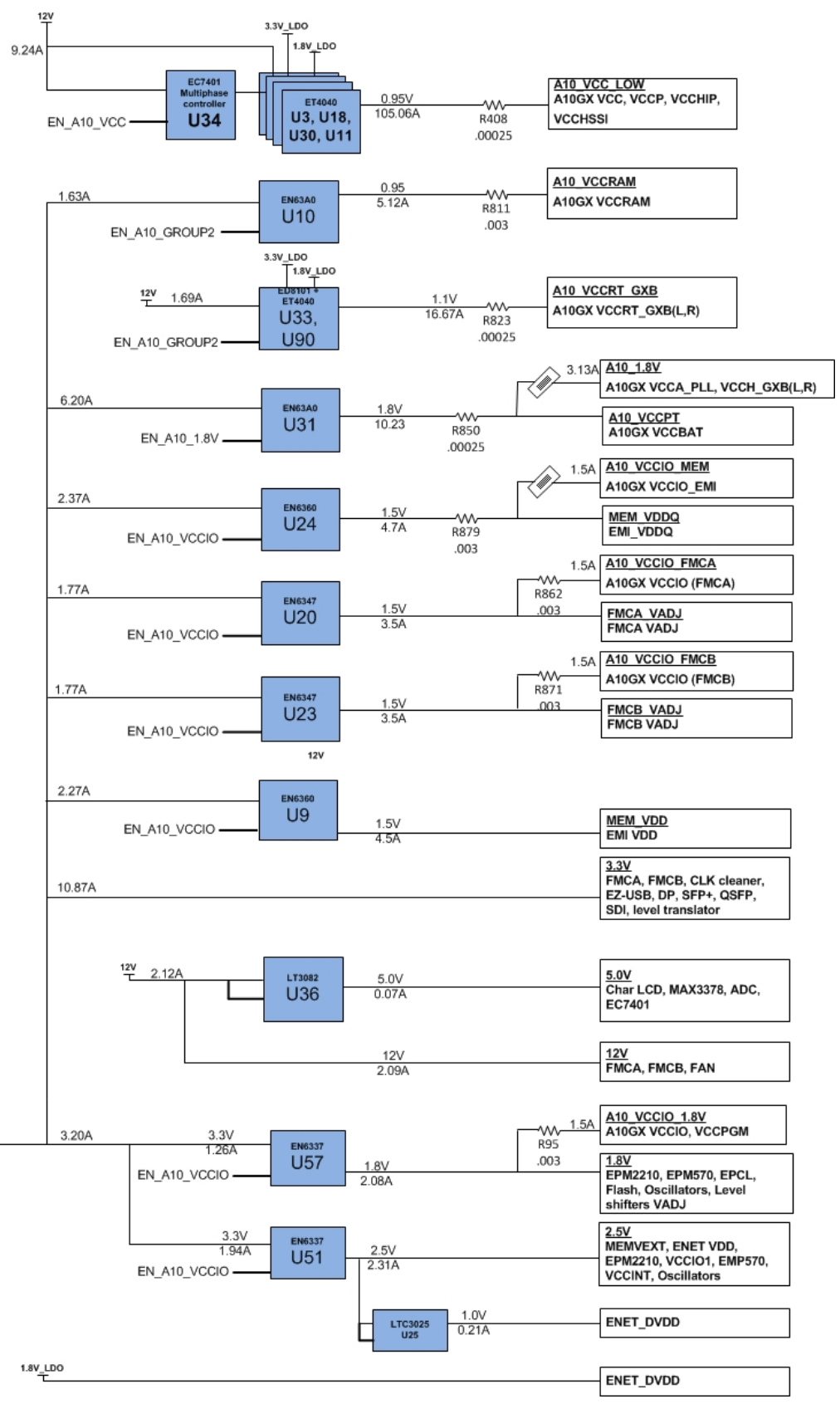
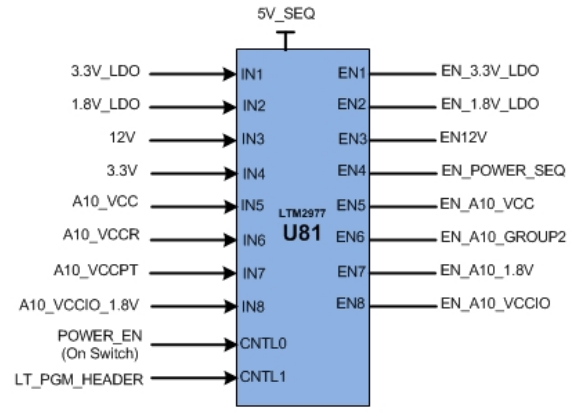
# Power Tree



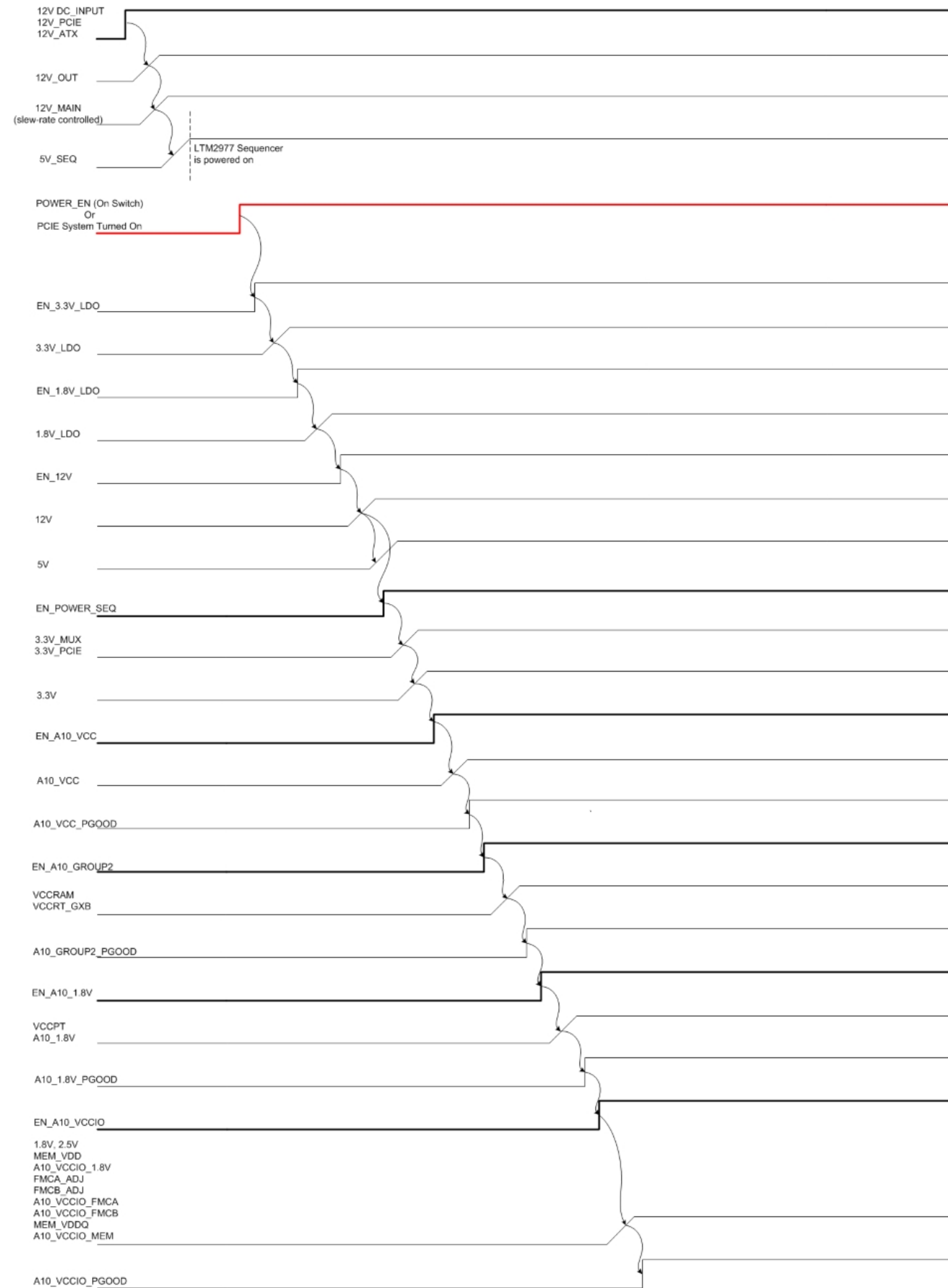
- Power UP Sequencing:
- 1) EN\_3.3V\_LDO
  - 2) EN\_1.8V\_LDO
  - 3) EN\_12V
  - 4) EN\_POWER\_SEQ
  - 5) EN\_A10\_VCC
  - 6) EN\_A10\_GROUP2
  - 7) EN\_A10\_1.8V
  - 8) EN\_A10\_VCCIO

- Power DOWN Sequencing:
- 1) DISABLE A10\_VCCIO
  - 2) DISABLE A10\_1.8V
  - 3) DISABLE A10\_GROUP2
  - 4) DISABLE A10\_VCC
  - 5) DISABLE POWER\_SEQ
  - 6) DISABLE 12V
  - 7) DISABLE 1.8V\_LDO
  - 8) DISABLE 3.3V\_LDO

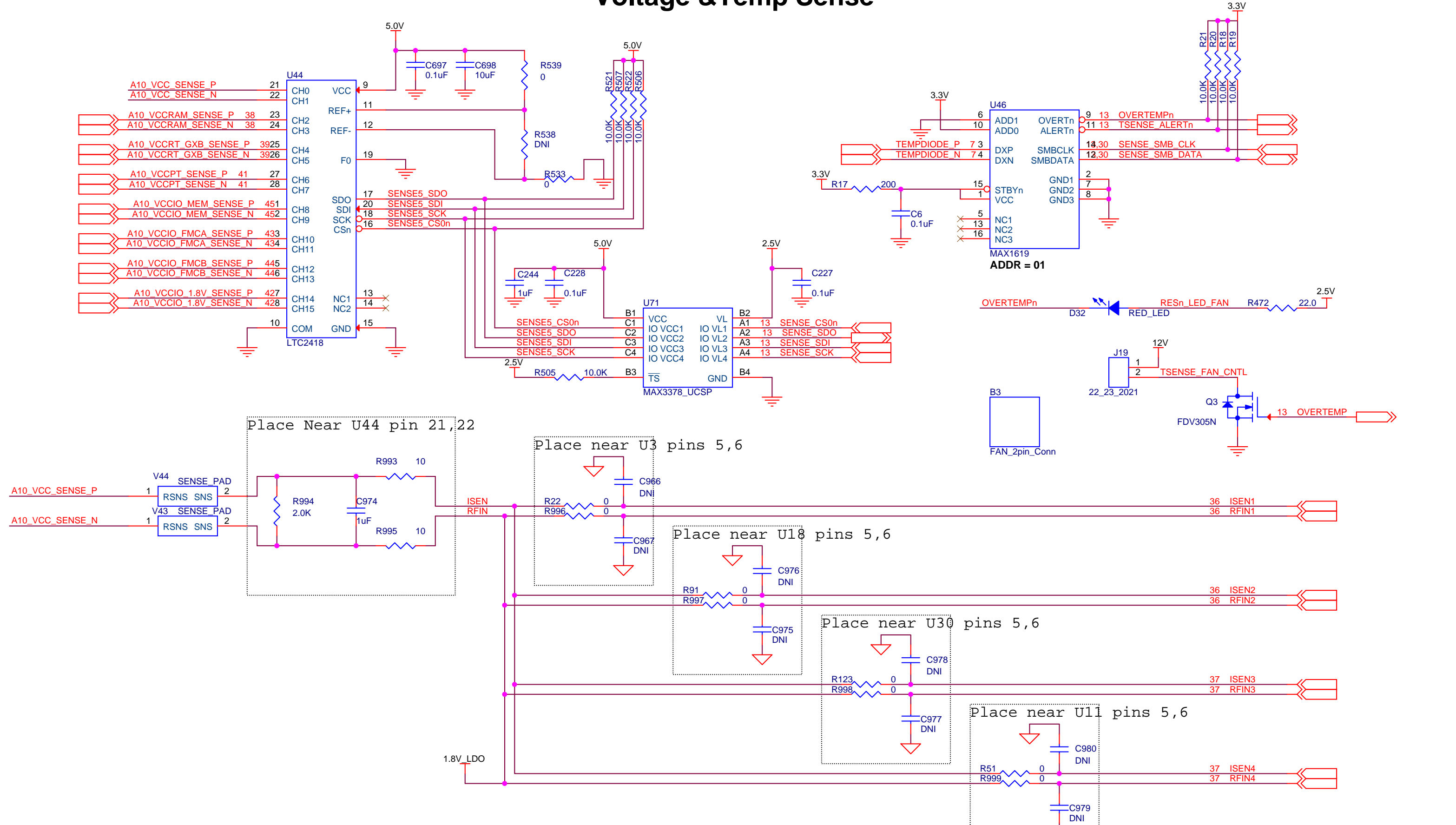
PCIe Component Height Restrictions:  
 -Top Side (Max): 14.47mm  
 -Bottom Side (Max) 2.67mm



Power-On Sequencing  
(Power-Off is reverse of Power-On)



# Voltage & Temp Sense



Place Near U44 pin 21,22

Place near U3 pins 5,6

Place near U18 pins 5,6

Place near U30 pins 5,6

Place near U11 pins 5,6

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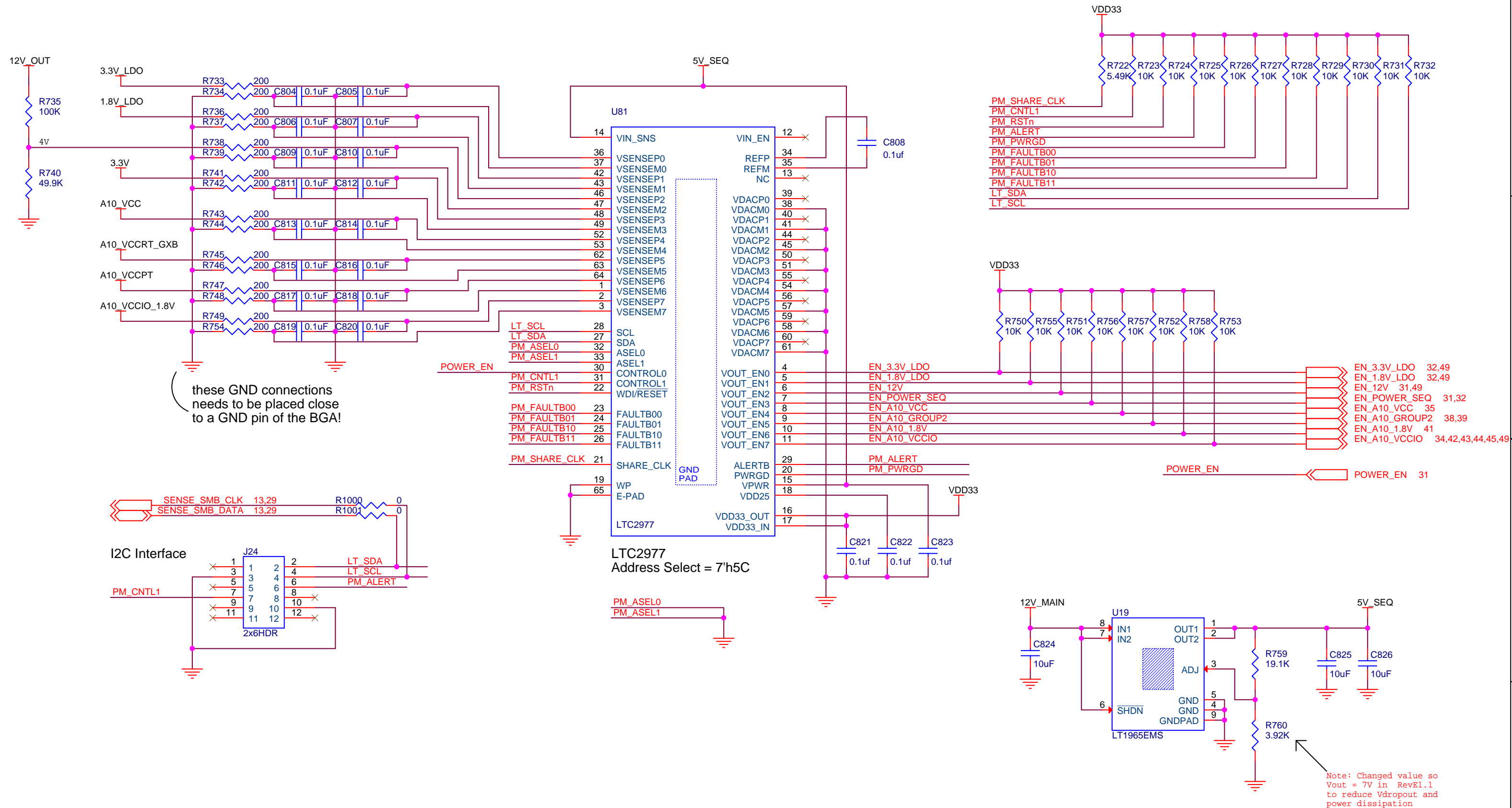
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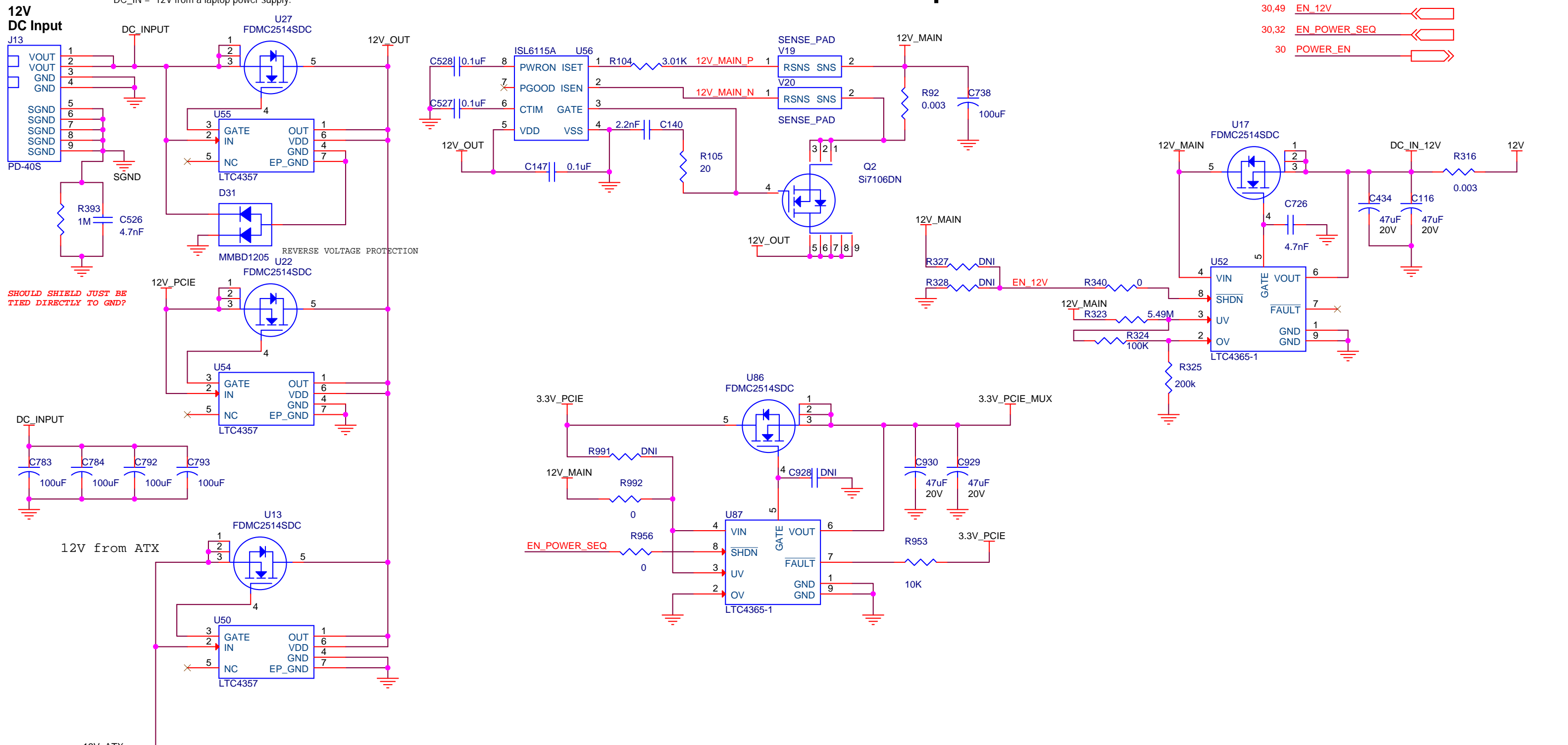




# Power Sequence Controller



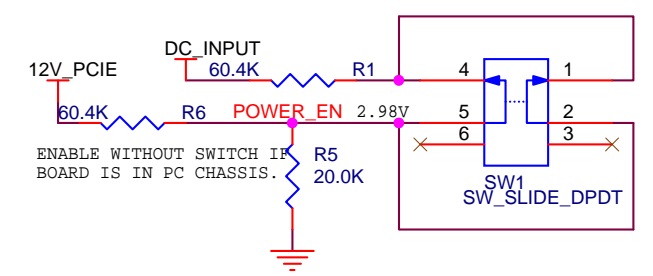
# Power - Select Power Input



- 30,49 EN\_12V
- 30,32 EN\_POWER\_SEQ
- 30 POWER\_EN

SHOULD SHIELD JUST BE TIED DIRECTLY TO GND?

## Power On Switch



Sense0 = GND  
Sense1 = GND  
A 2 x 4 auxiliary power connector is plugged into the card. The card can draw up to 150 W from the auxiliary power connector.

DC_IN -> 12V (Laptop Supply)	12V_PCIE ATX (2x4 ATX)	DC_IN_ATX (Voltage Selected by LTC4357)
12V	12V	12V from 12V_ATX_IN
12V	0V	12V from DC_IN->12V
0V	12V	12V from 12V_ATX_IN

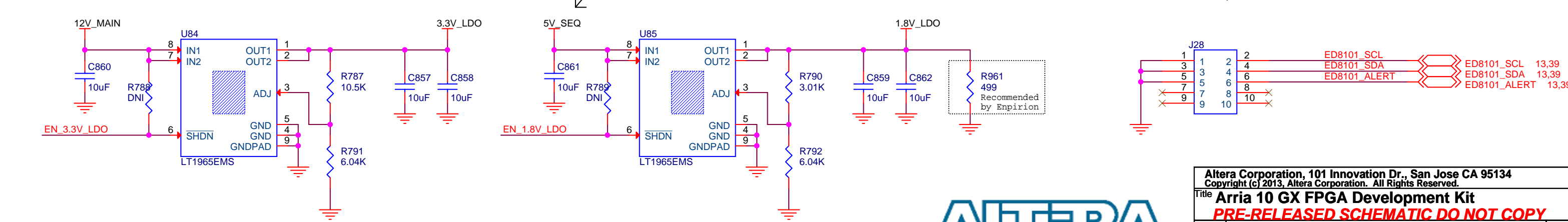
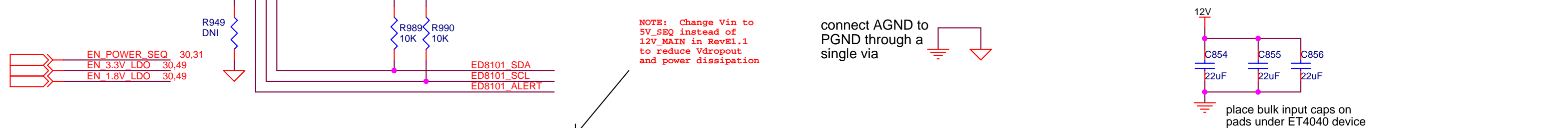
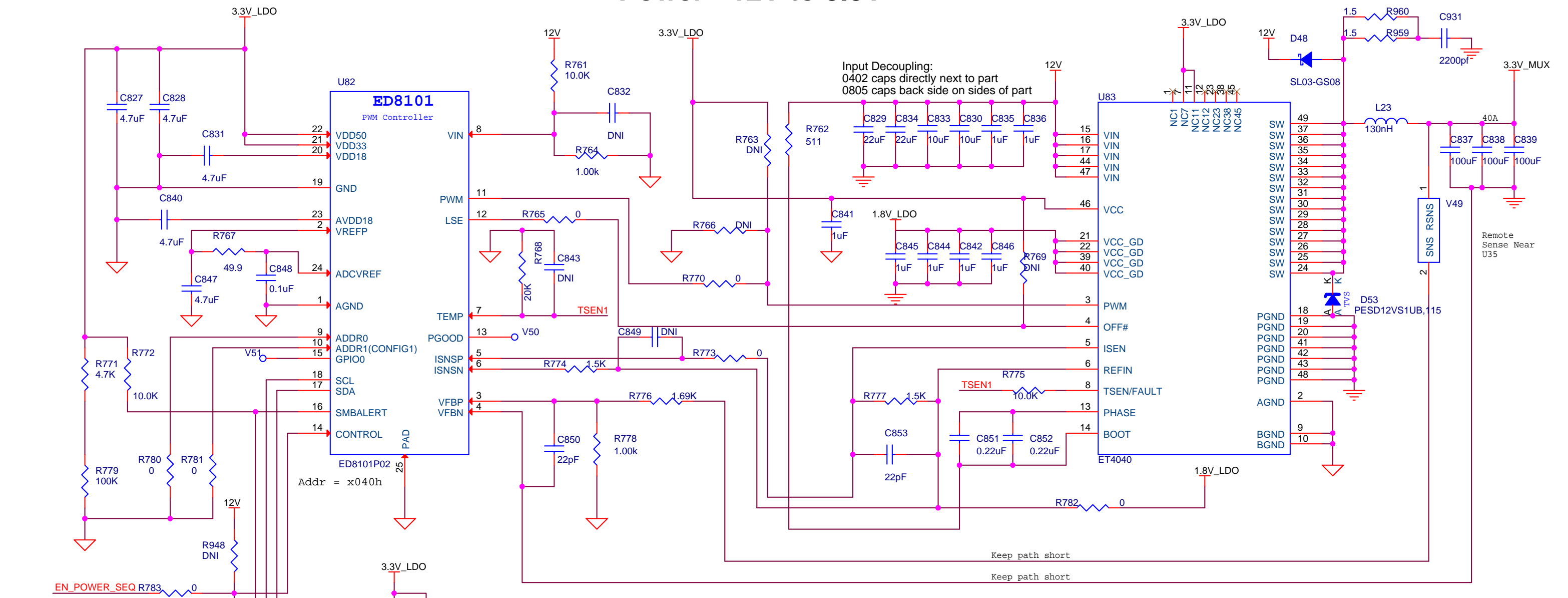
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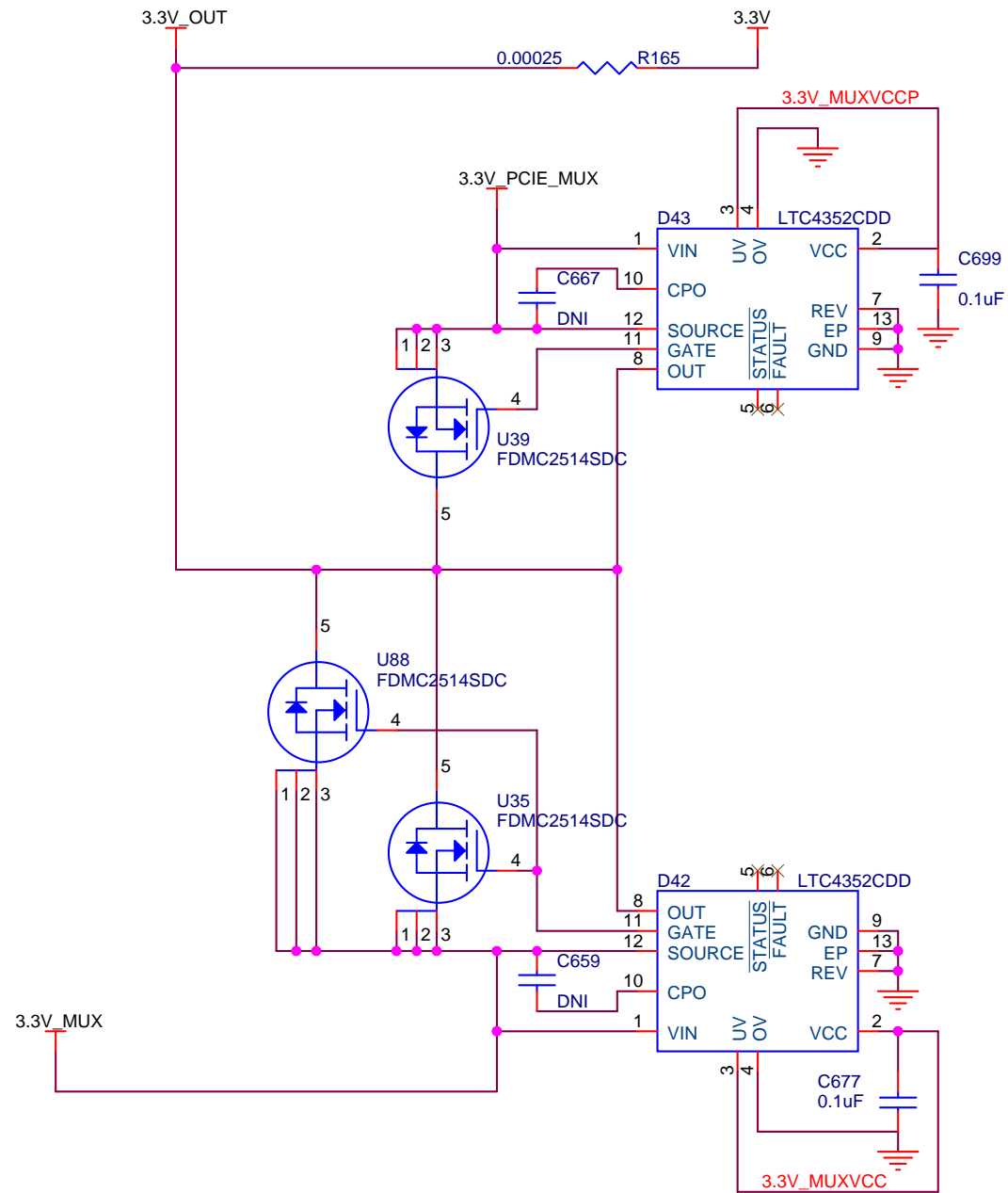
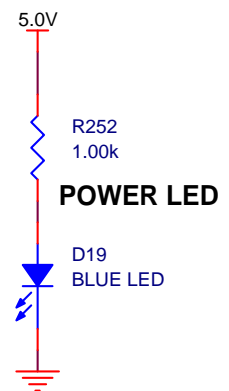
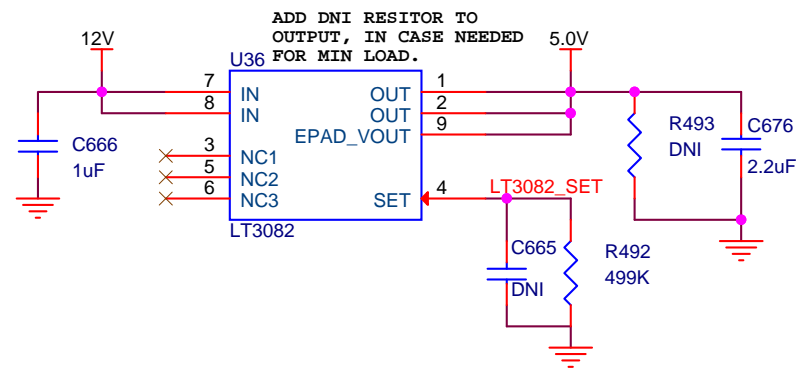


# Power - 12V to 3.3V



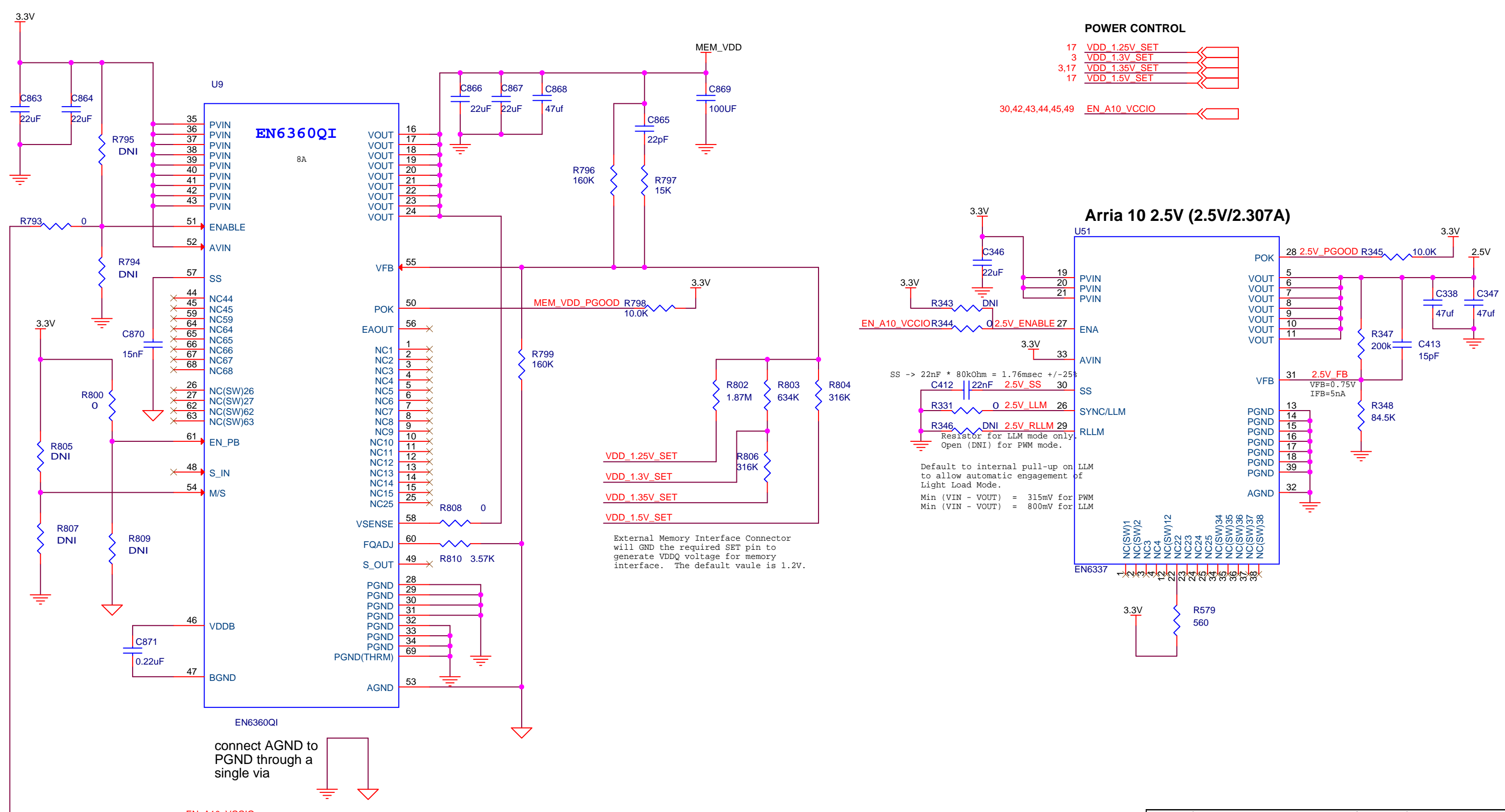


# Power 1 - DC Input to 3.3V Output

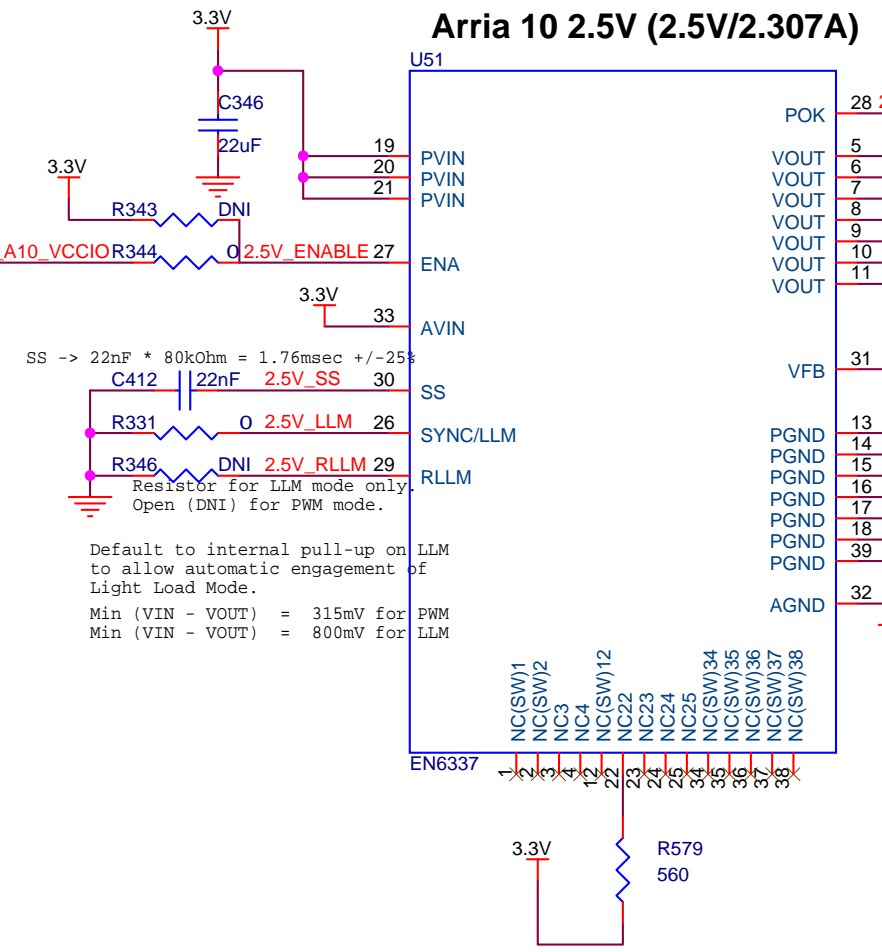


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# Power - MEM\_VDD, 2.5V



- POWER CONTROL**
- 17 VDD\_1.25V\_SET
  - 3 VDD\_1.3V\_SET
  - 3,17 VDD\_1.35V\_SET
  - 17 VDD\_1.5V\_SET
  - 30,42,43,44,45,49 EN\_A10\_VCCIO



VDD\_1.25V\_SET

VDD\_1.3V\_SET

VDD\_1.35V\_SET

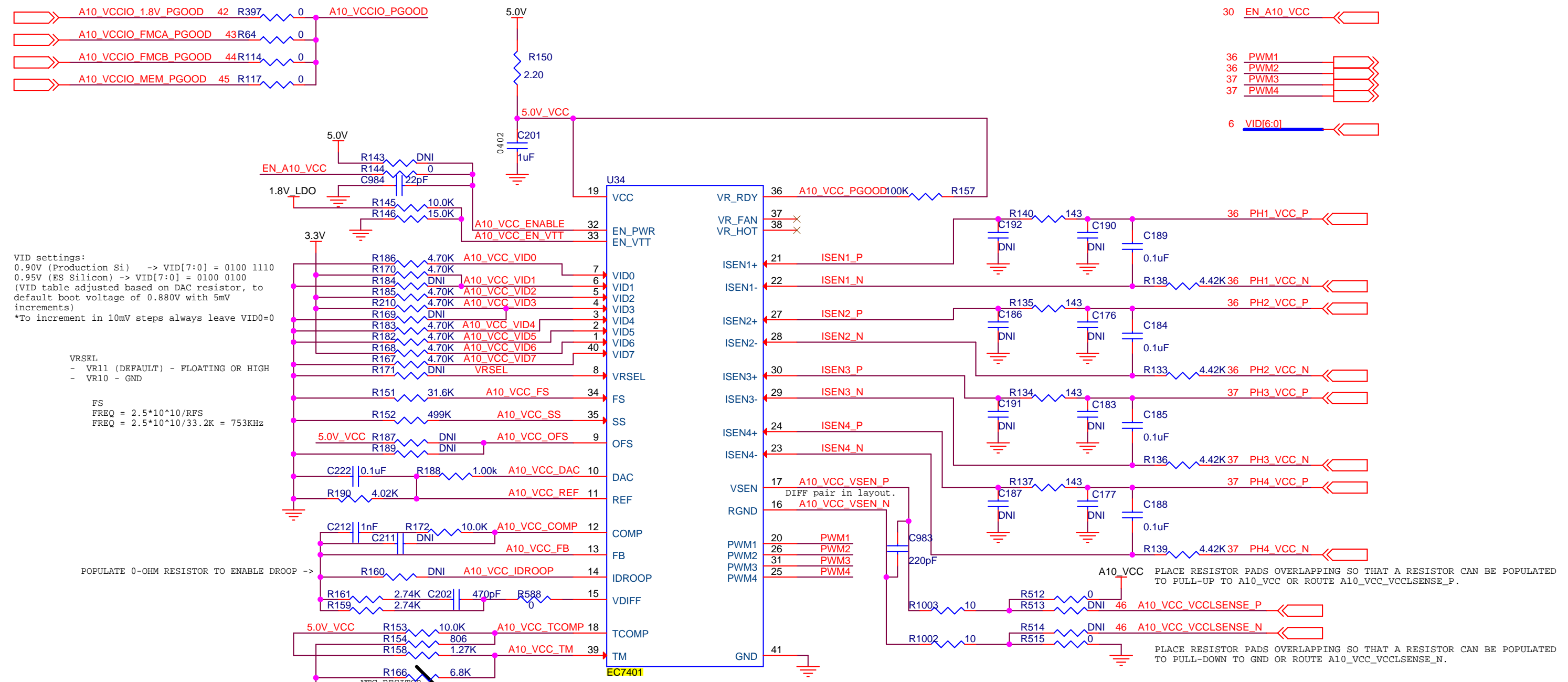
VDD\_1.5V\_SET

External Memory Interface Connector will GND the required SET pin to generate VDDQ voltage for memory interface. The default value is 1.2V.

connect AGND to PGND through a single via



# Power - A10 VCC



VID settings:  
 0.90V (Production Si) -> VID[7:0] = 0100 1110  
 0.95V (ES Silicon) -> VID[7:0] = 0100 0100  
 (VID table adjusted based on DAC resistor, to default boot voltage of 0.880V with 5mV increments)  
 \*To increment in 10mV steps always leave VID0=0

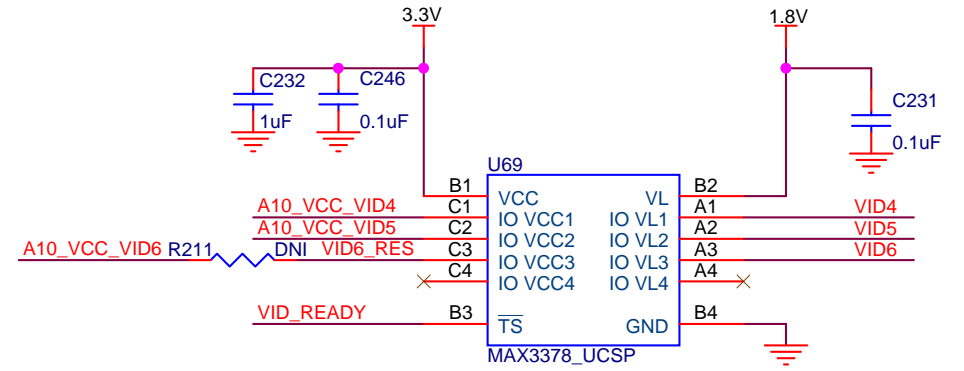
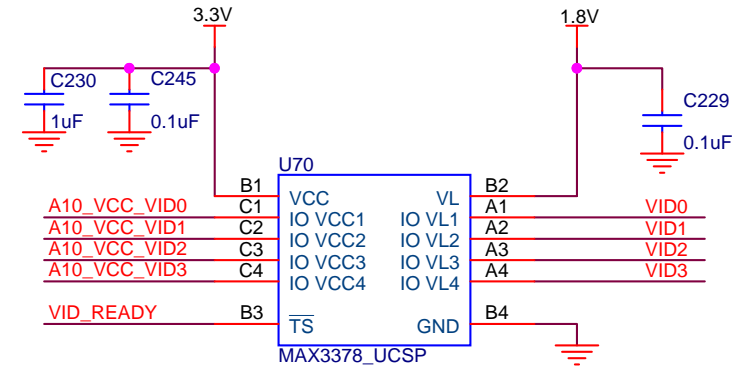
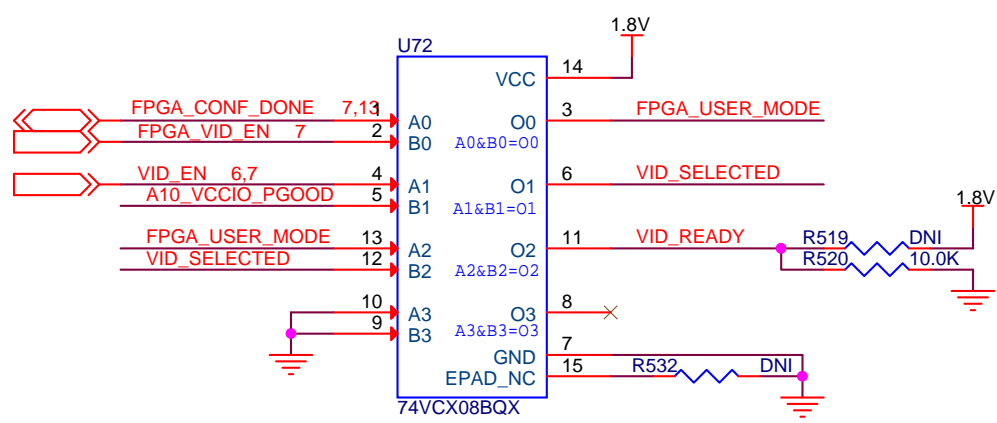
VRSEL  
 - VR11 (DEFAULT) - FLOATING OR HIGH  
 - VR10 - GND

FS  
 FREQ = 2.5\*10<sup>10</sup>/RFS  
 FREQ = 2.5\*10<sup>10</sup>/33.2K = 753KHz

POPULATE 0-OHM RESISTOR TO ENABLE DROOP ->

PLACE RESISTOR PADS OVERLAPPING SO THAT A RESISTOR CAN BE POPULATED TO PULL-UP TO A10\_VCC OR ROUTE A10\_VCC\_VCCLSSENSE\_P.

PLACE RESISTOR PADS OVERLAPPING SO THAT A RESISTOR CAN BE POPULATED TO PULL-DOWN TO GND OR ROUTE A10\_VCC\_VCCLSSENSE\_N.



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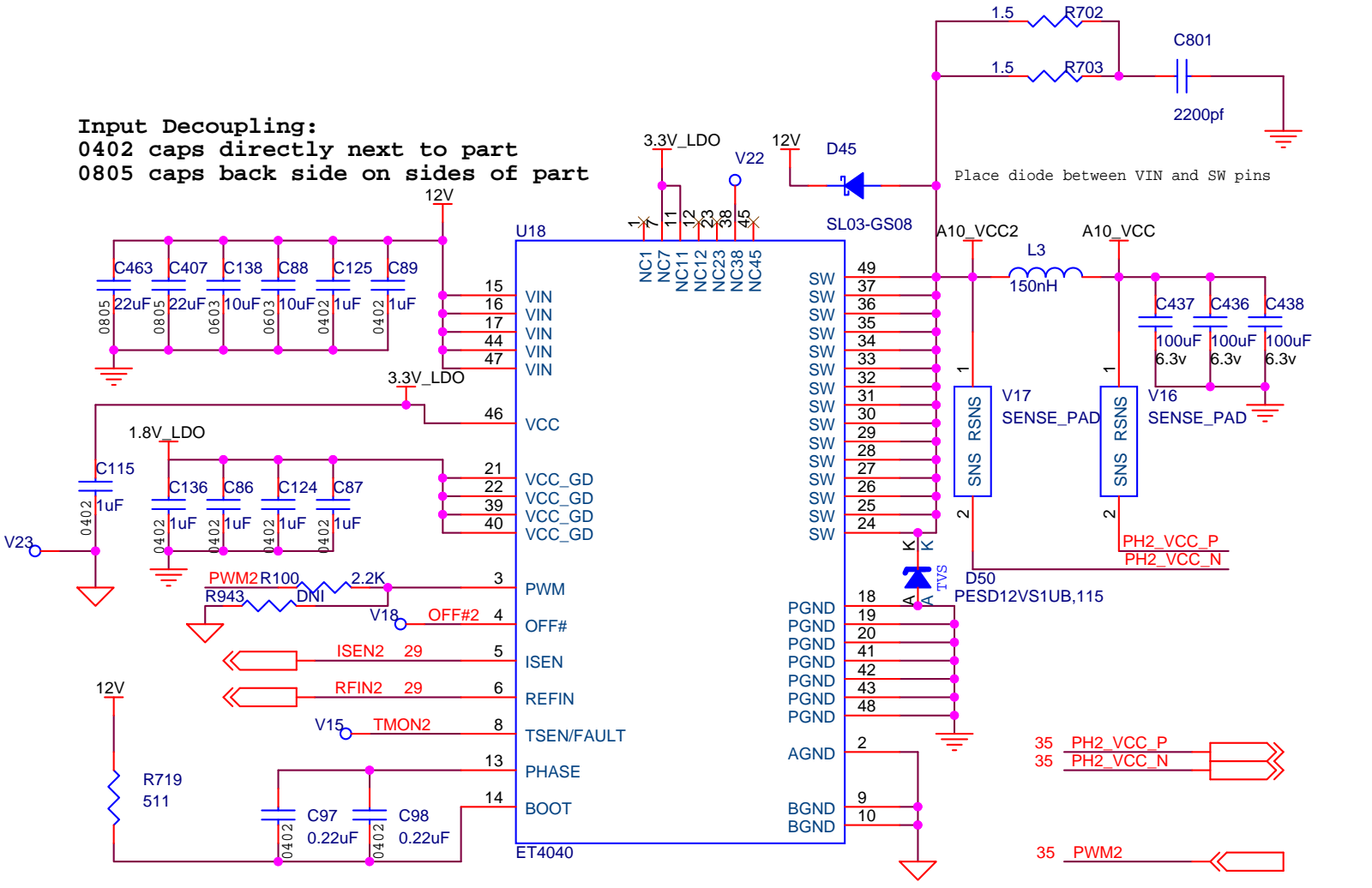
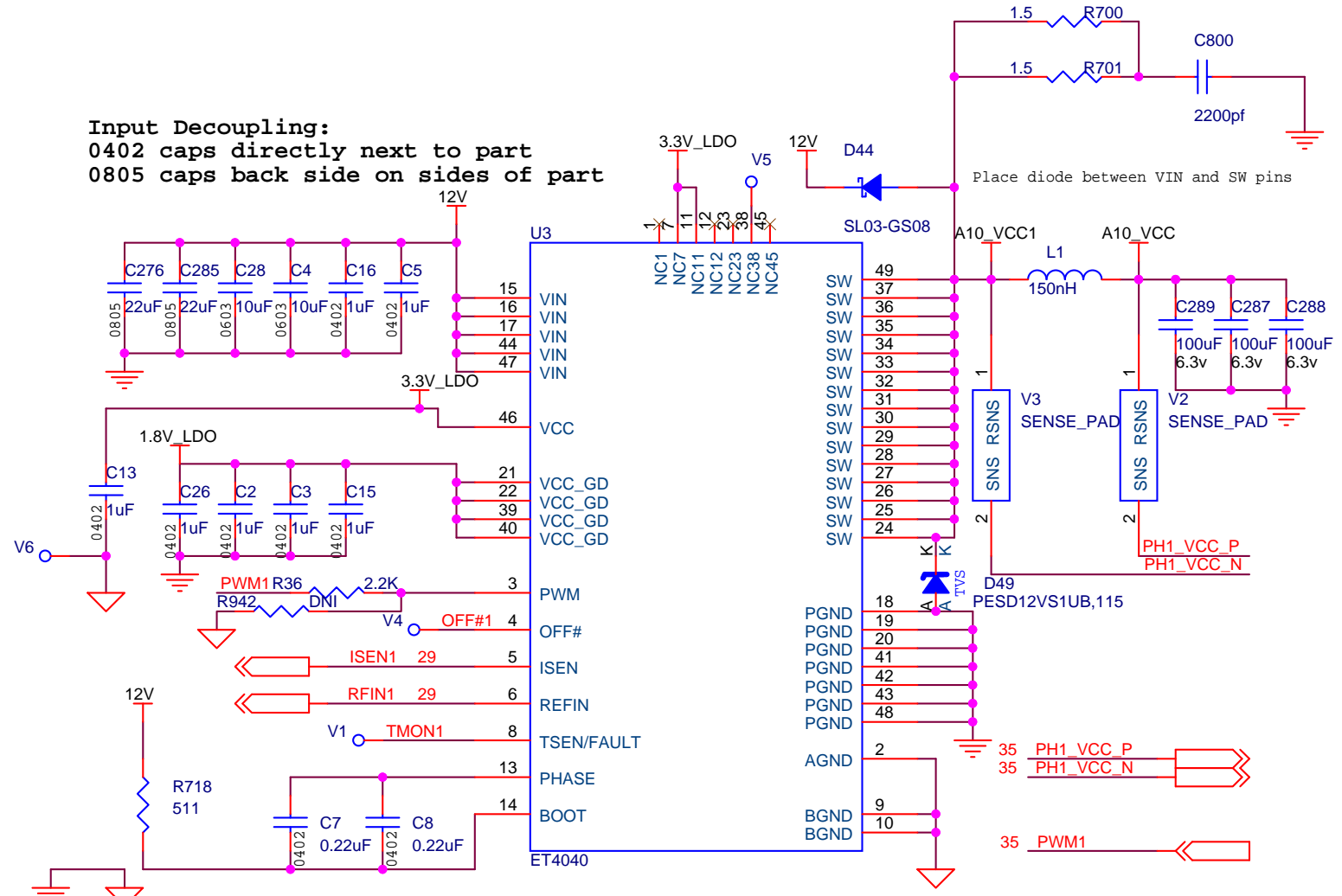
# Power1 A10VCC ET4040 (1)

PHASE 1

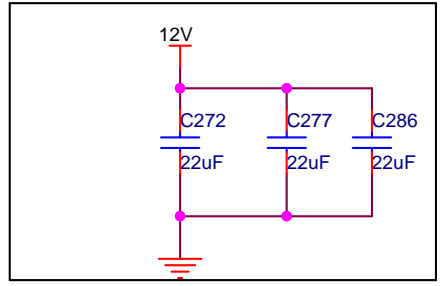
PHASE 2

**Input Decoupling:**  
0402 caps directly next to part  
0805 caps back side on sides of part

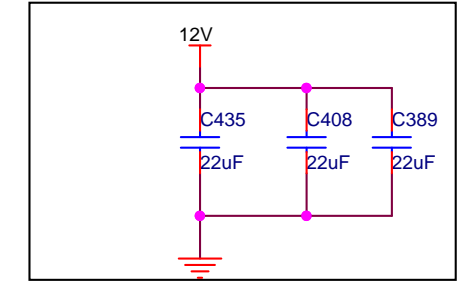
**Input Decoupling:**  
0402 caps directly next to part  
0805 caps back side on sides of part



Input caps on part pads directly under part



Input caps on part pads directly under part

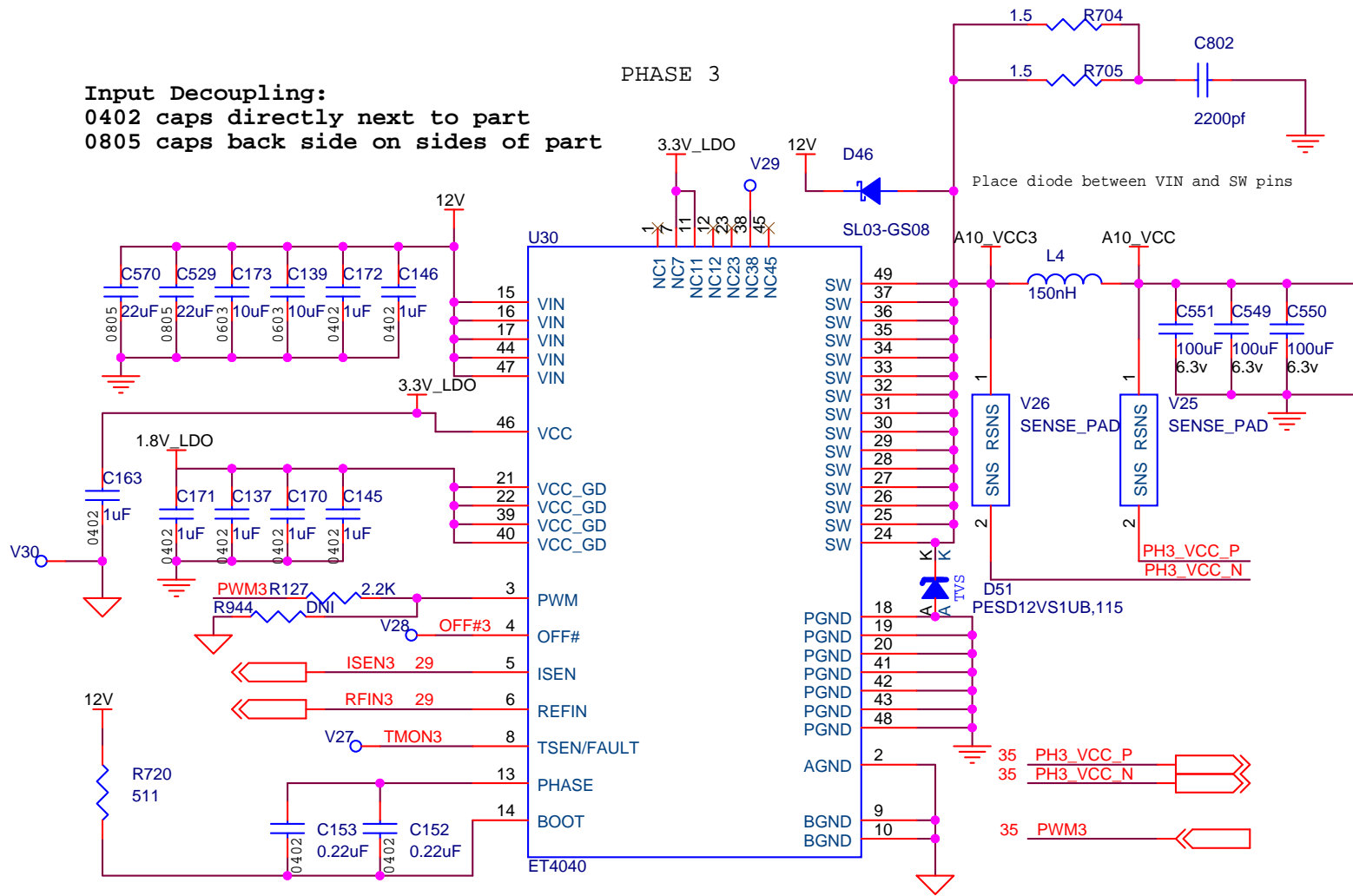


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# Power1 A10 VCC ET4040 (2)

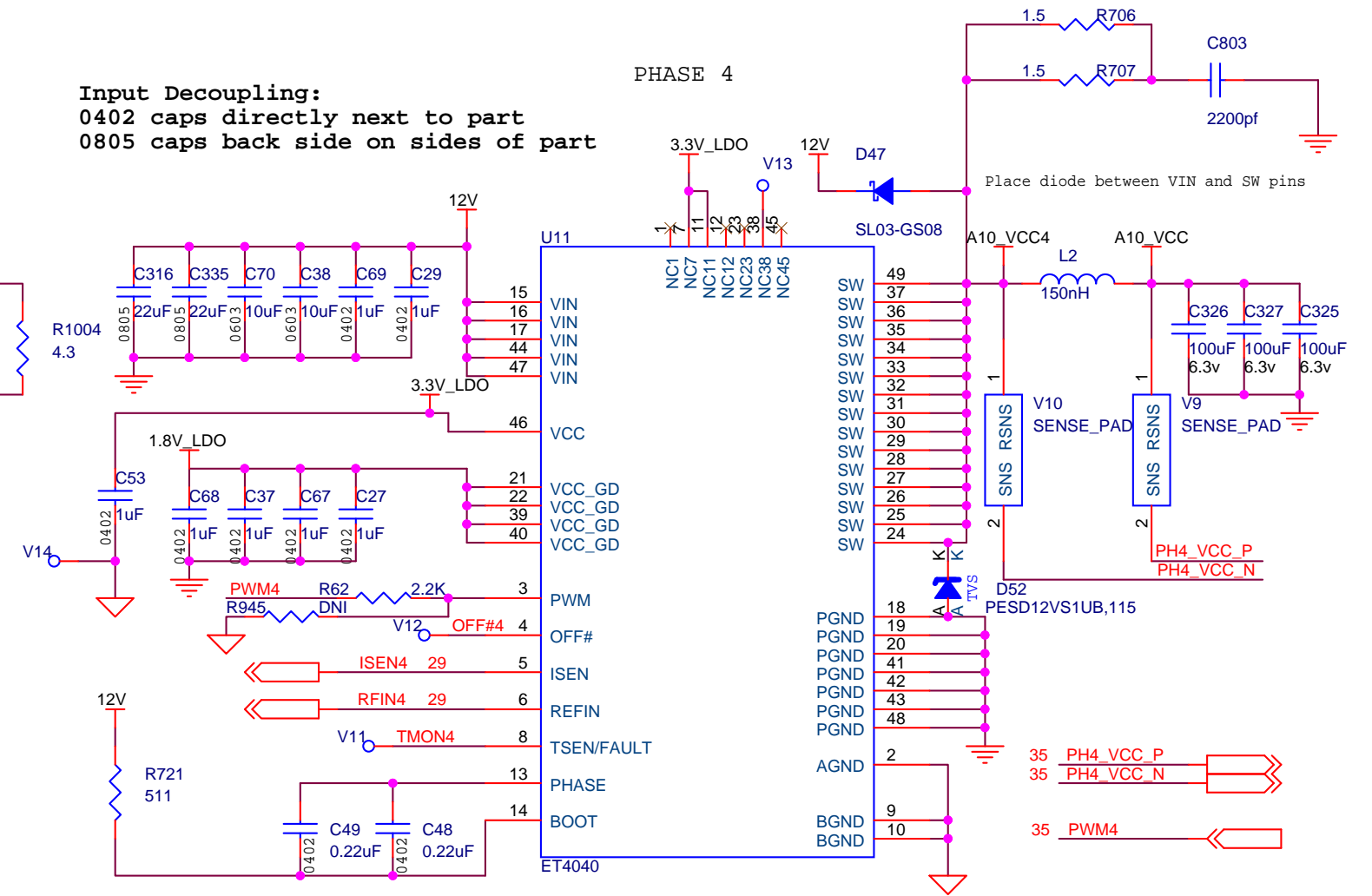
Input Decoupling:  
0402 caps directly next to part  
0805 caps back side on sides of part

PHASE 3

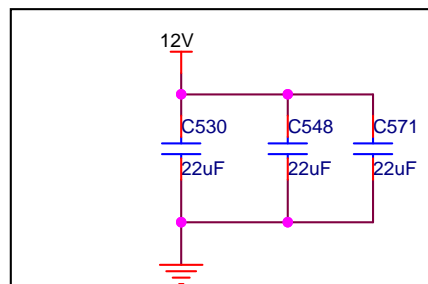


Input Decoupling:  
0402 caps directly next to part  
0805 caps back side on sides of part

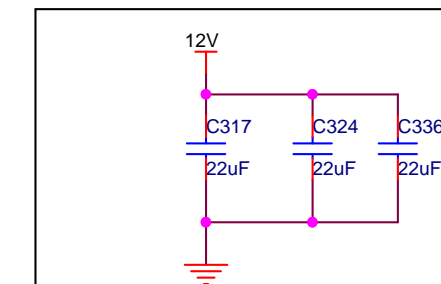
PHASE 4



Input caps on part pads directly under part



Input caps on part pads directly under part



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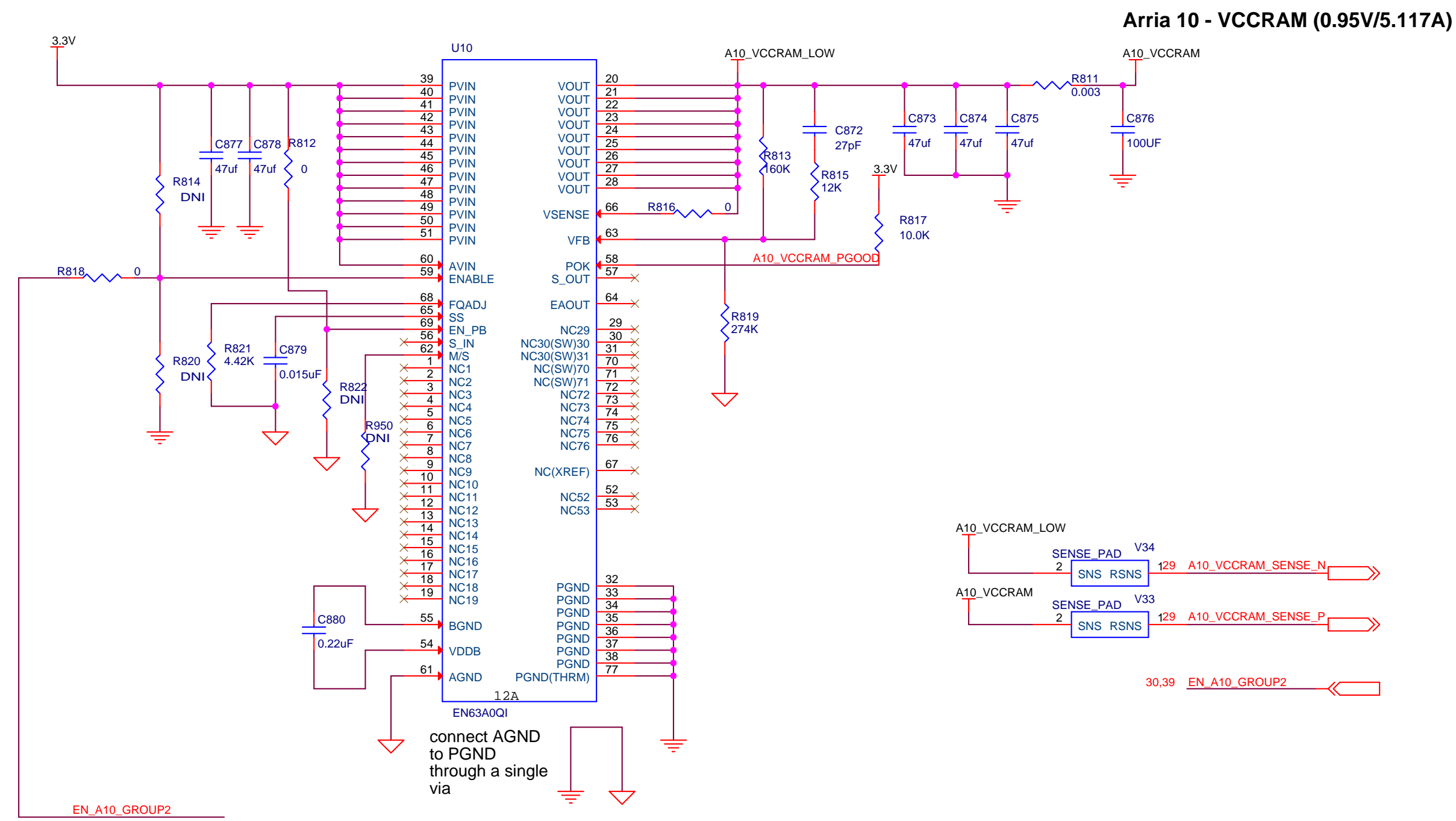
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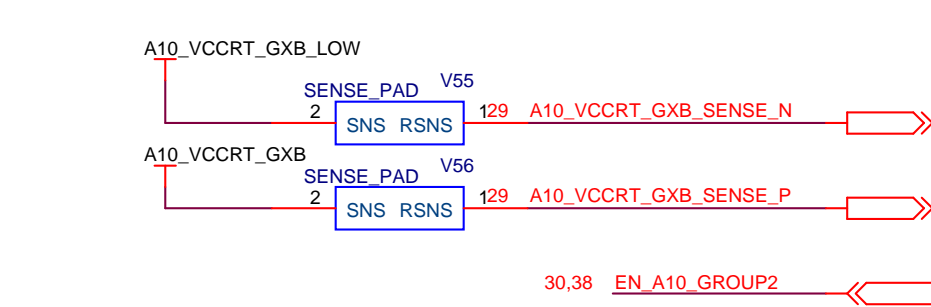
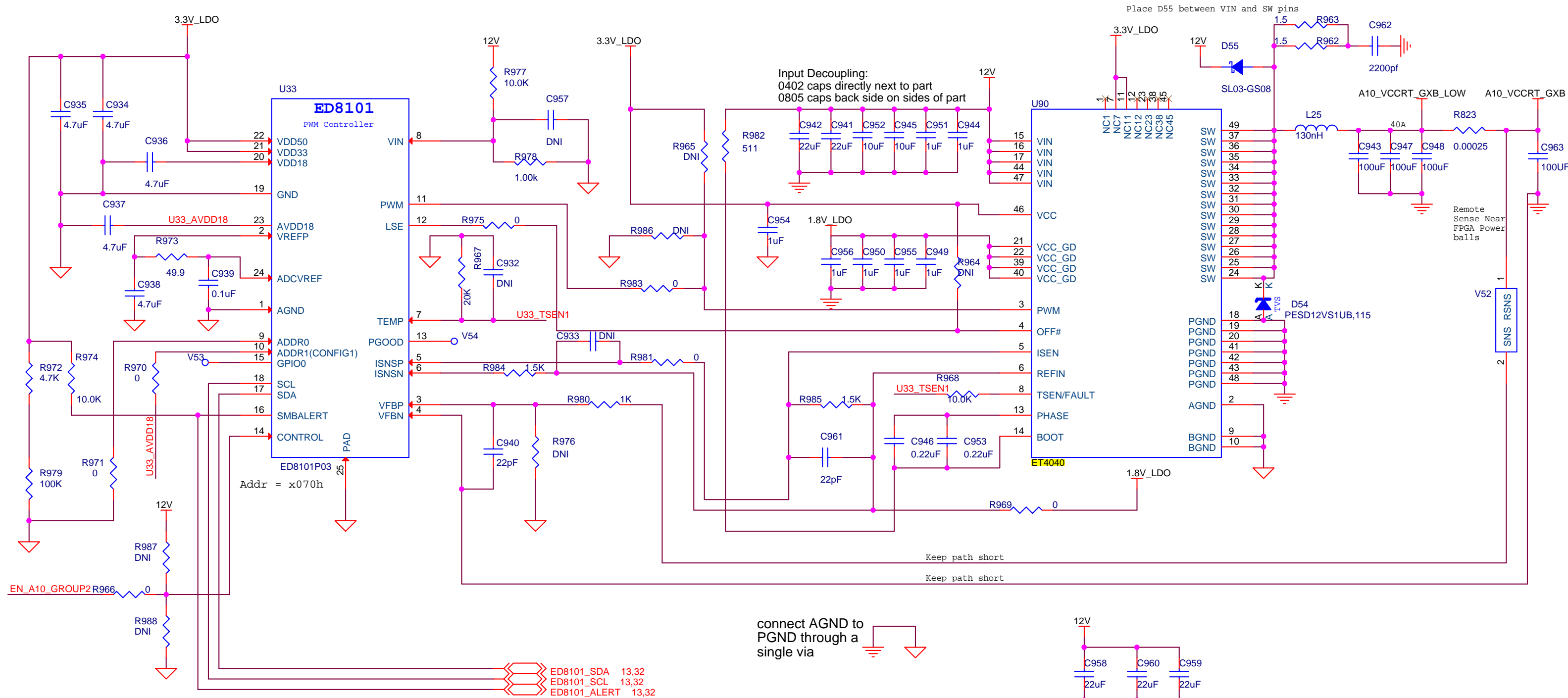
# Power - A10 VCCRAM





# Power - A10 VCCRT GXB

Arria 10 - VCCRT\_GXB (1.03V/17A)  
Can be 0.9V, 1.03V, or 1.1V



connect AGND to PGND through a single via

place bulk input caps on pads under ET4040 device

ED8101\_SDA 13,32  
ED8101\_SCL 13,32  
ED8101\_ALERT 13,32

Keep path short

Keep path short



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8 7 6 5 4 3 2 1

E  
D  
C  
B  
A

E  
D  
C  
B  
A

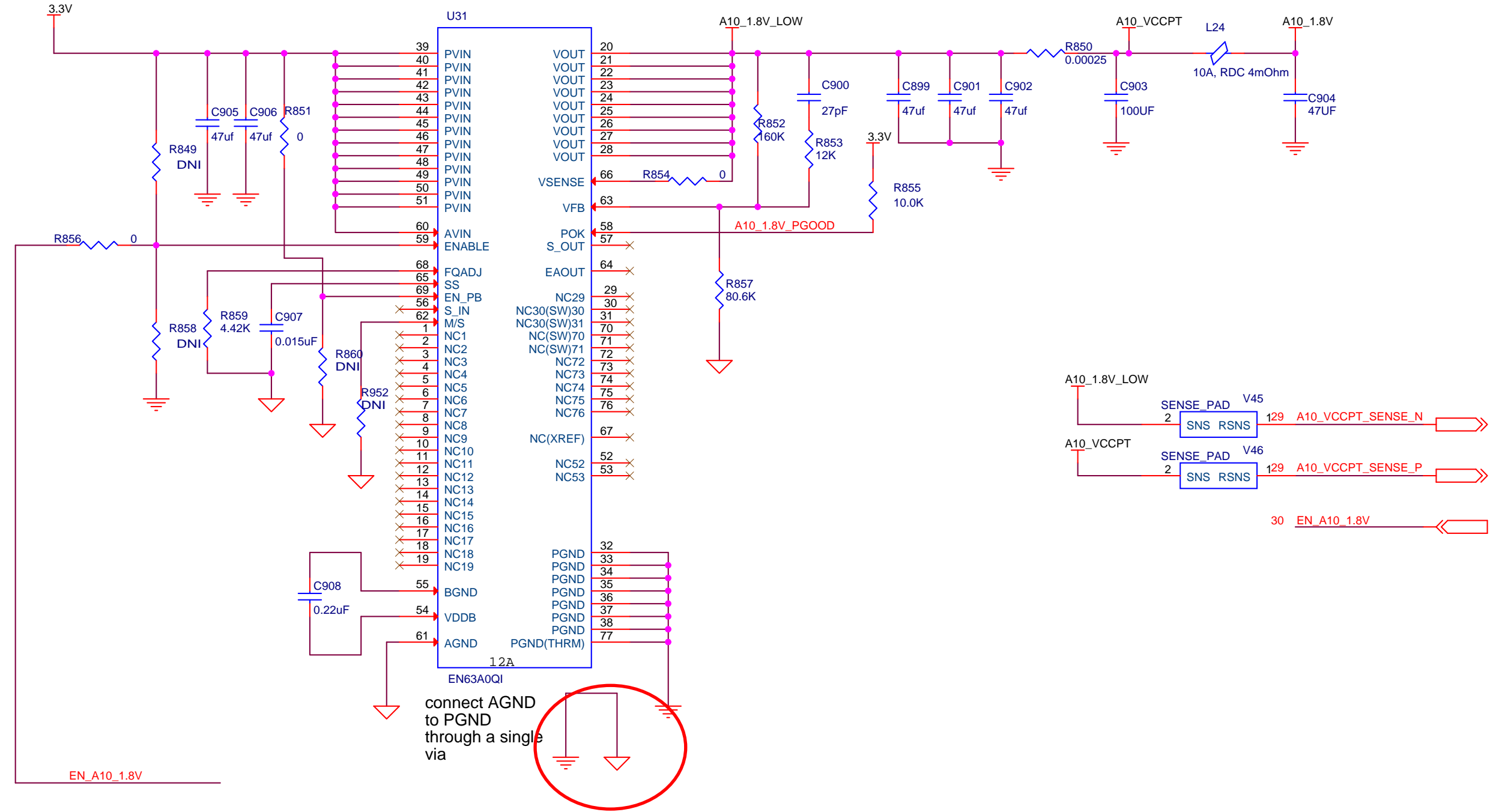


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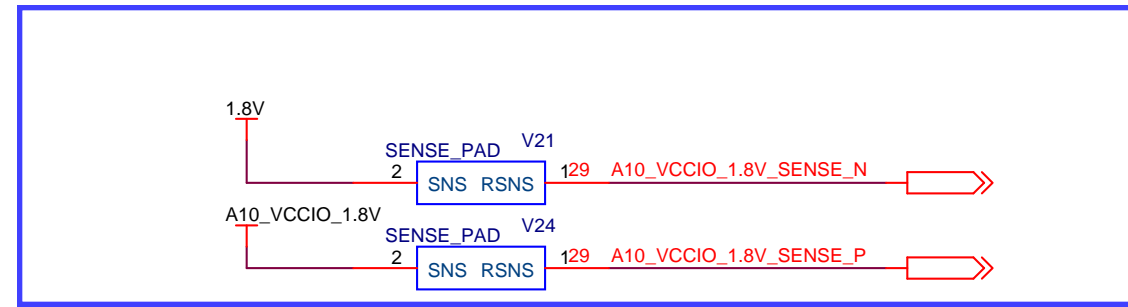
8 7 6 5 4 3 2 1

# Power - A10 VCCPT & 1.8V

Arria 10  
VCCA\_PLL, VCCH\_GXB, VCCPT  
(1.8V/10.229A)

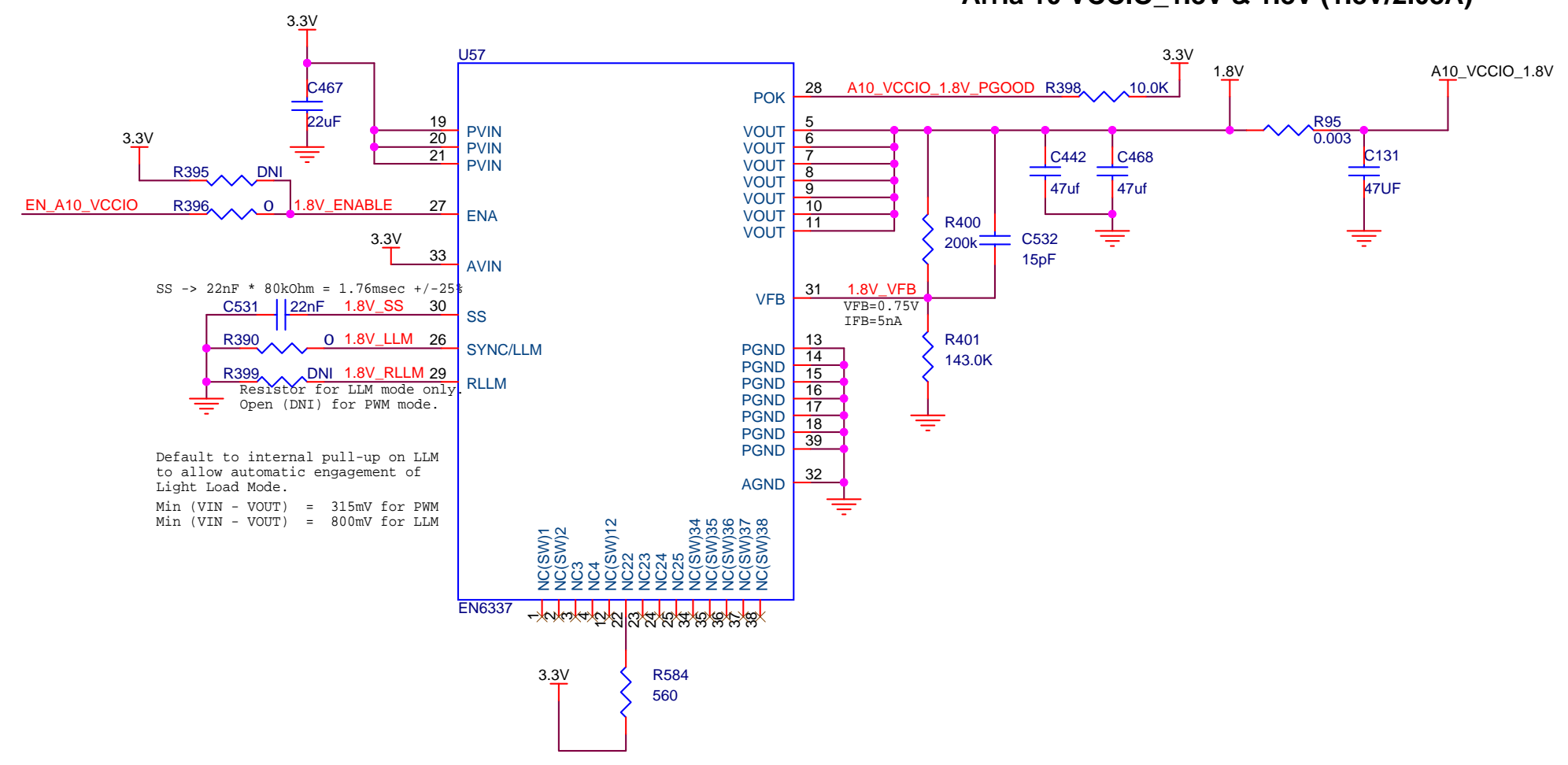


# Power - A10 VCCIO 1.8V



34,43,44,45,49 EN\_A10\_VCCIO

35 A10\_VCCIO\_1.8V\_PGOOD

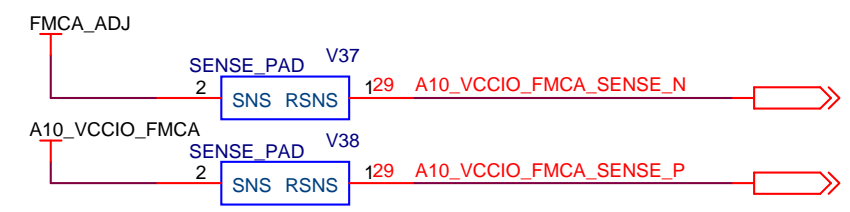


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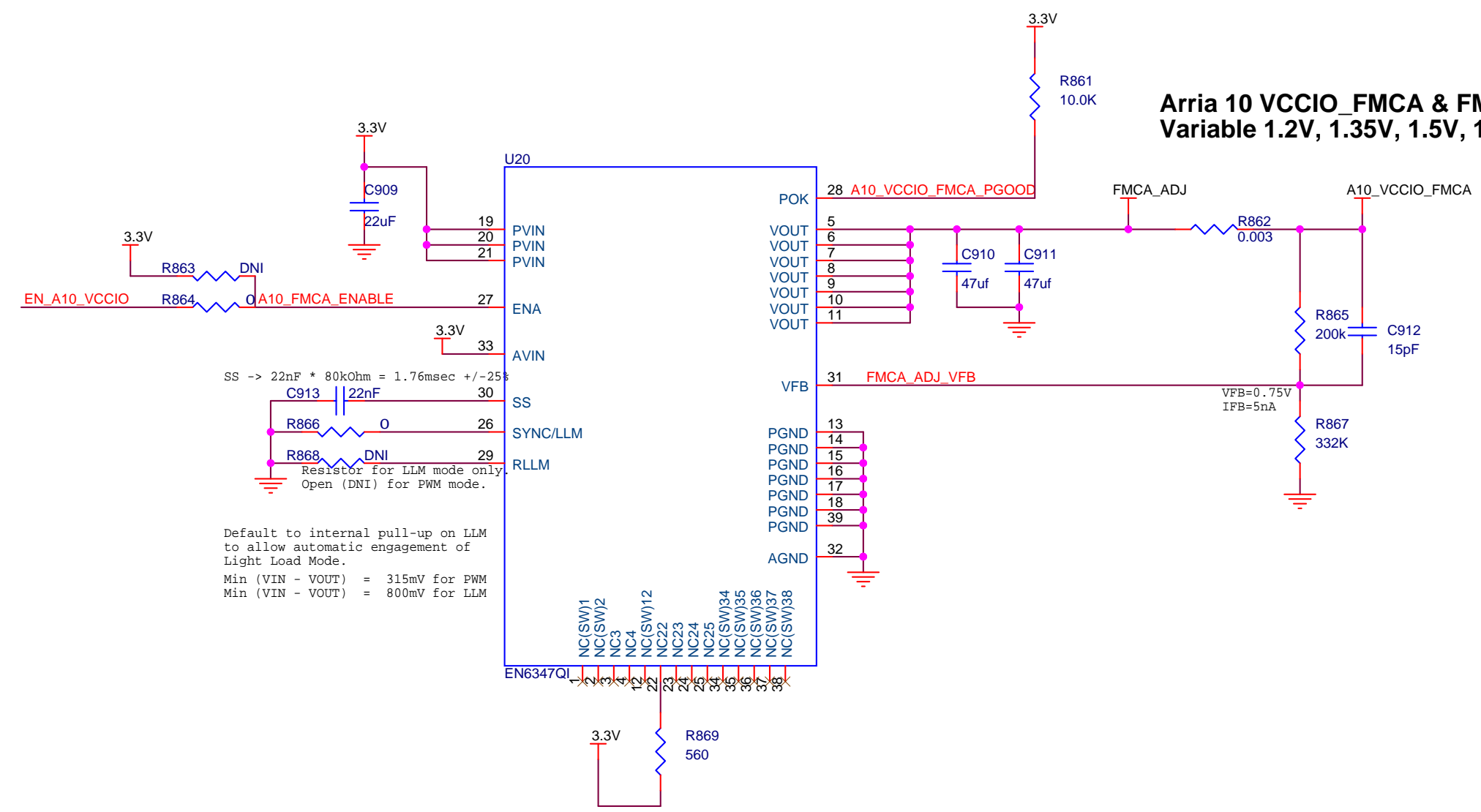


# Power - A10 VCCIO FMCA

34,42,44,45,49 EN\_A10\_VCCIO  
 35 A10\_VCCIO\_FMCA\_PGOOD

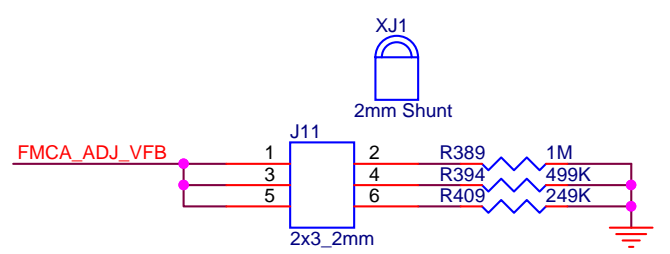


## Arria 10 VCCIO\_FMCA & FMCA\_VADJ (1.2V/3.5A) Variable 1.2V, 1.35V, 1.5V, 1.8V



SS ->  $22nF * 80k\Omega = 1.76msec \pm 25\%$   
 C913 22nF  
 R866 0  
 R868 DNI  
 Resistor for LLM mode only  
 Open (DNI) for PWM mode.

Default to internal pull-up on LLM  
 to allow automatic engagement of  
 Light Load Mode.  
 Min (VIN - VOUT) = 315mV for PWM  
 Min (VIN - VOUT) = 800mV for LLM



FMCA Voltage

Setting	VCCIO FMCA SELECT
NO JUMPER	1.2V
JUMPER 1-2	1.35V
JUMPER 3-4	1.5V
JUMPER 5-6	1.8V



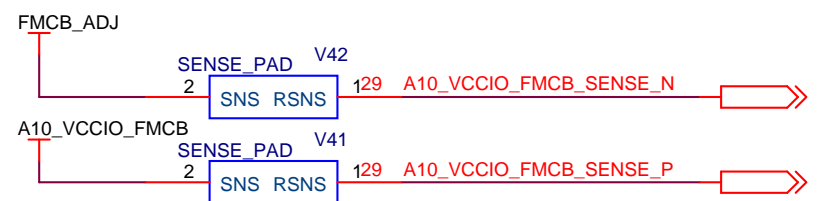
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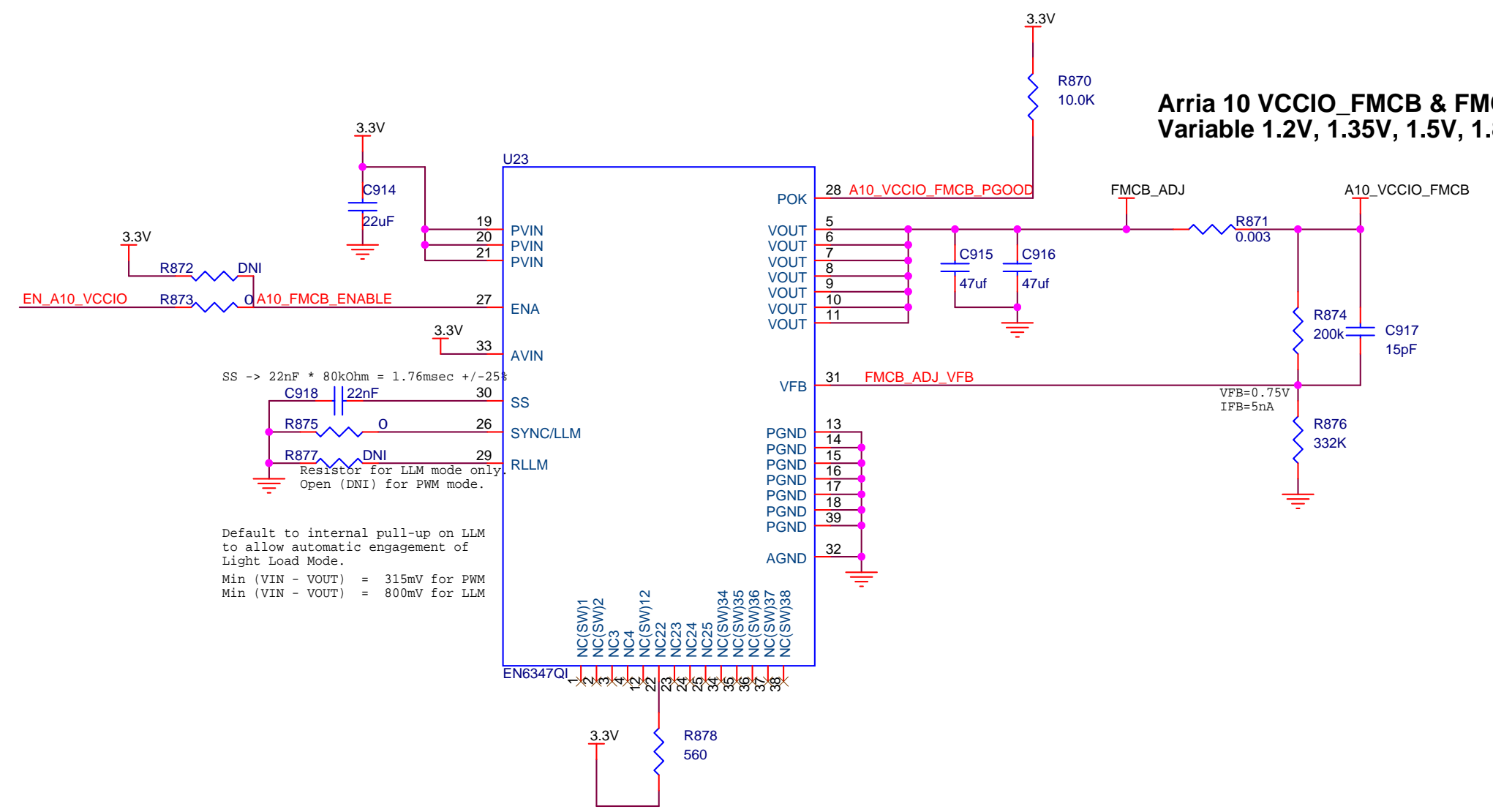
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# Power - A10 VCCIO FMCB

3,45,49 EN\_A10\_VCCIO  
 35 A10\_VCCIO\_FMCB\_PGOOD

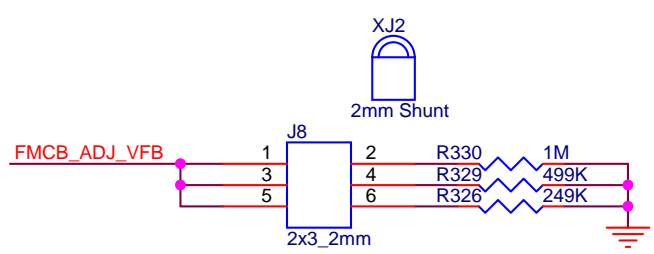


## Arria 10 VCCIO\_FMCB & FMCB\_VADJ (1.2V/3.5A) Variable 1.2V, 1.35V, 1.5V, 1.8V



SS ->  $22nF * 80k\Omega = 1.76msec +/- 25%$   
 Resistor for LLM mode only.  
 Open (DNI) for PWM mode.

Default to internal pull-up on LLM to allow automatic engagement of Light Load Mode.  
 Min (VIN - VOUT) = 315mV for PWM  
 Min (VIN - VOUT) = 800mV for LLM



**FMCA Voltage**

Setting	VCCIO FMCB SELECT
NO JUMPER	1.2V
JUMPER 1-2	1.35V
JUMPER 3-4	1.5V
JUMPER 5-6	1.8V



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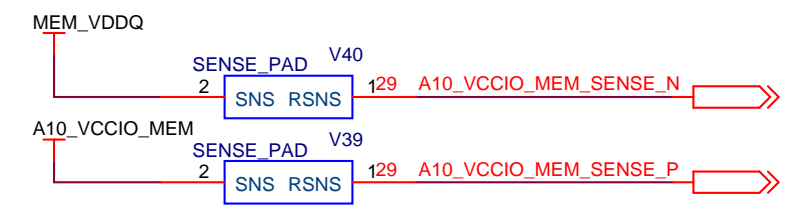
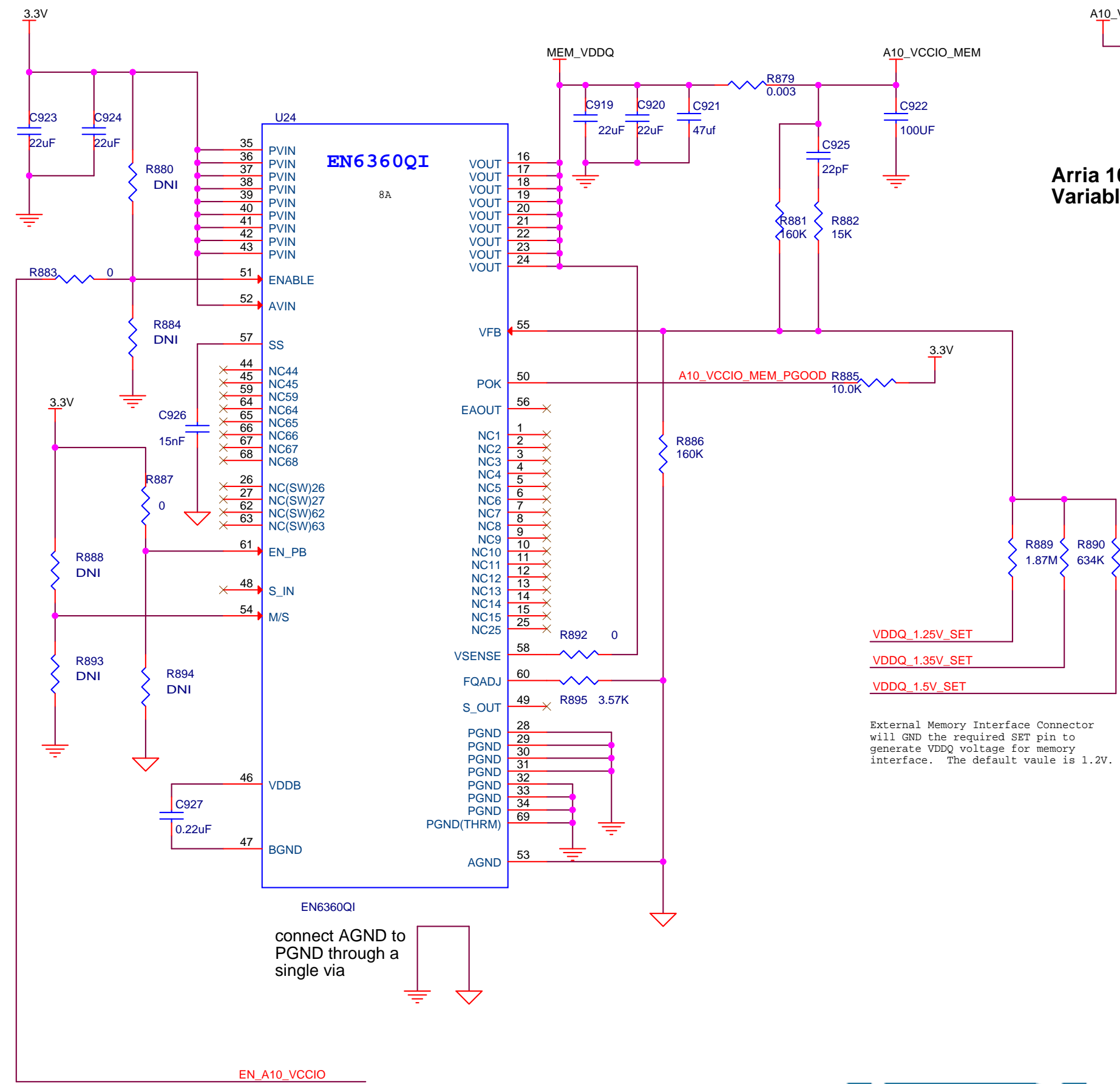
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# Power - A10 VCCIO MEM

## POWER CONTROL

- 17 VDDQ\_1.25V\_SET
- 17 VDDQ\_1.35V\_SET
- 17 VDDQ\_1.5V\_SET
- 49 EN\_A10\_VCCIO
- 35 A10\_VCCIO\_MEM\_PGOOD



**Arria 10 VCCIO\_MEM & MEM\_VDDQ (1.2V/4.7A)  
Variable 1.2V, 1.25V, 1.35V, 1.5V**

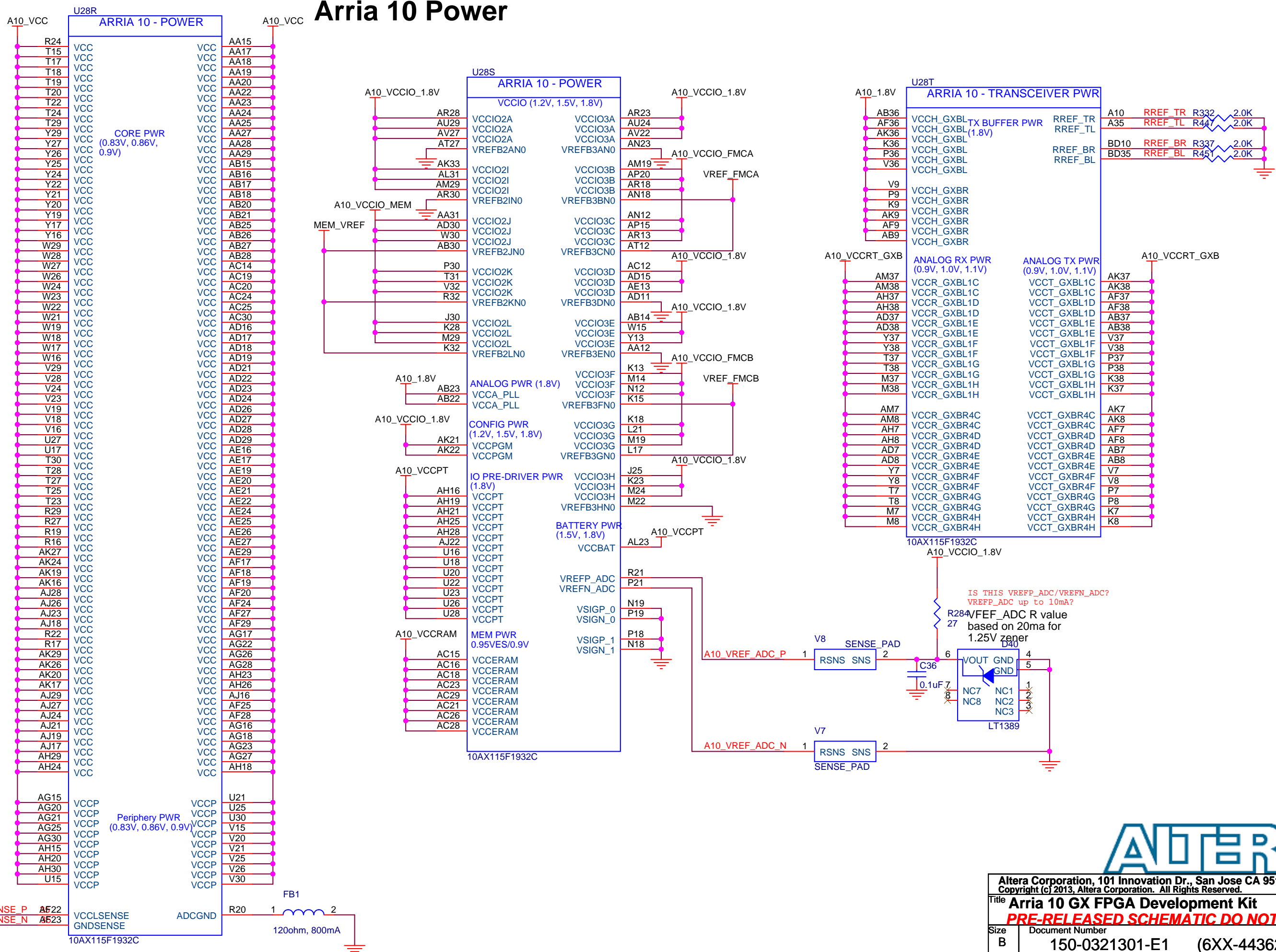
- VDDQ\_1.25V\_SET
- VDDQ\_1.35V\_SET
- VDDQ\_1.5V\_SET

External Memory Interface Connector will GND the required SET pin to generate VDDQ voltage for memory interface. The default vaule is 1.2V.



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# Arria 10 Power







# Decoupling

**Do Not Copy. Decoupling requirements is design specific. Please use the Early Power Estimator and PDN Tool available on Altera.com to determine your specific decoupling requirements.**



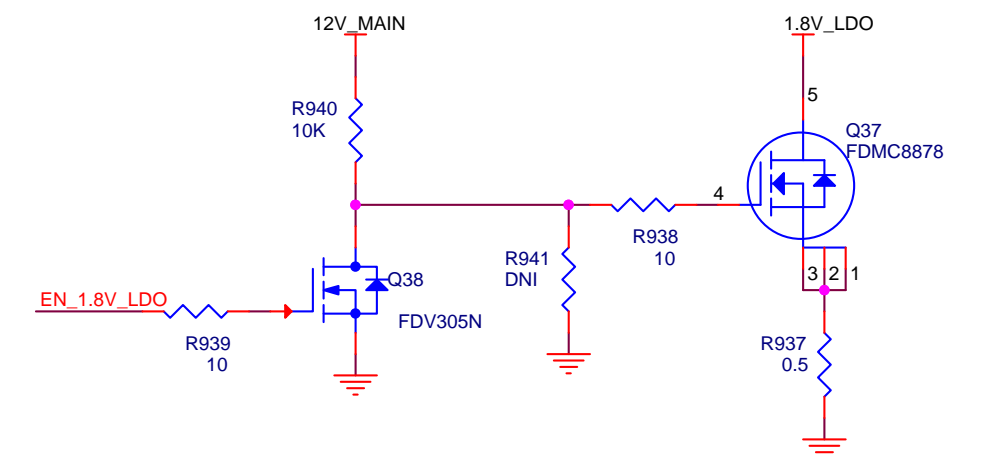
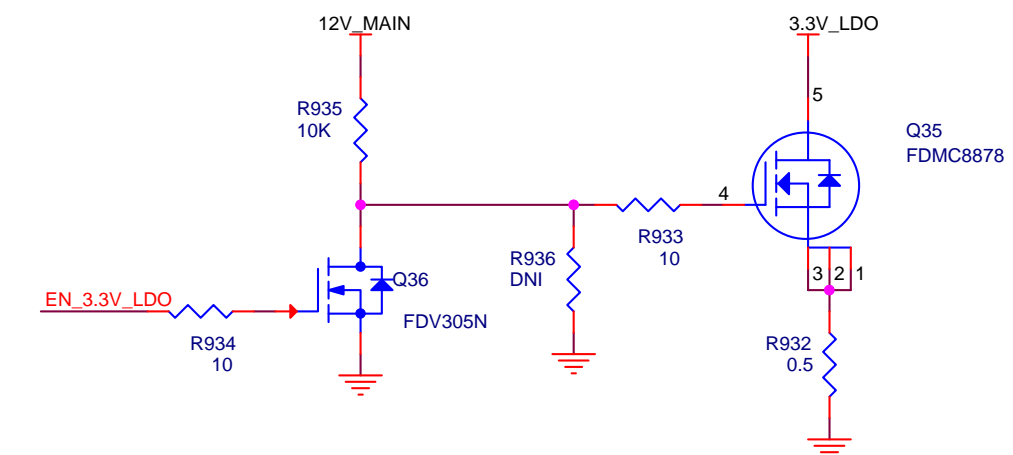
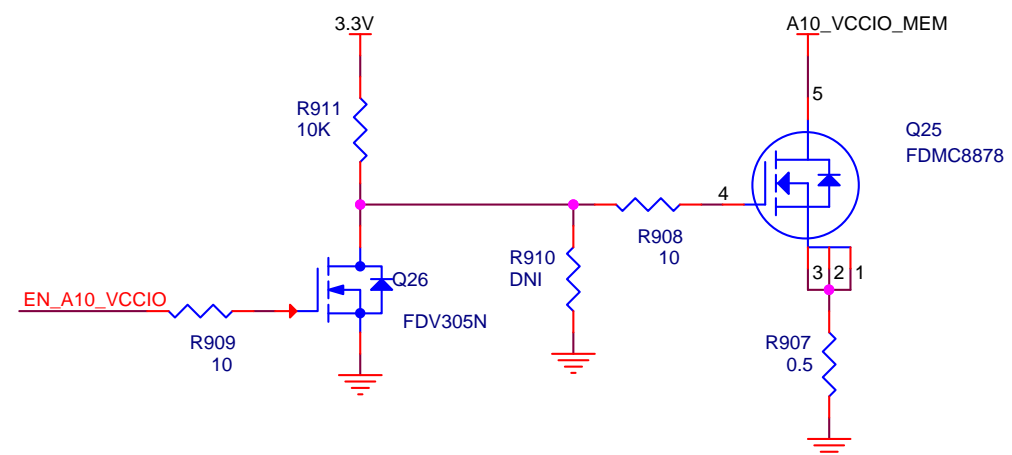
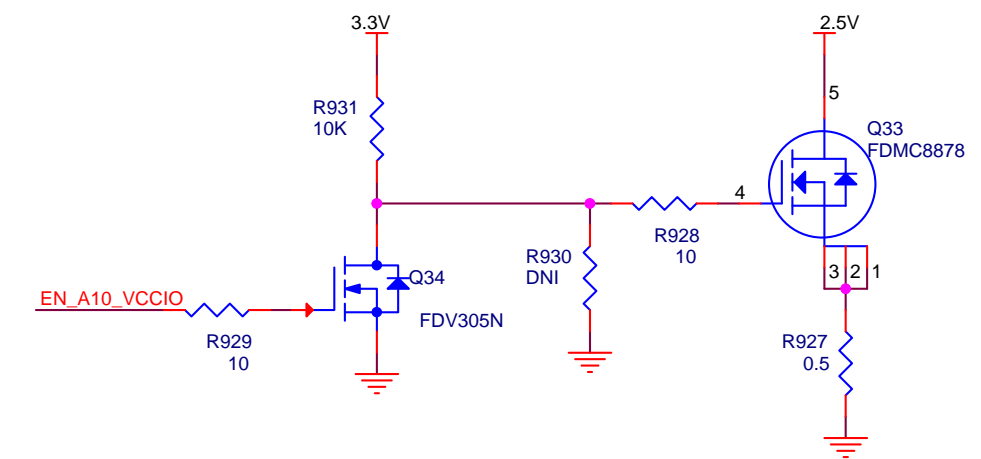
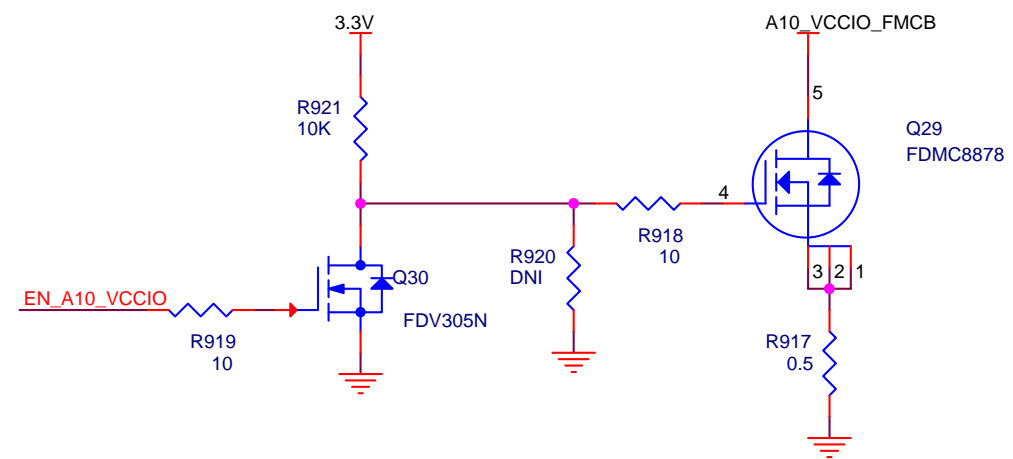
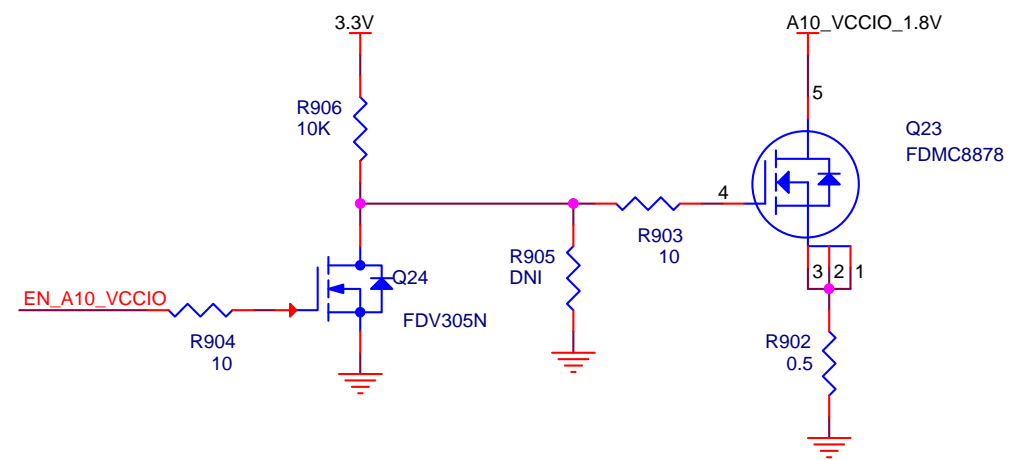
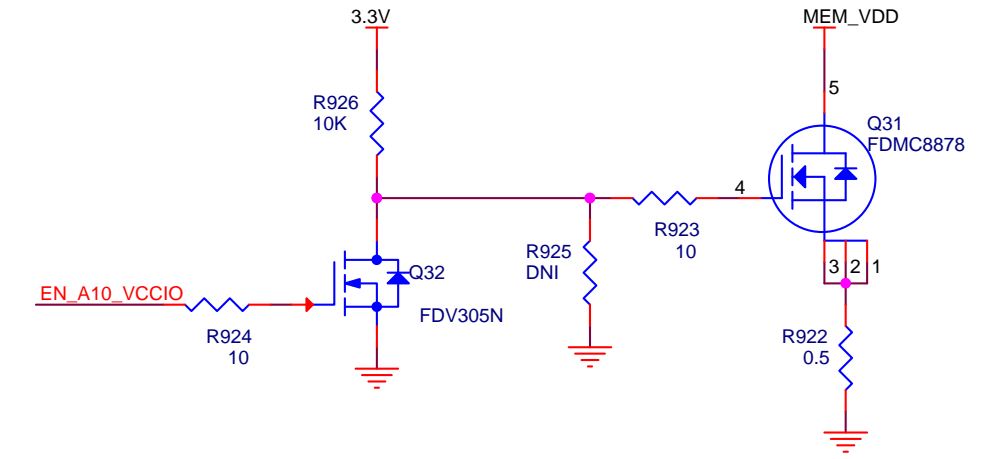
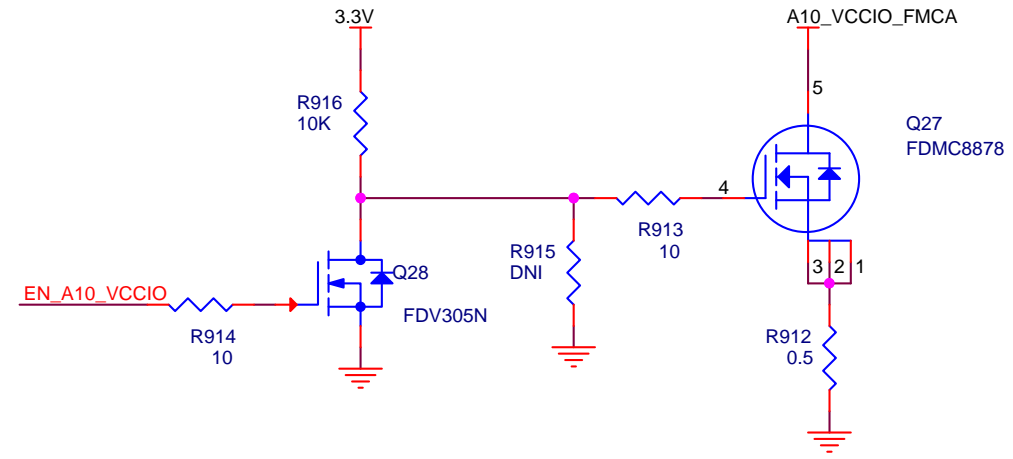
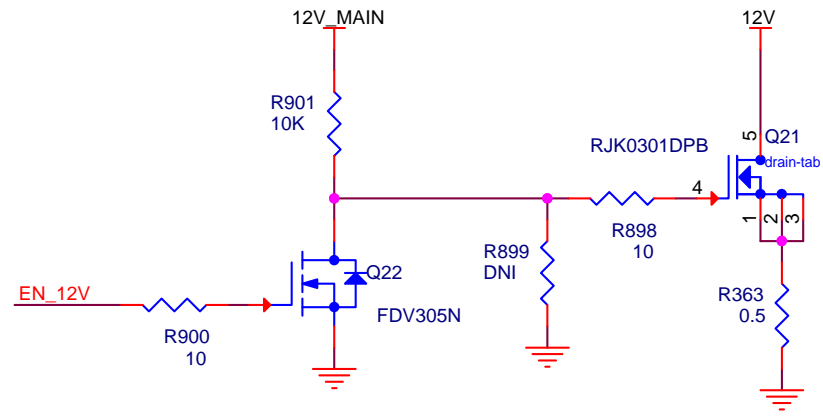
SCREW1	STANDOFF1	PCB1
SCREW2	STANDOFF2	
SCREW3	STANDOFF3	
SCREW4	STANDOFF4	
SCREW5	STANDOFF5	



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# Power-down Fast Discharge

- EN\_12V 30,31
- EN\_A10\_VCCIO 30,34,42,43,44,45
- EN\_3.3V\_LDO 30,32
- EN\_1.8V\_LDO 30,32



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