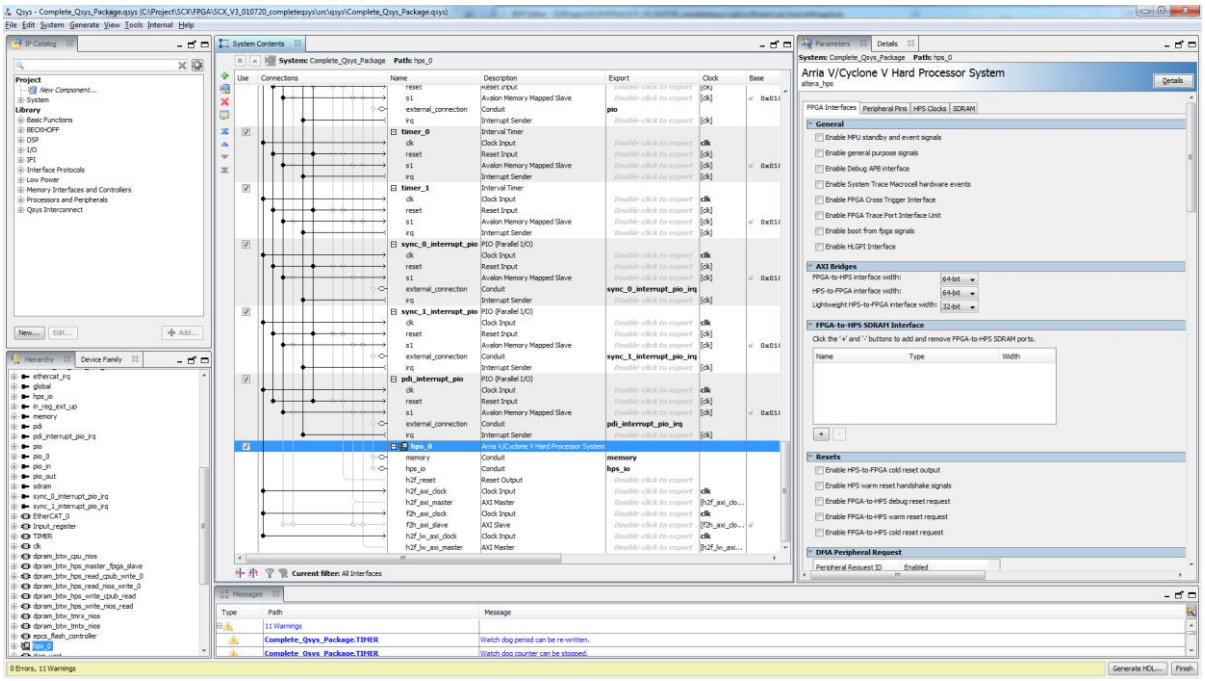
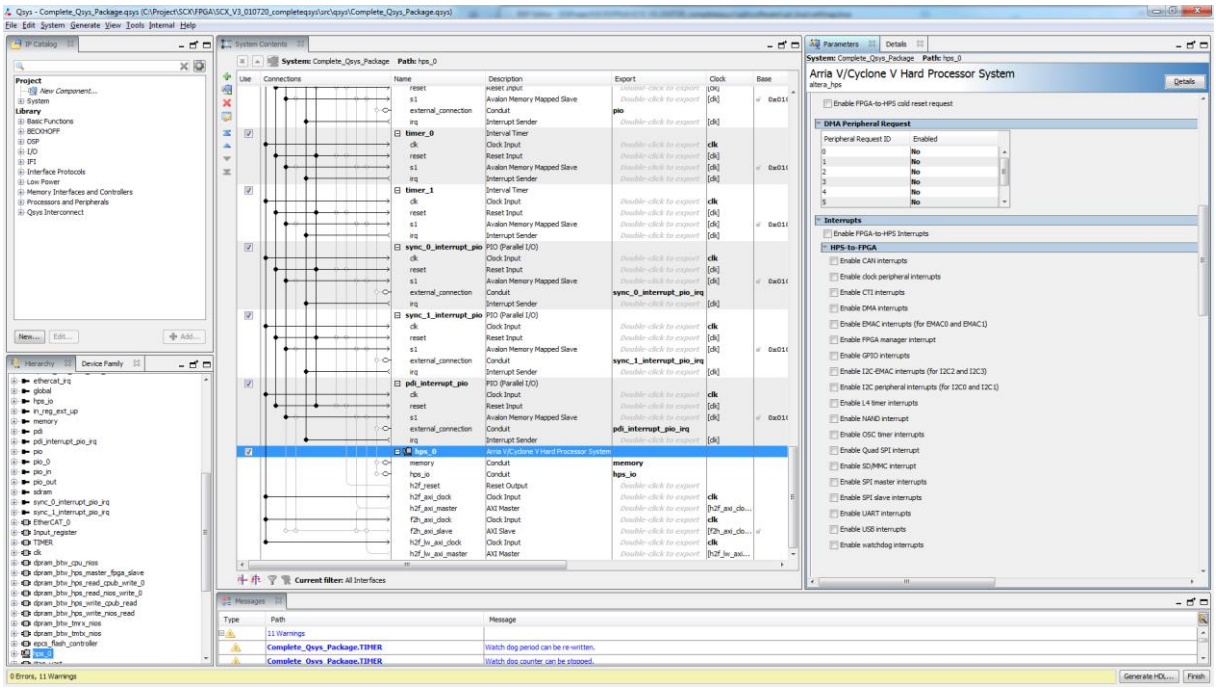
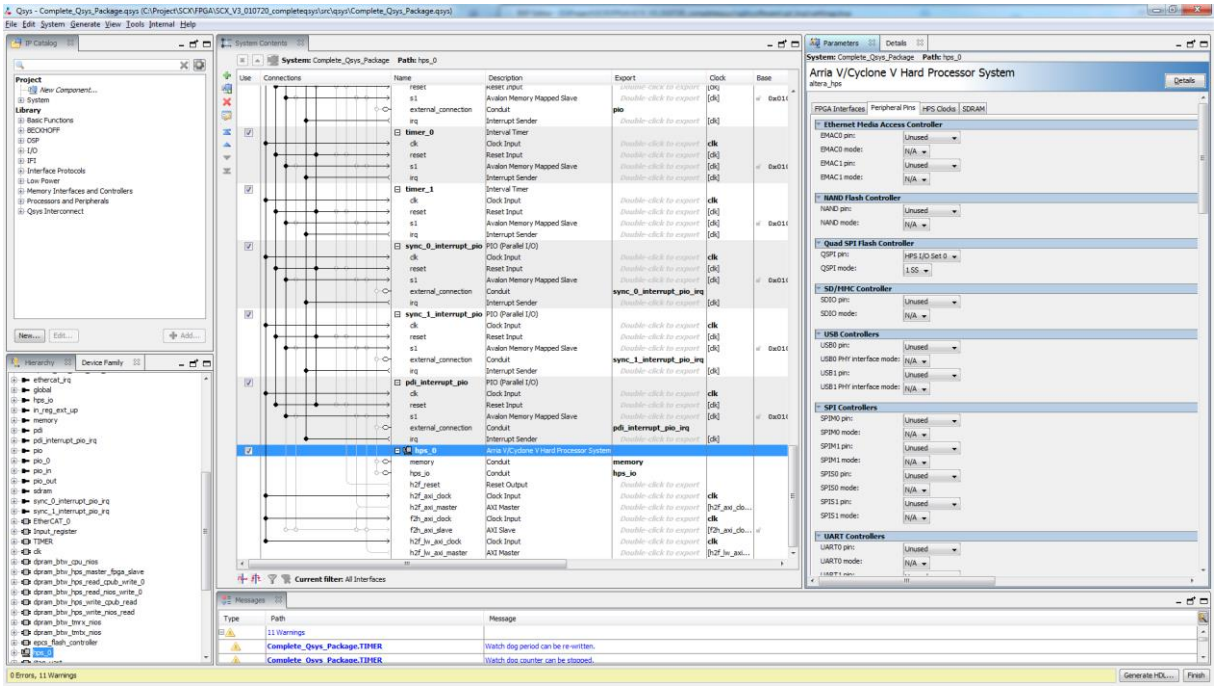
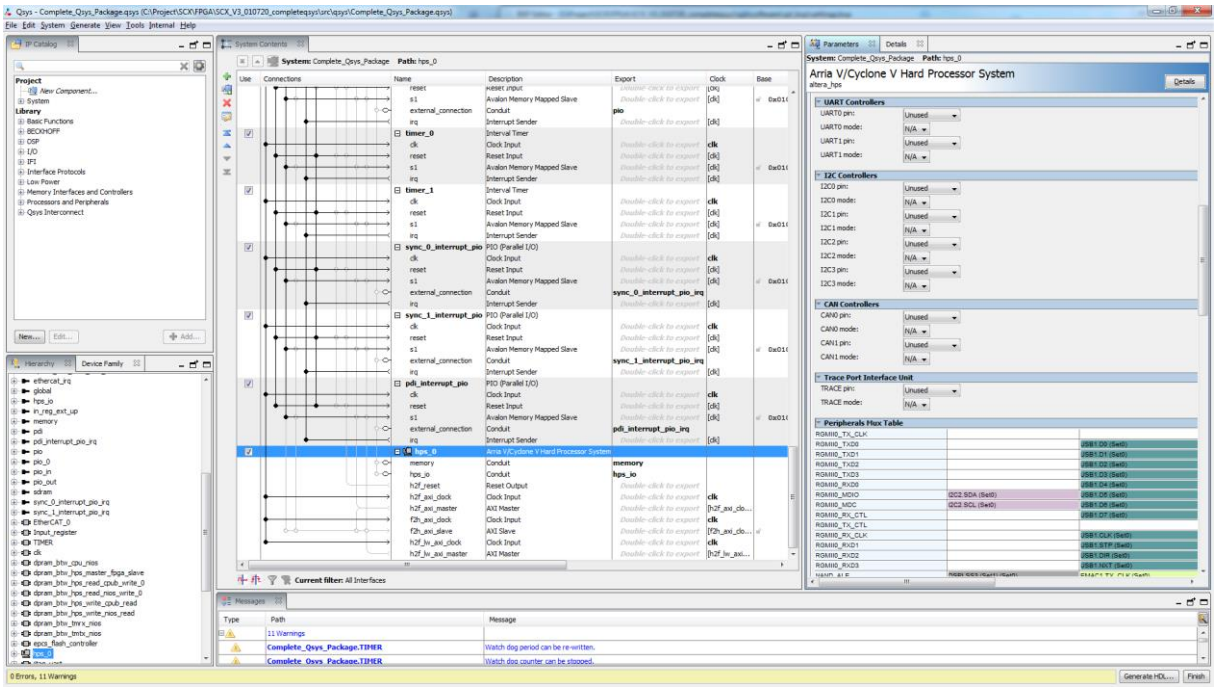
1. **HPS in the qsys and its settings**
   We are using almost empty hps with only basic settings for the DDR3.
   Following is the settings of the QSPI and the HPS in QSYS project.

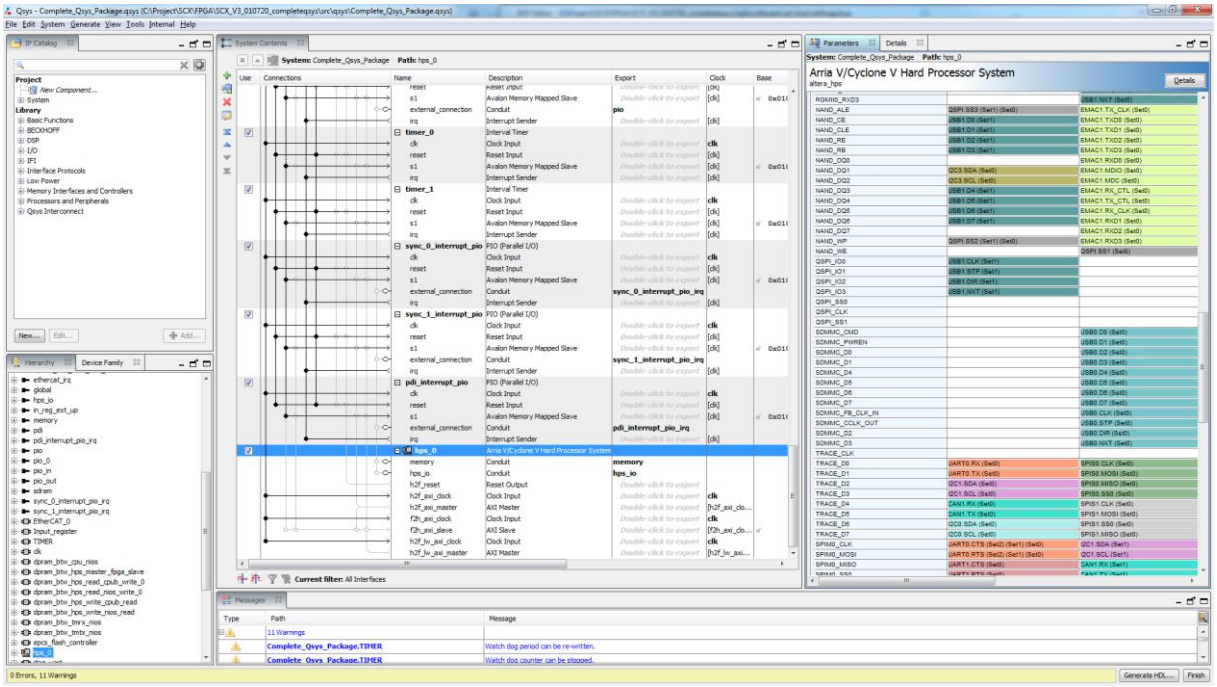


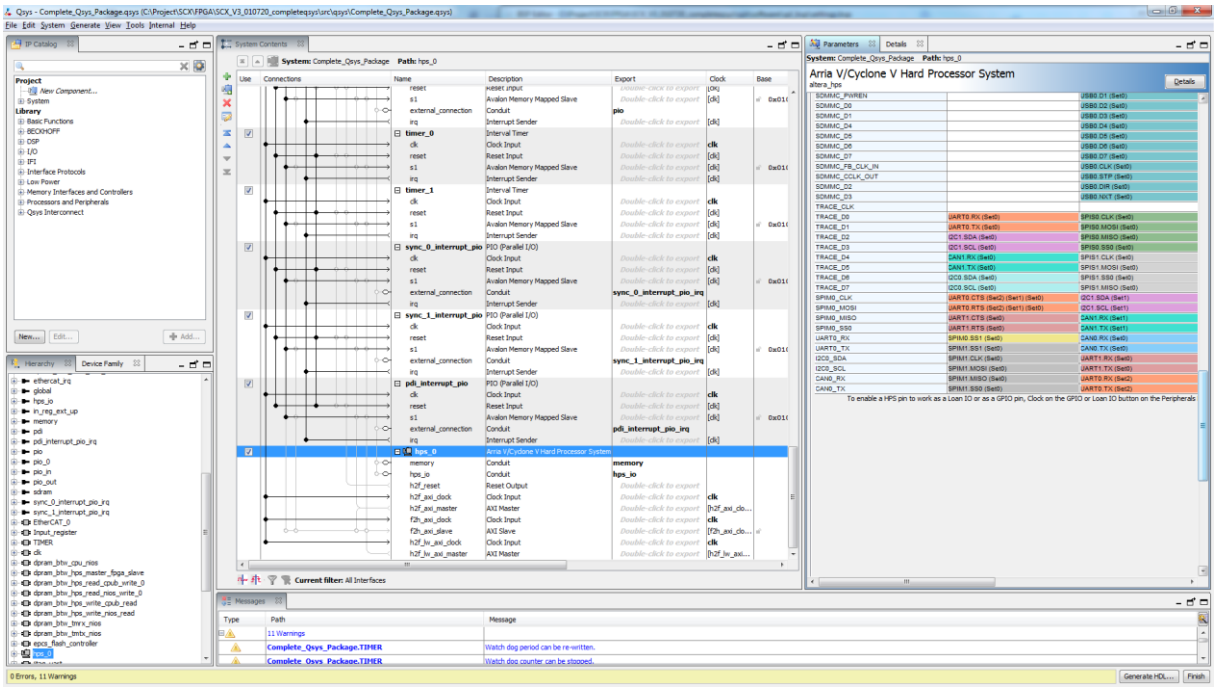


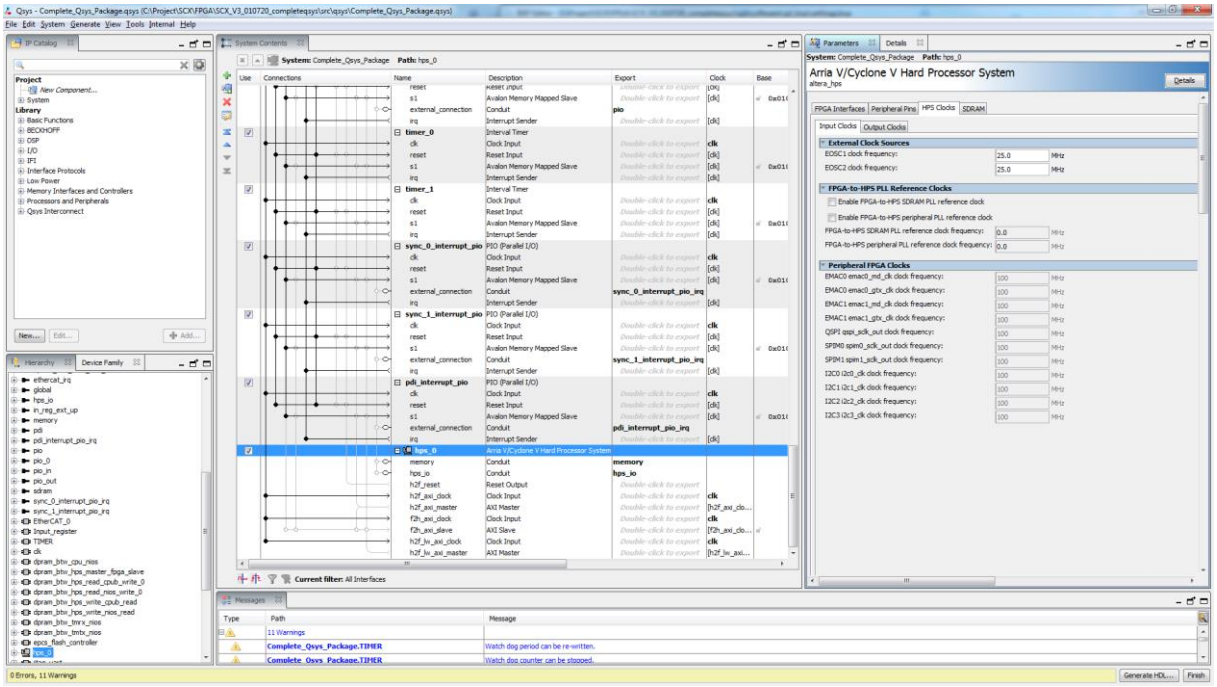
As we are flashing from QSPI we need only QSPI flash controller

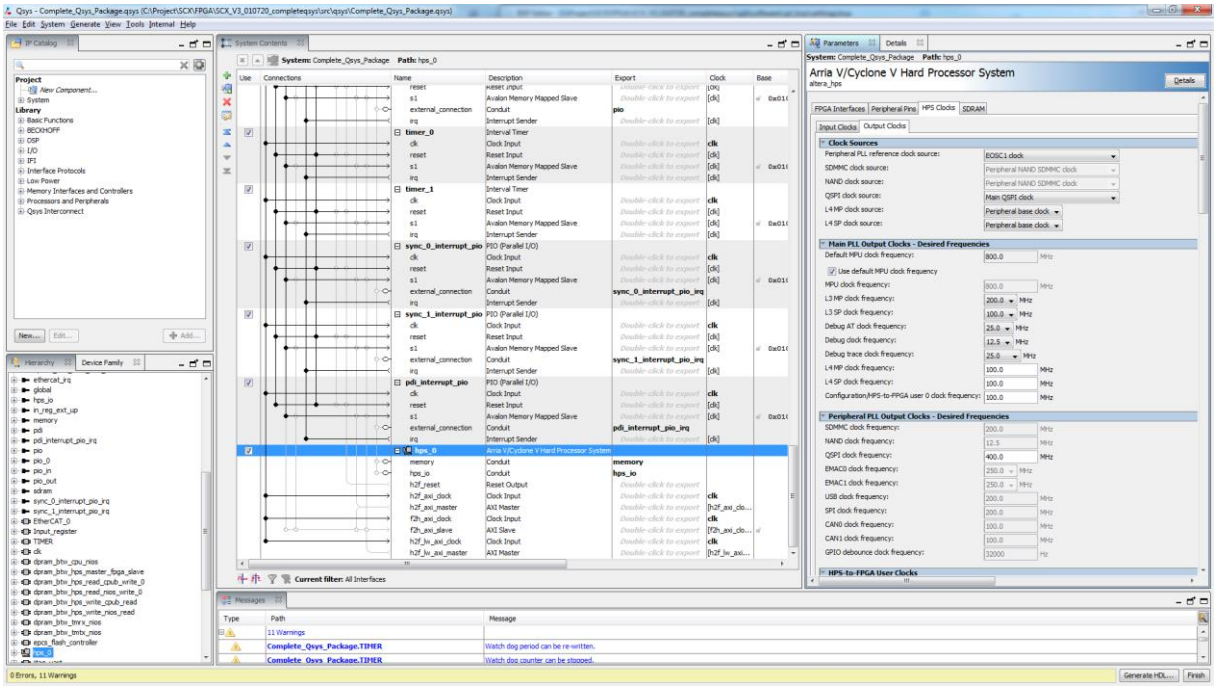

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
OSP
I/O
IFI
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New...
Edit...
Add...
Hierarchy
Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
timer_0
timer_1
sync_0_interrupt_pio
sync_1_interrupt_pio
pdi_interrupt_pio
hps_0
Arria V/Cyclone V Hard Processor System
Current filter: All Interfaces
Parameters
Details
Arria V/Cyclone V Hard Processor System
altera_hps
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
Ethernet Media Access Controller
NAND Flash Controller
Quad SPI Flash Controller
SD/MMC Controller
USB Controllers
SPI Controllers
UART Controllers
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER
Watch dog period can be re-written.
Complete_Qsys_Package.TIMER
Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL...
Finish

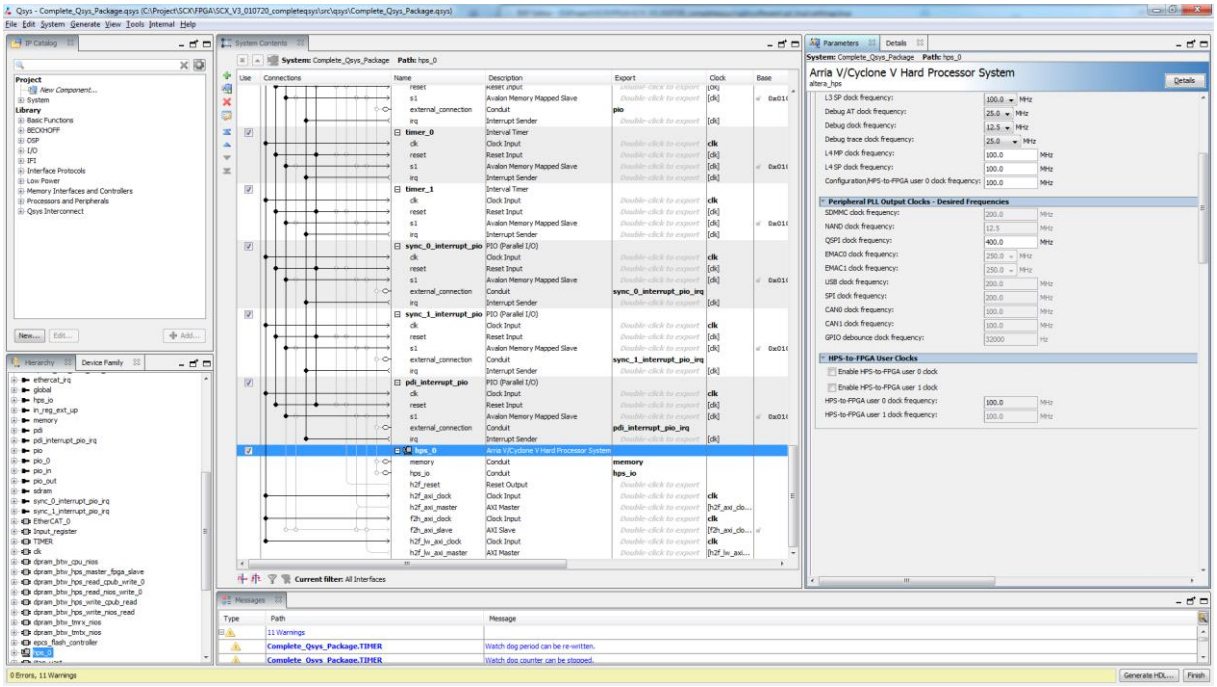

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
OSP
I/O
IFI
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New...
Edit...
Add...
Hierarchy
Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
timer_0
timer_1
sync_0_interrupt_pio
sync_1_interrupt_pio
pdi_interrupt_pio
hps_0
Arria V/Cyclone V Hard Processor System
Current filter: All Interfaces
Parameters
Details
Arria V/Cyclone V Hard Processor System
altera_hps
UART Controllers
I2C Controllers
CAN Controllers
Trace Port Interface Unit
Peripherals Mux Table
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER
Watch dog period can be re-written.
Complete_Qsys_Package.TIMER
Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL...
Finish

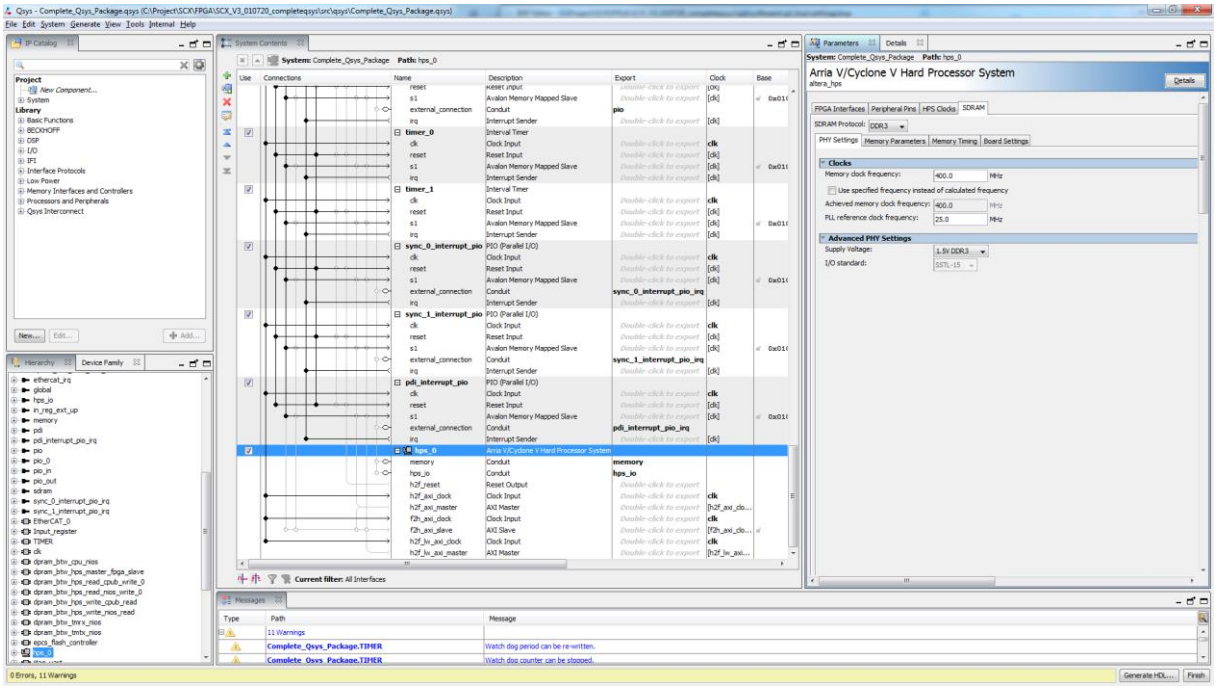

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
DSP
I/O
IFI
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New... Edit... Add...
Hierarchy
Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
reset reset input
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pio
irq Interrupt Sender [clk]
timer_0 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
timer_1 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
sync_0_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_0_interrupt_pio_irq
irq Interrupt Sender [clk]
sync_1_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_1_interrupt_pio_irq
irq Interrupt Sender [clk]
pdi_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pdi_interrupt_pio_irq
irq Interrupt Sender [clk]
hps_0 Arria V/Cyclone V Hard Processor System
memory Conduit memory
hps_io Conduit hps_io
h2f_reset Reset Output
h2f_axi_clock Clock Input clk
h2f_axi_master AXI Master [h2f_axi_clo...
f2h_axi_clock Clock Input clk
f2h_axi_slave AXI Slave [f2h_axi_clo...
h2f_lw_axi_clock Clock Input clk
h2f_lw_axi_master AXI Master [h2f_lw_axi...
Current filter: All Interfaces
Parameters Details
System: Complete_Qsys_Package Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
Details
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL... Finish

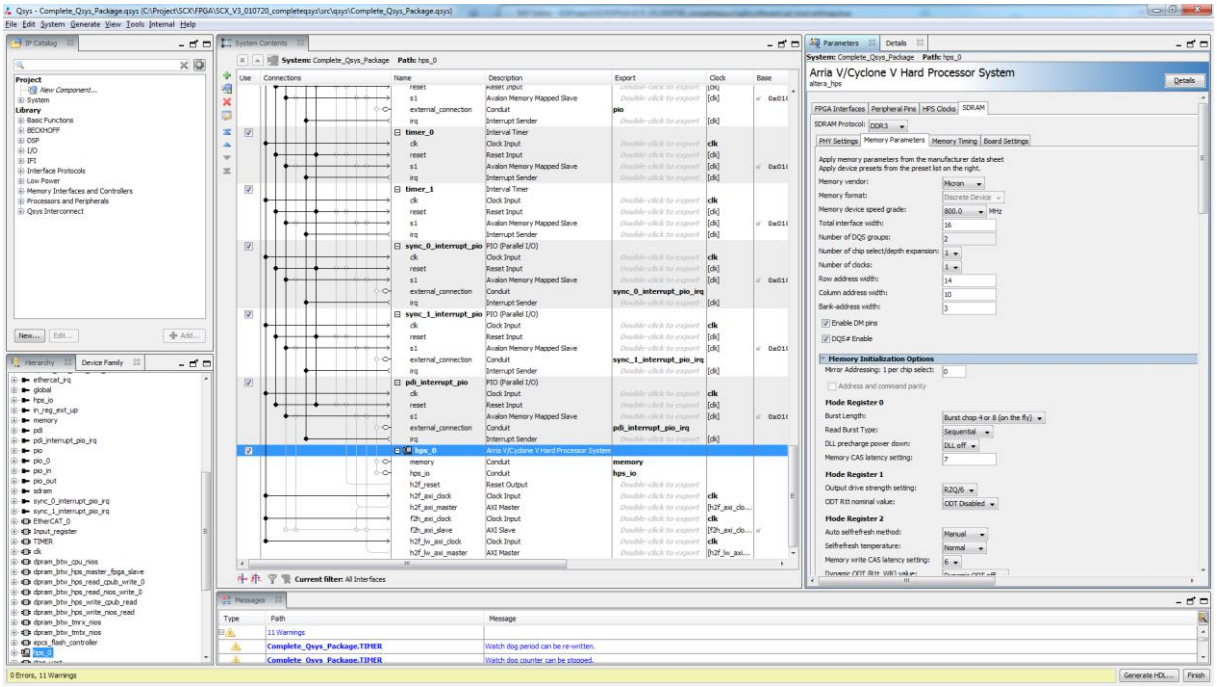

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
DSP
I/O
IFI
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New... Edit... Add...
Hierarchy
Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
reset reset input
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pio
irq Interrupt Sender [clk]
timer_0 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
timer_1 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
sync_0_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_0_interrupt_pio_irq
irq Interrupt Sender [clk]
sync_1_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_1_interrupt_pio_irq
irq Interrupt Sender [clk]
pdi_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pdi_interrupt_pio_irq
irq Interrupt Sender [clk]
hps_0 Arria V/Cyclone V Hard Processor System
memory Conduit memory
hps_io Conduit hps_io
h2f_reset Reset Output
h2f_axi_clock Clock Input clk
h2f_axi_master AXI Master [h2f_axi_clo...
f2h_axi_clock Clock Input clk
f2h_axi_slave AXI Slave [f2h_axi_clo...
h2f_lw_axi_clock Clock Input clk
h2f_lw_axi_master AXI Master [h2f_lw_axi...
Current filter: All Interfaces
Parameters Details
System: Complete_Qsys_Package Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
Details
To enable a HPS pin to work as a Loan IO or as a GPIO pin, Clock on the GPIO or Loan IO button on the Peripherals
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL... Finish

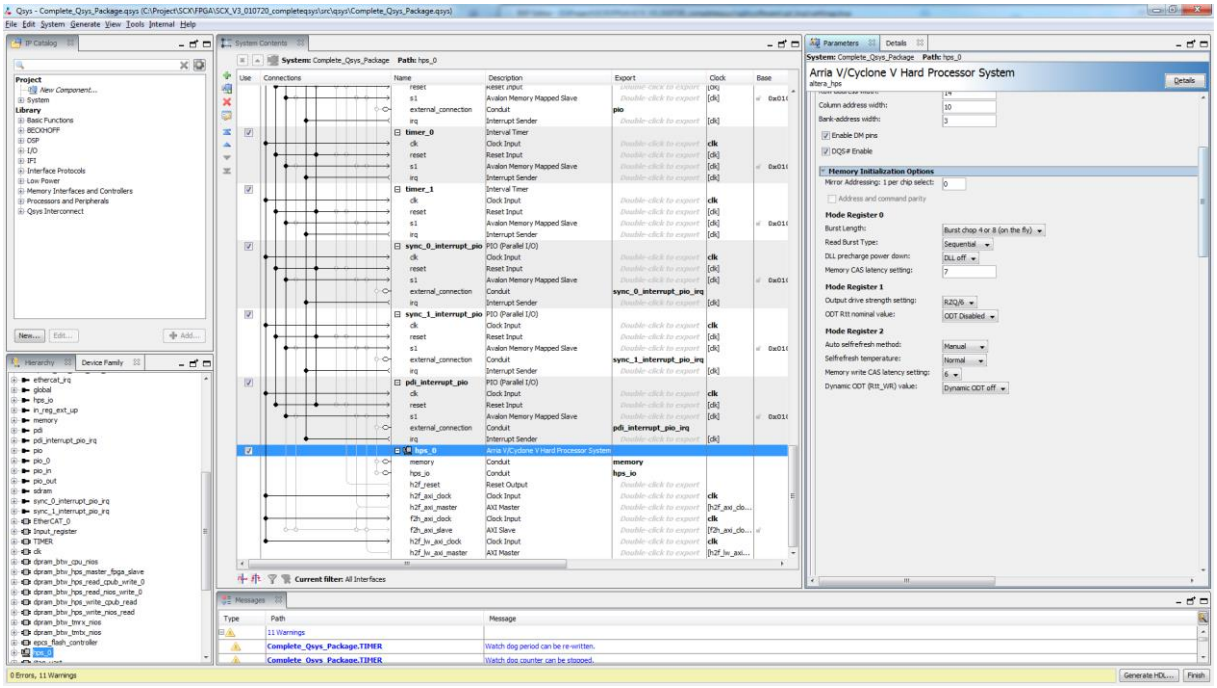

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
DSP
I/O
IP1
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New... Edit... Add...
Hierarchy
Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
reset reset input
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pio
irq Interrupt Sender [clk]
timer_0 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
timer_1 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
sync_0_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_0_interrupt_pio_irq
irq Interrupt Sender [clk]
sync_1_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_1_interrupt_pio_irq
irq Interrupt Sender [clk]
pdi_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pdi_interrupt_pio_irq
irq Interrupt Sender [clk]
hps_0 Arria V/Cyclone V Hard Processor System
memory Conduit memory
hps_io Conduit hps_io
h2f_reset Reset Output
h2f_axi_clock Clock Input clk
h2f_axi_master AXI Master [h2f_axi_clo...
f2h_axi_clock Clock Input clk
f2h_axi_slave AXI Slave [f2h_axi_clo...
h2f_lw_axi_clock Clock Input clk
h2f_lw_axi_master AXI Master [h2f_lw_axi...
Current filter: All Interfaces
Parameters Details
System: Complete_Qsys_Package Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
Details
FPGA Interfaces Peripheral Pins HPS Clocks SDRAM
Input Clocks Output Clocks
External Clock Sources
EOSC1 clock frequency: 25.0 MHz
EOSC2 clock frequency: 25.0 MHz
FPGA-to-HPS PLL Reference Clocks
Enable FPGA-to-HPS SDRAM PLL reference clock
Enable FPGA-to-HPS peripheral PLL reference clock
FPGA-to-HPS SDRAM PLL reference clock frequency: 0.0 MHz
FPGA-to-HPS peripheral PLL reference clock frequency: 0.0 MHz
Peripheral FPGA Clocks
EMAC0 emac0_md_clk clock frequency: 100 MHz
EMAC0 emac0_gtx_clk clock frequency: 100 MHz
EMAC1 emac1_md_clk clock frequency: 100 MHz
EMAC1 emac1_gtx_clk clock frequency: 100 MHz
QSPI qspi_sclk_out clock frequency: 100 MHz
SPIM0 spim0_sclk_out clock frequency: 100 MHz
SPIM1 spim1_sclk_out clock frequency: 100 MHz
I2C0 i2c0_clk clock frequency: 100 MHz
I2C1 i2c1_clk clock frequency: 100 MHz
I2C2 i2c2_clk clock frequency: 100 MHz
I2C3 i2c3_clk clock frequency: 100 MHz
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL... Finish

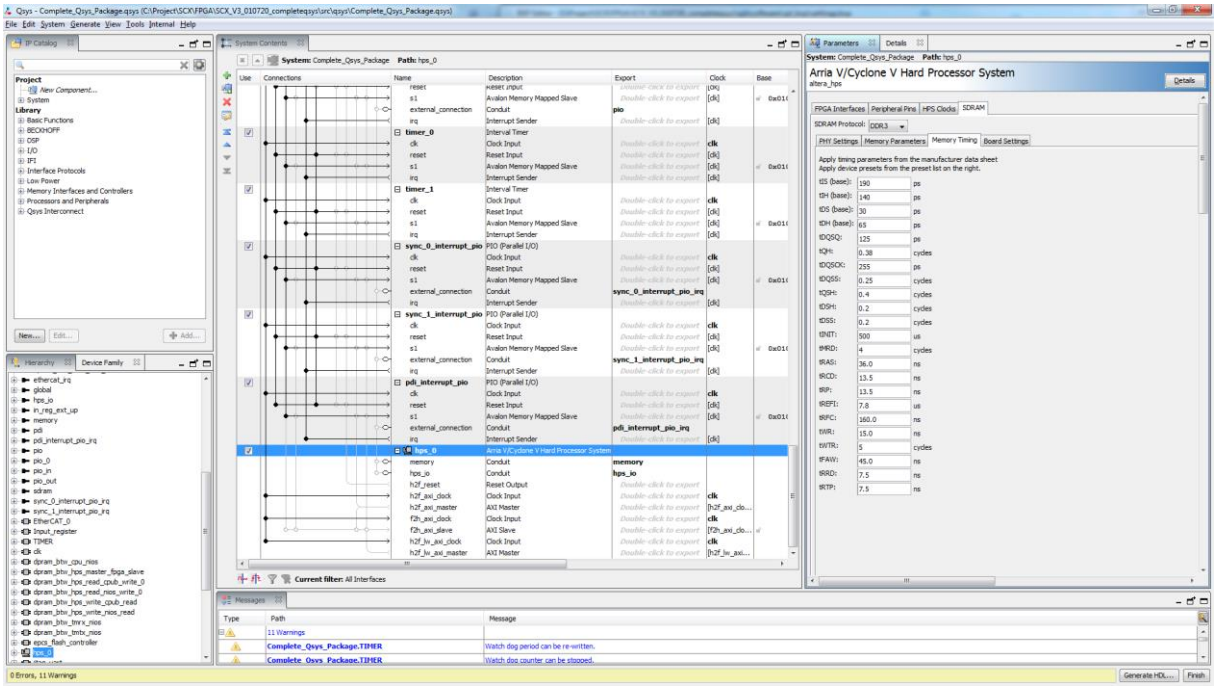

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
DSP
I/O
IP1
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New... Edit... Add...
Hierarchy
Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
reset reset input
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pio
irq Interrupt Sender [clk]
timer_0 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
timer_1 Interval Timer
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
irq Interrupt Sender [clk]
sync_0_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_0_interrupt_pio_irq
irq Interrupt Sender [clk]
sync_1_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit sync_1_interrupt_pio_irq
irq Interrupt Sender [clk]
pdi_interrupt_pio PIO (Parallel I/O)
clk Clock Input clk
reset Reset Input [clk]
s1 Avalon Memory Mapped Slave [clk] 0x01(
external_connection Conduit pdi_interrupt_pio_irq
irq Interrupt Sender [clk]
hps_0 Arria V/Cyclone V Hard Processor System
memory Conduit memory
hps_io Conduit hps_io
h2f_reset Reset Output
h2f_axi_clock Clock Input clk
h2f_axi_master AXI Master [h2f_axi_clo...
f2h_axi_clock Clock Input clk
f2h_axi_slave AXI Slave [f2h_axi_clo...
h2f_lw_axi_clock Clock Input clk
h2f_lw_axi_master AXI Master [h2f_lw_axi...
Current filter: All Interfaces
Parameters Details
System: Complete_Qsys_Package Path: hps_0
Arria V/Cyclone V Hard Processor System
altera_hps
Details
FPGA Interfaces Peripheral Pins HPS Clocks SDRAM
Input Clocks Output Clocks
Clock Sources
Peripheral PLL reference clock source: EOSC1 clock
SDMMC clock source: Peripheral NAND SDMMC clock
NAND clock source: Peripheral NAND SDMMC clock
QSPI clock source: Main QSPI clock
L4 MP clock source: Peripheral base clock
L4 SP clock source: Peripheral base clock
Main PLL Output Clocks - Desired Frequencies
Default MPU clock frequency: 800.0 MHz
Use default MPU clock frequency
MPU clock frequency: 800.0 MHz
L3 MP clock frequency: 200.0 MHz
L3 SP clock frequency: 100.0 MHz
Debug AT clock frequency: 25.0 MHz
Debug clock frequency: 12.5 MHz
Debug trace clock frequency: 25.0 MHz
L4 MP clock frequency: 100.0 MHz
L4 SP clock frequency: 100.0 MHz
Configuration/HPS-to-FPGA user 0 clock frequency: 100.0 MHz
Peripheral PLL Output Clocks - Desired Frequencies
SDMMC clock frequency: 200.0 MHz
NAND clock frequency: 12.5 MHz
QSPI clock frequency: 400.0 MHz
EMAC0 clock frequency: 250.0 MHz
EMAC1 clock frequency: 250.0 MHz
USB clock frequency: 200.0 MHz
SPI clock frequency: 200.0 MHz
CAN0 clock frequency: 100.0 MHz
CAN1 clock frequency: 100.0 MHz
GPIO debounce clock frequency: 32000 Hz
HPS-to-FPGA User Clocks
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL... Finish

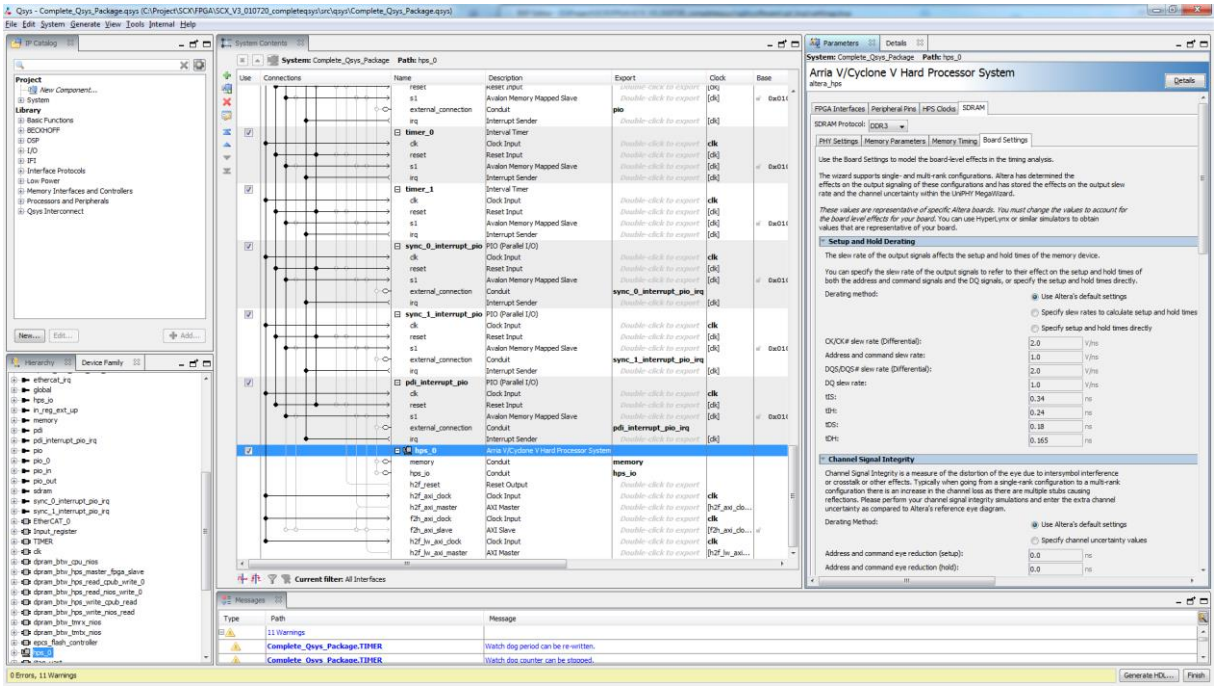

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
DSP
I/O
IFI
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New... Edit... Add...
Hierarchy Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
timer_0 Interval Timer
timer_1 Interval Timer
sync_0_interrupt_pio PIO (Parallel I/O)
sync_1_interrupt_pio PIO (Parallel I/O)
pdi_interrupt_pio PIO (Parallel I/O)
hps_0 Arria V/Cyclone V Hard Processor System
Current filter: All Interfaces
Parameters Details
Arria V/Cyclone V Hard Processor System
altera_hps
Details
Peripheral PLL Output Clocks - Desired Frequencies
HPS-to-FPGA User Clocks
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL... Finish

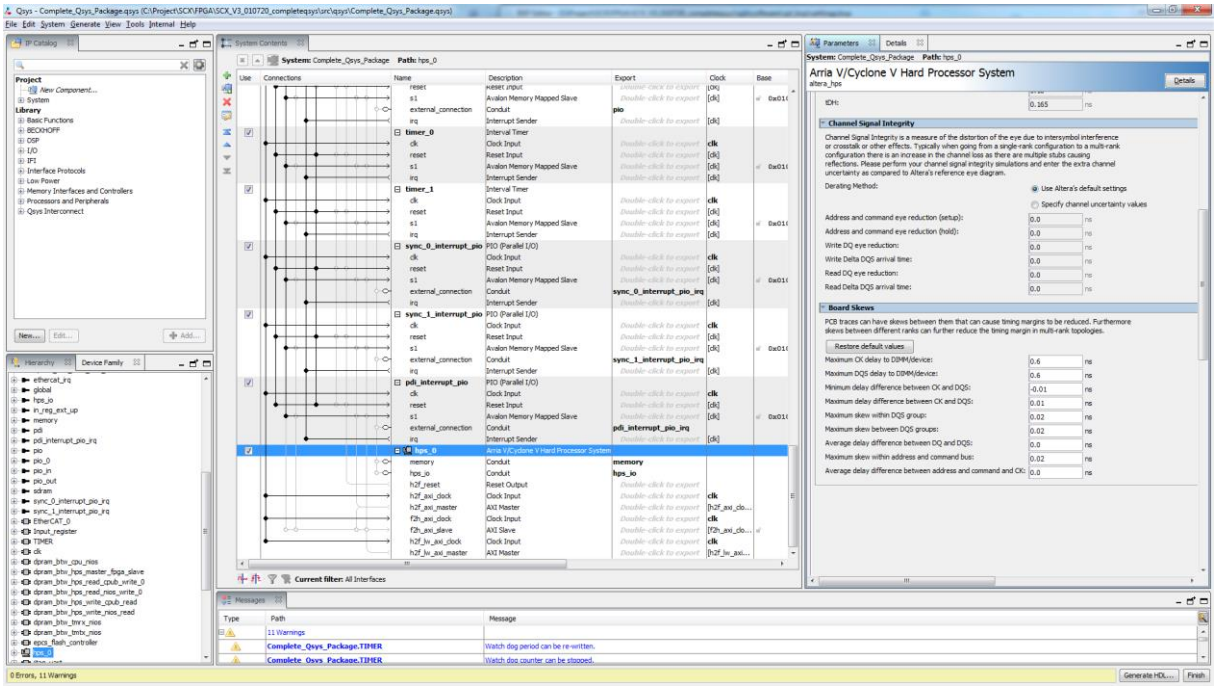

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
Project
New Component...
System
Library
Basic Functions
BECKHOFF
DSP
I/O
IFI
Interface Protocols
Low Power
Memory Interfaces and Controllers
Processors and Peripherals
Qsys Interconnect
New... Edit... Add...
Hierarchy Device Family
System Contents
System: Complete_Qsys_Package Path: hps_0
Use Connections Name Description Export Clock Base
timer_0 Interval Timer
timer_1 Interval Timer
sync_0_interrupt_pio PIO (Parallel I/O)
sync_1_interrupt_pio PIO (Parallel I/O)
pdi_interrupt_pio PIO (Parallel I/O)
hps_0 Arria V/Cyclone V Hard Processor System
Current filter: All Interfaces
Parameters Details
Arria V/Cyclone V Hard Processor System
altera_hps
Details
FPGA Interfaces Peripheral Pins HPS Clocks SDRAM
SDRAM Protocol: DDR3
PHY Settings Memory Parameters Memory Timing Board Settings
Clocks
Memory clock frequency: 400.0 MHz
Use specified frequency instead of calculated frequency
Achieved memory clock frequency: 400.0 MHz
PLL reference clock frequency: 25.0 MHz
Advanced PHY Settings
Supply Voltage: 1.5V DDR3
I/O standard: SSTL-15
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL... Finish


Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
System Contents
System: Complete_Qsys_Package Path: hps_0
Parameters
Details
Arria V/Cyclone V Hard Processor System
altera_hps
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL...
Finish


Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
System Contents
System: Complete_Qsys_Package Path: hps_0
Parameters
Details
Arria V/Cyclone V Hard Processor System
altera_hps
Messages
Type Path Message
11 Warnings
Complete_Qsys_Package.TIMER Watch dog period can be re-written.
Complete_Qsys_Package.TIMER Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL...
Finish

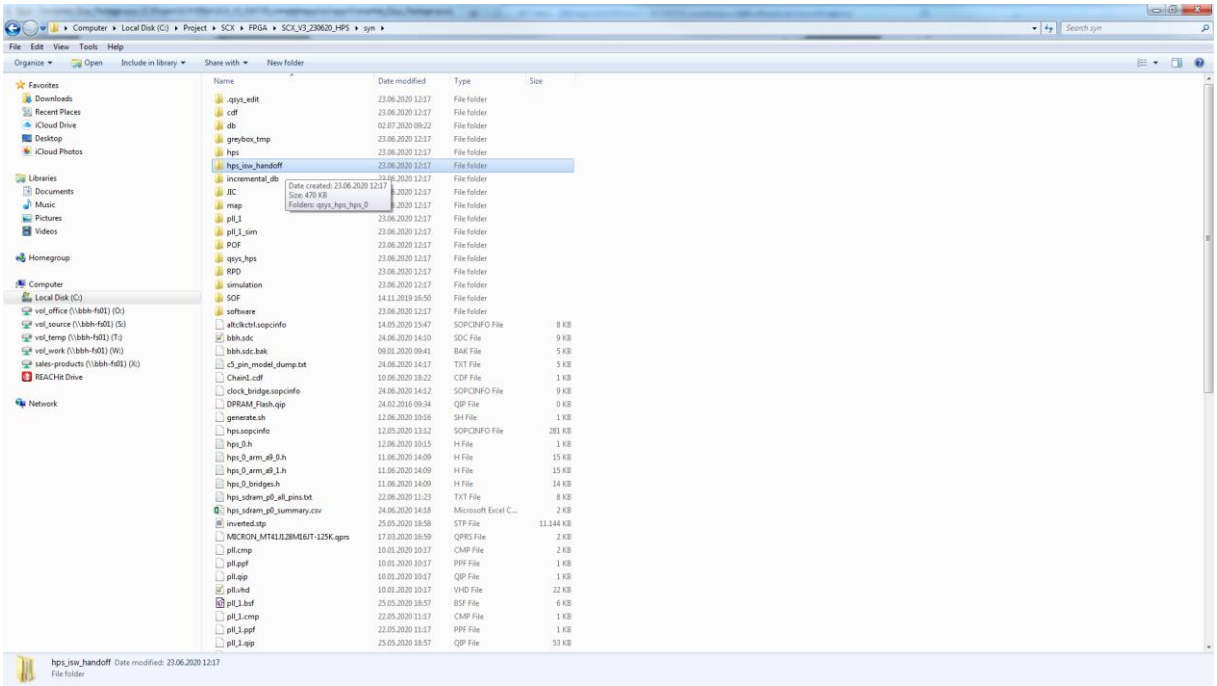

Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
System Contents
System: Complete_Qsys_Package Path: hps_0
Parameters
Details
Arria V/Cyclone V Hard Processor System
altera_hps
Details
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol: DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Apply timing parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
Hierarchy
Device Family
Messages
Type
Path
Message
11 Warnings
Complete_Qsys_Package.TIMER
Watch dog period can be re-written.
Complete_Qsys_Package.TIMER
Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL...
Finish


Qsys - Complete_Qsys_Package.qsys (C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\src\qsys\Complete_Qsys_Package.qsys)
File Edit System Generate View Tools Internal Help
IP Catalog
System Contents
System: Complete_Qsys_Package Path: hps_0
Parameters
Details
Arria V/Cyclone V Hard Processor System
altera_hps
Details
FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol: DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Use the Board Settings to model the board-level effects in the timing analysis.
The wizard supports single- and multi-rank configurations. Altera has determined the effects on the output signaling of these configurations and has stored the effects on the output slew rate and the channel uncertainty within the UniPHY MegaWizard.
These values are representative of specific Altera boards. You must change the values to account for the board level effects for your board. You can use HyperLynx or similar simulators to obtain values that are representative of your board.
Setup and Hold Derating
The slew rate of the output signals affects the setup and hold times of the memory device.
You can specify the slew rate of the output signals to refer to their effect on the setup and hold times of both the address and command signals and the DQ signals, or specify the setup and hold times directly.
Derating method:
Use Altera's default settings
Specify slew rates to calculate setup and hold times
Specify setup and hold times directly
CK/CK# slew rate (Differential):
Address and command slew rate:
DQS/DQS# slew rate (Differential):
DQ slew rate:
tIS:
tIH:
tDS:
tDH:
Channel Signal Integrity
Channel Signal Integrity is a measure of the distortion of the eye due to intersymbol interference or crosstalk or other effects. Typically when going from a single-rank configuration to a multi-rank configuration there is an increase in the channel loss as there are multiple stubs causing reflections. Please perform your channel signal integrity simulations and enter the extra channel uncertainty as compared to Altera's reference eye diagram.
Derating Method:
Use Altera's default settings
Specify channel uncertainty values
Address and command eye reduction (setup):
Address and command eye reduction (hold):
Hierarchy
Device Family
Messages
Type
Path
Message
11 Warnings
Complete_Qsys_Package.TIMER
Watch dog period can be re-written.
Complete_Qsys_Package.TIMER
Watch dog counter can be stopped.
0 Errors, 11 Warnings
Generate HDL...
Finish

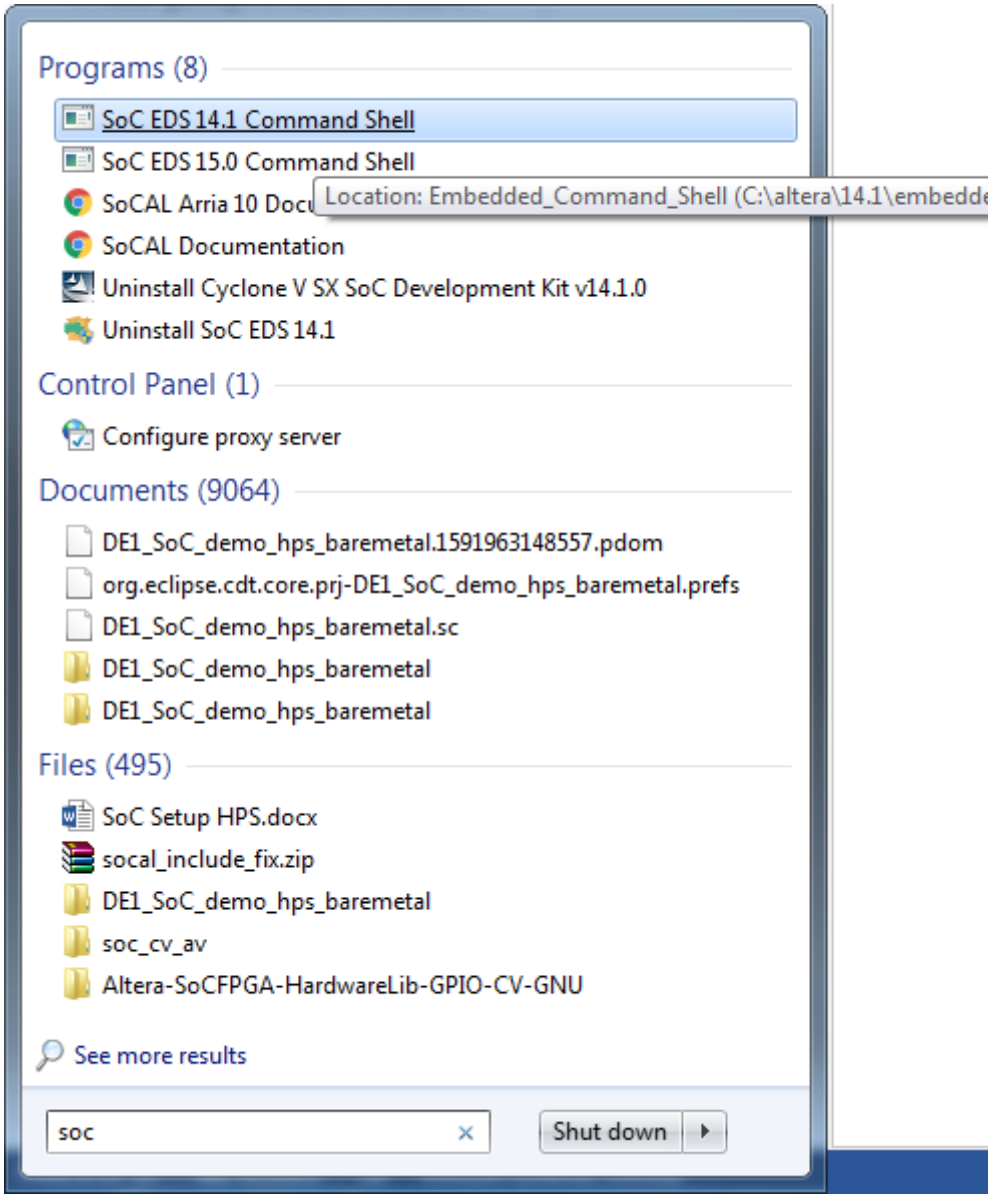


After compiling the FPGA we get the following folder.

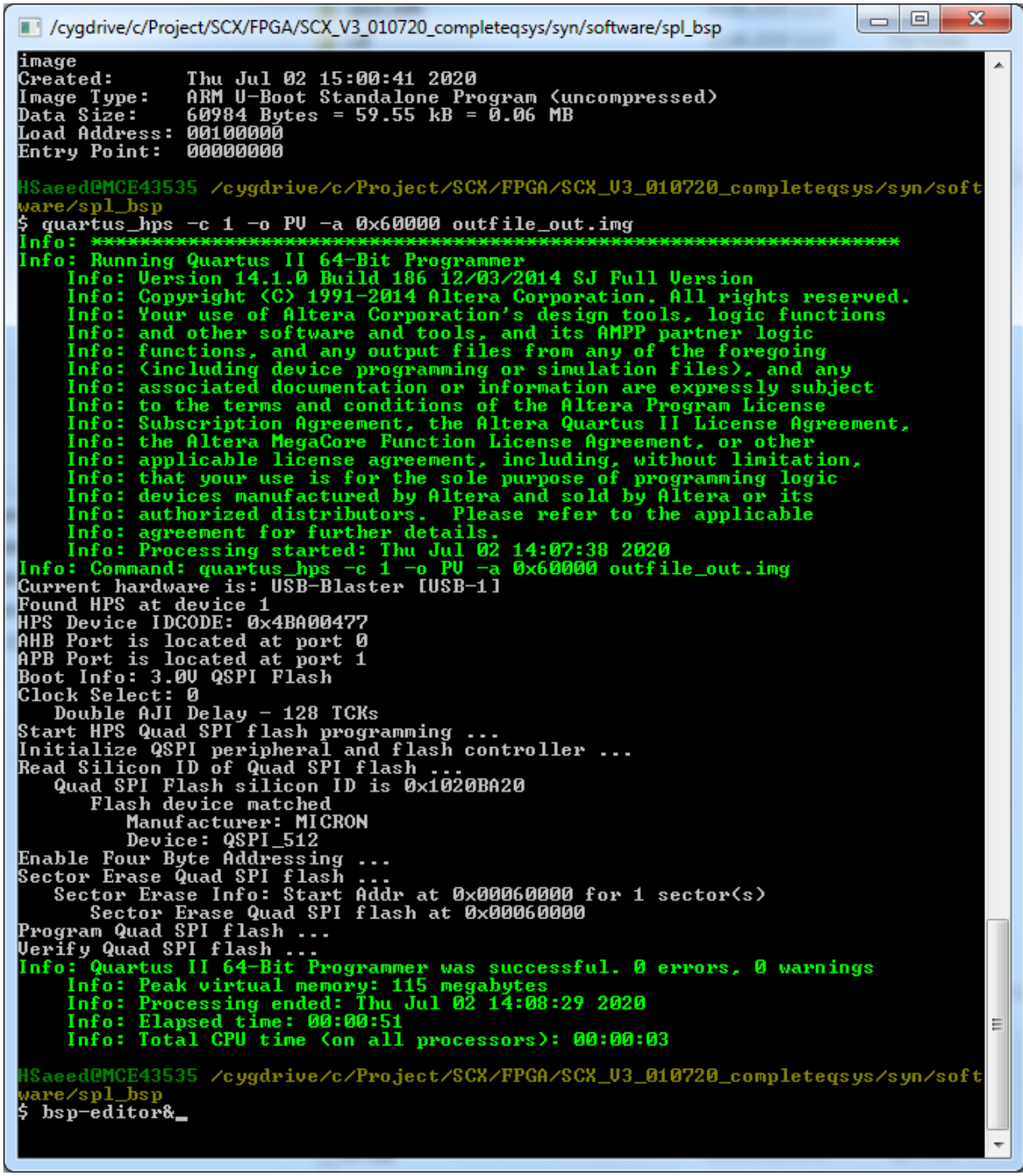
Hps_isw_handoff



2. **Now open SoC command shell**



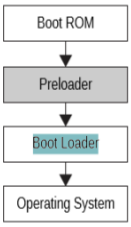
3. **OPEN the bsp-editor**
   By using bsp-editor&



4. **The rules of Preloader**

There are four stages of the hard processor system (HPS) booting process; the preloader is the second stage.

Figure 8-1: Typical Boot Flow



The Preloader configures the HPS component based on the information from the handoff folder, initializes the SDRAM and then loads the next stage of the boot process into SDRAM and passes control to it.

The preloader can directly load your final application for Bare Metal applications and simple RTOSes.

Typically, a boot ROM loads the preloader from a flash device into the on-chip RAM and executes the preloader. The preloader can also be executed directly from the FPGAmemory.

5. **Handoff Files (this files is generated by Qsys)**

Hardware Handoff Files

Use the Qsys system integration tool in the Quartus II software to generate a set of handoff files containing the hardware information required by the preloader.

The handoff files from the Qsys compilation are located in the *<quartus project directory>*/**hps_isw_handoff**/**<hps entity name>** directory (where **hps entity name** is the HPS component name in Qsys).

Note: You must update the hardware handoff files and regenerate the preloader support package each time a hardeare change impacts the HPS, such as after pin multiplexing or pin assignment.

1. **The preloader can be generated by using the bsp-editor (please see the next 2 screen shot)**

In this example, you will re-create the **Preloader** in the folder *<SoC EDS installation directory>***/examples/hardware/cv_soc_devkit_ghrd/software/spl_bsp**.

The screen snapshots presented in this section were created using the Windows version of SoC EDS, but the example can be run in a very similar way on a Linux host PC.

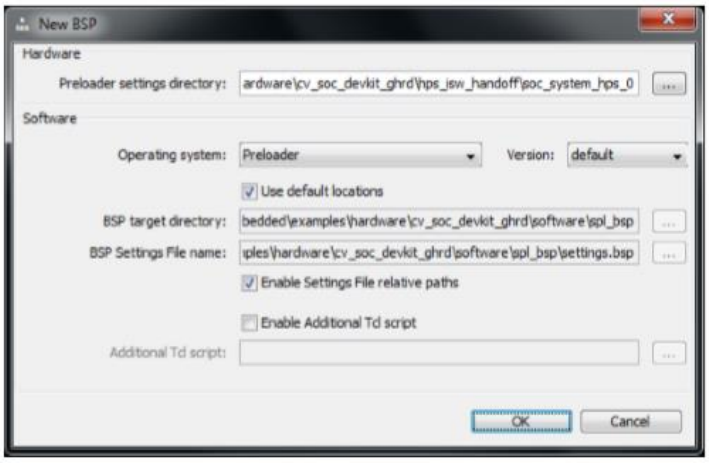
The steps to create the Preloader are:

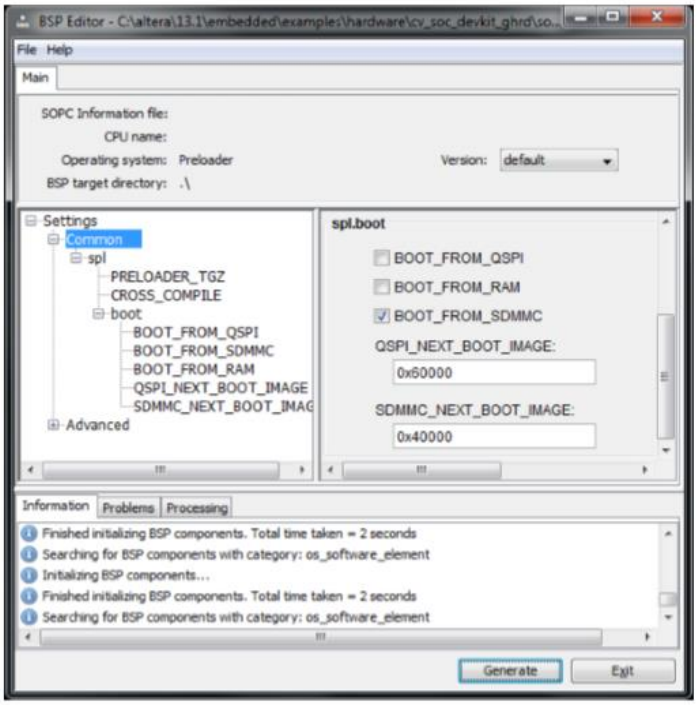
1. Start an Embedded Command Shell by executing *<SoC EDS installation directory>***\Embedded_Command_Shell.bat**.
2. Run the command, `bsp-editor`. The **BSP Editor** dialog box appears.

   Note: The tool that generates a preloader support package is the BSP Editor, also used to generate BSPs for other Altera products.

3. Select **File > New BSP**.The **New BSP** dialog opens.
4. Click the "..." button to browse for the Preloader settings directory in the **New BSP** dialog box.
5. Browse **<SoCEDS folder>\examples\hardware\cv_soc_devkit_ghrd\hps_isw_handoff\soc_system_hps_0** for the hardware handoff folder. The rest of the Preloader settings are populated automatically.

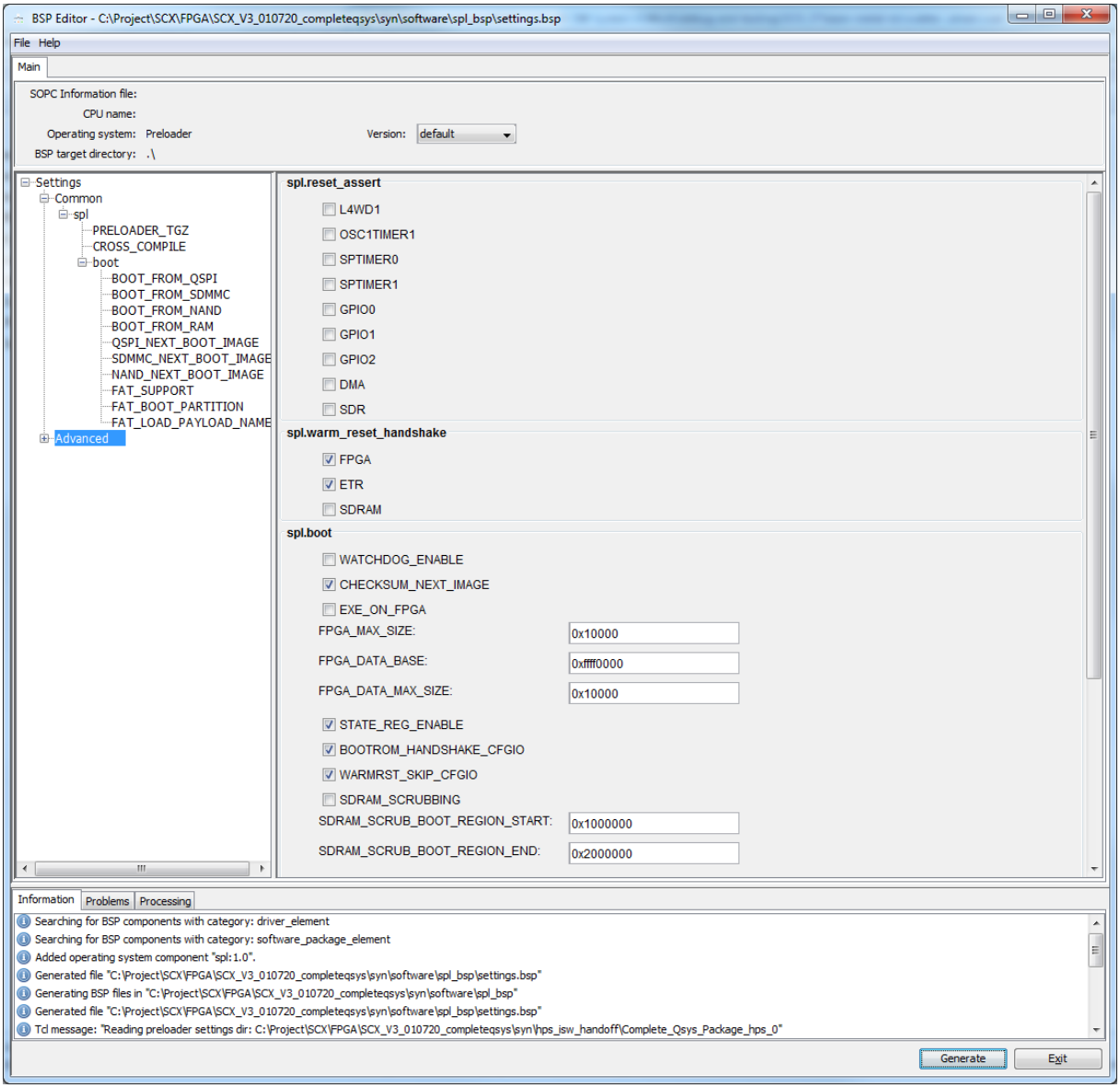
Figure 5-2: Populated Options in the New BSP window

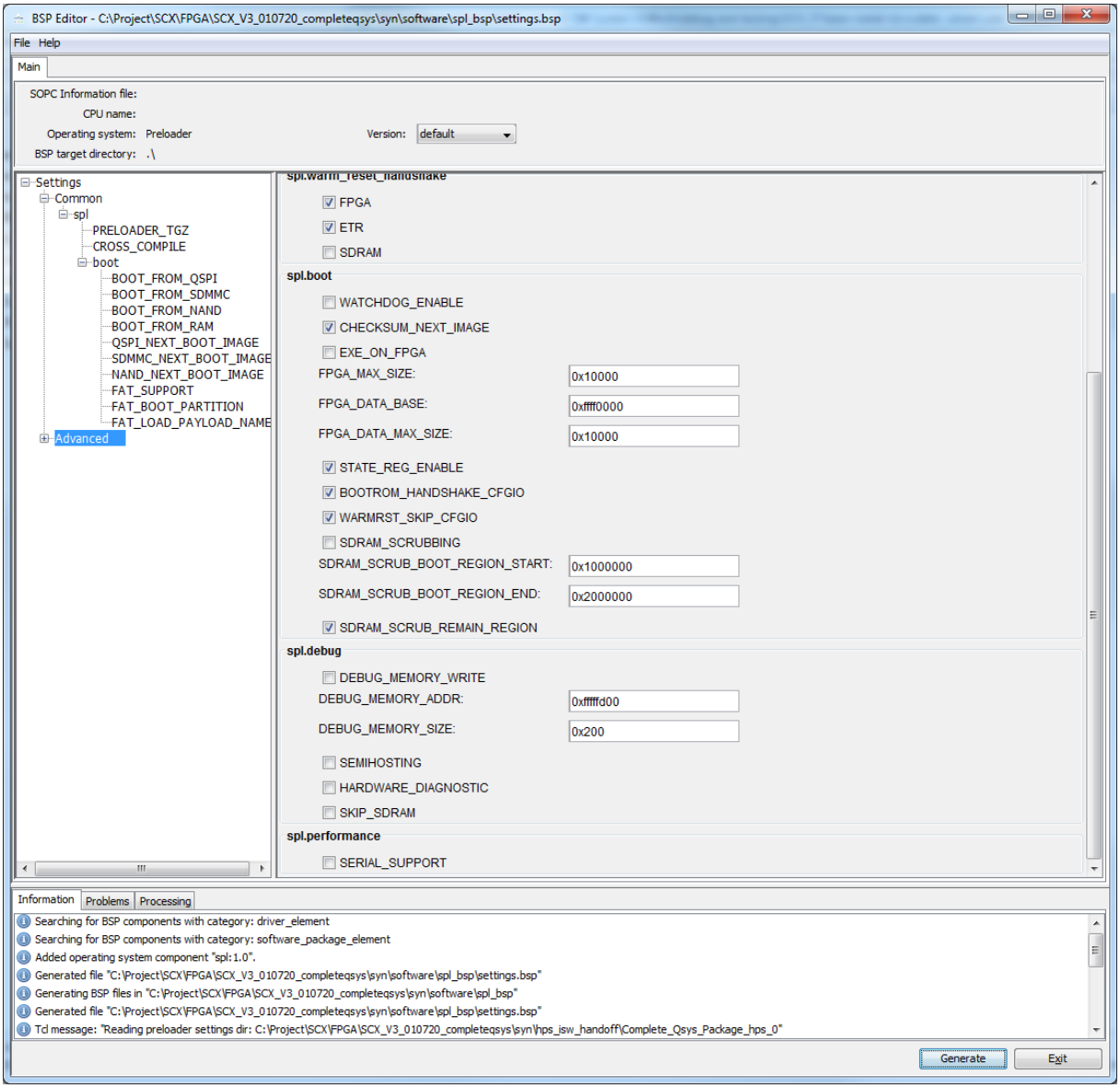




7. Click **Generate** in the **BSP Editor** dialog box to generate the Preloader files.
8. Click **Exit** in the **BSP Editor** dialog box to exit the application.
9. In the Embedded Command Shell, execute the following commands:
   - cd <*SoC EDS installation directory*>**\examples\hardware\cv_soc_devkit_ghrd\software\spl_bsp**
   - **make**
10. The Preloader is ready to be used in the above folder. Some of the more relevant files that are created:
    - **preloader-mkpimage.bin** – Preloader with the proper header to be loaded by BootROM
    - **uboot-socfpga \ spl \ u-boot- spl** – Preloader ELF file, to be used for debugging purposes
    - **uboot-socfpga \tools\mkimage.exe** – Utility to add the header needed by the Preloader to recognize the next boot stage

2. see the following boot loader settings for booting from qspi


BSP Editor - C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\syn\software\spl_bsp\settings.bsp
File Help
Main
SOPC Information file:
CPU name:
Operating system: Preloader
Version: default
BSP target directory: .\
Settings
Common
spl
PRELOADER_TGZ
CROSS_COMPILE
boot
BOOT_FROM_QSPI
BOOT_FROM_SDMMC
BOOT_FROM_NAND
BOOT_FROM_RAM
QSPI_NEXT_BOOT_IMAGE
SDMMC_NEXT_BOOT_IMAGE
NAND_NEXT_BOOT_IMAGE
FAT_SUPPORT
FAT_BOOT_PARTITION
FAT_LOAD_PAYLOAD_NAME
Advanced
spl.reset_assert
L4WD1
OSC1TIMER1
SPTIMER0
SPTIMER1
GPIO0
GPIO1
GPIO2
DMA
SDR
spl.warm_reset_handshake
FPGA
ETR
SDRAM
spl.boot
WATCHDOG_ENABLE
CHECKSUM_NEXT_IMAGE
EXE_ON_FPGA
FPGA_MAX_SIZE: 0x10000
FPGA_DATA_BASE: 0xffff0000
FPGA_DATA_MAX_SIZE: 0x10000
STATE_REG_ENABLE
BOOTROM_HANDSHAKE_CFGIO
WARMRST_SKIP_CFGIO
SDRAM_SCRUBBING
SDRAM_SCRUB_BOOT_REGION_START: 0x1000000
SDRAM_SCRUB_BOOT_REGION_END: 0x2000000
Information
Problems
Processing
Searching for BSP components with category: driver_element
Searching for BSP components with category: software_package_element
Added operating system component "spl:1.0".
Generated file "C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\syn\software\spl_bsp\settings.bsp"
Generating BSP files in "C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\syn\software\spl_bsp"
Generated file "C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\syn\software\spl_bsp\settings.bsp"
Tcl message: "Reading preloader settings dir: C:\Project\SCX\FPGA\SCX_V3_010720_completeqsys\syn\hps_isw_handoff\Complete_Qsys_Package_hps_0"
Generate
Exit

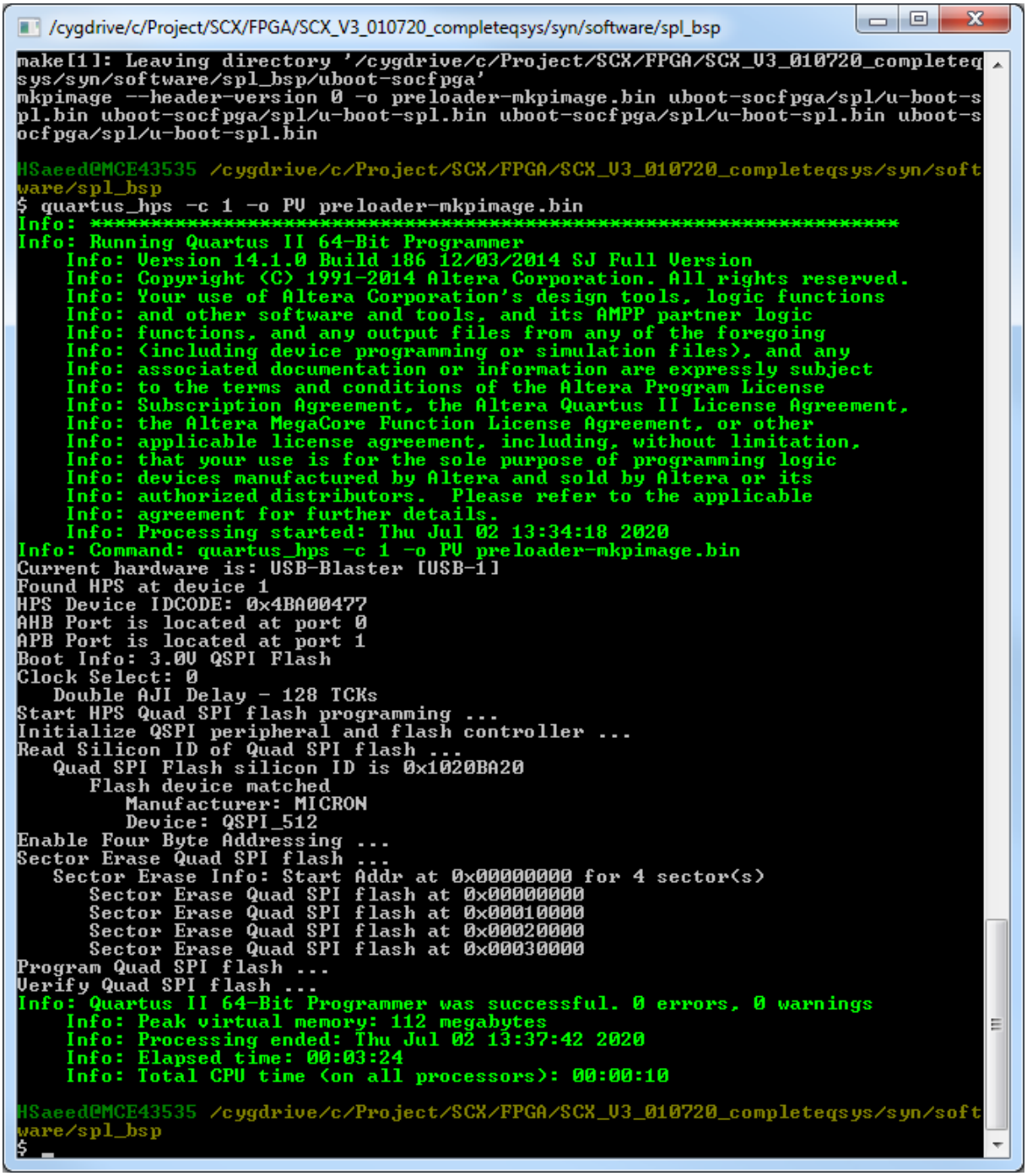


3. **For the debugging, the preloader ELF file (u-boot-spl) should be imported to the DS-5 debugger**

after generate the preloader, use the embedded shall to generate the preloader ELF file.

First, specify the path of preloader (cd: …..) that it is already generated, then write “make clean” or “make clean-all”, then “make uboot”.

4. **Flash this generated preloader-mkpimage.bin to QSPI flash using the following command**



5. **Add the scatter file to your DS-5 project. The scatter file which we are using will support the interrupts too. The interrupt is also called from the DDR3 memory. It makes no difference in the time If we use the onchip scatter file for interrupt or the DDR3 scatter file for the interrupt. The problem to use onchip scatter with DDR3 scatter makes a very big out.bin file.**

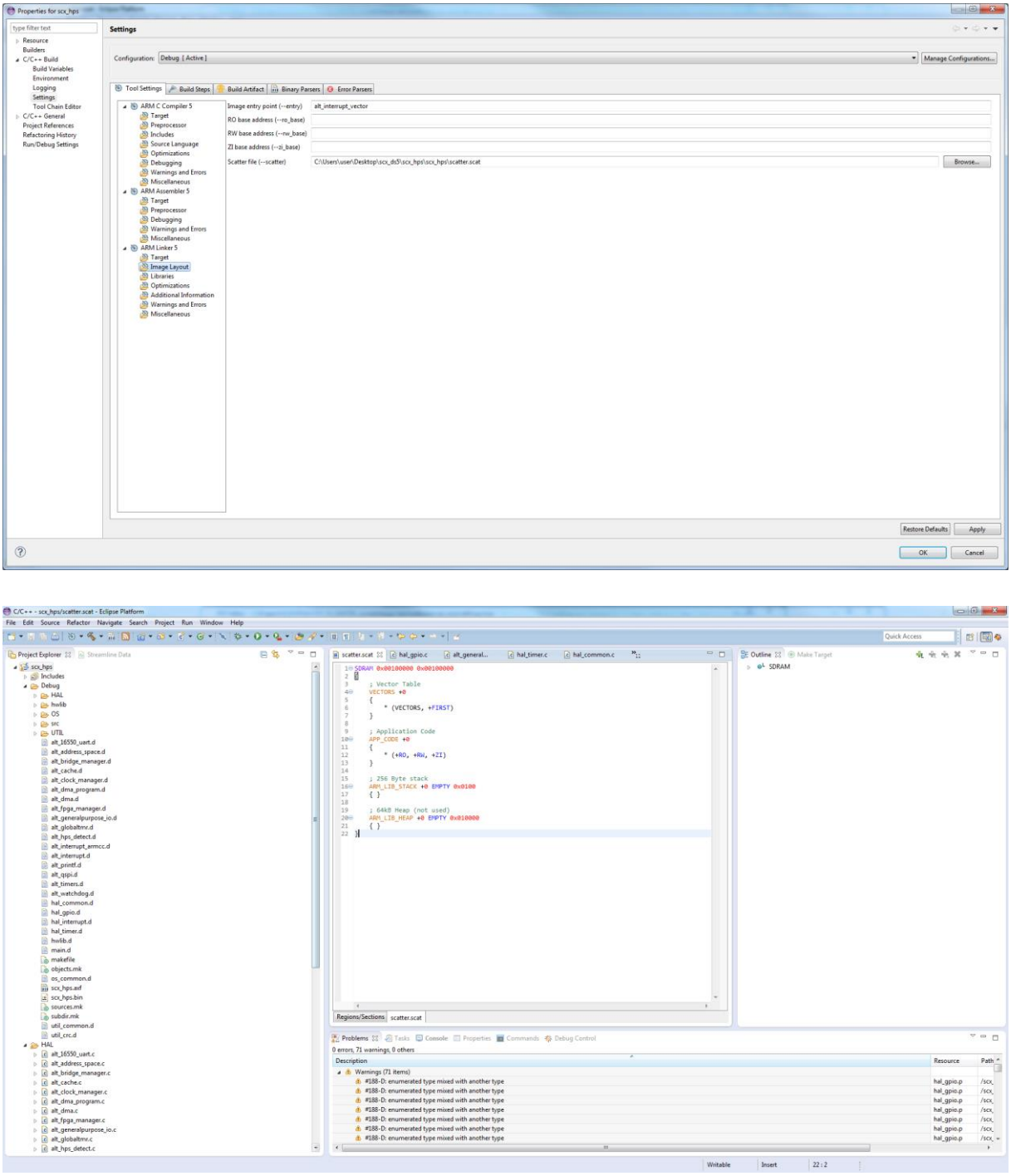


Abbildung 1: DDR3 interrupt

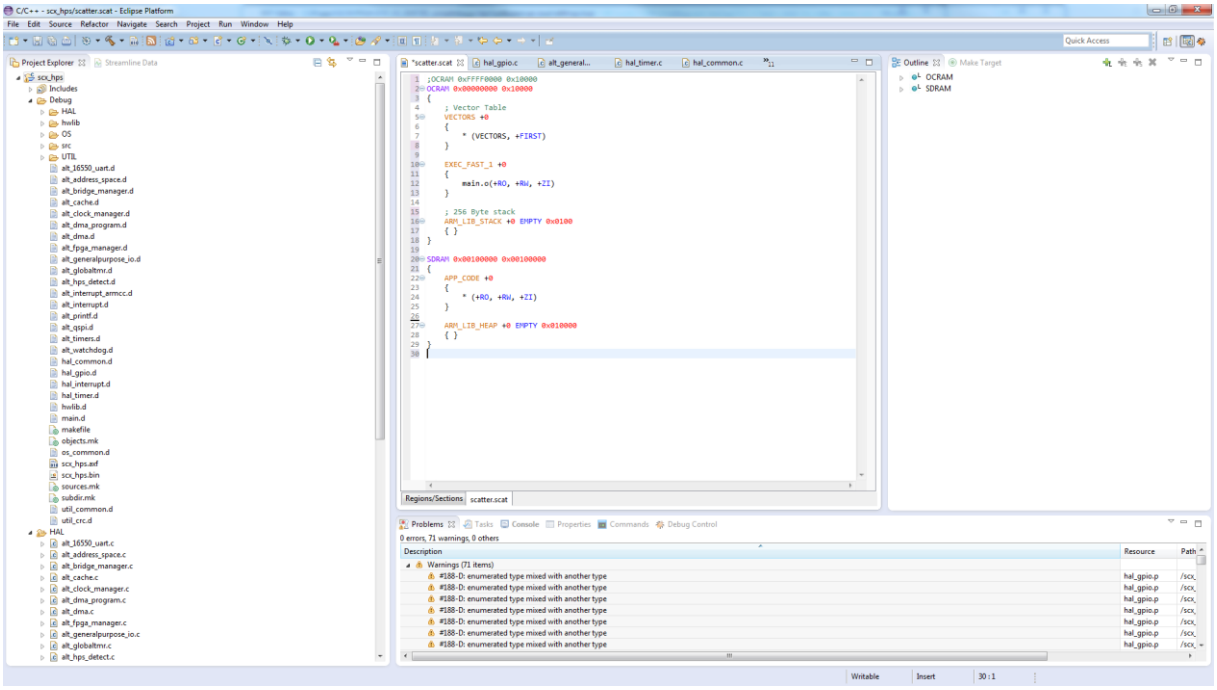
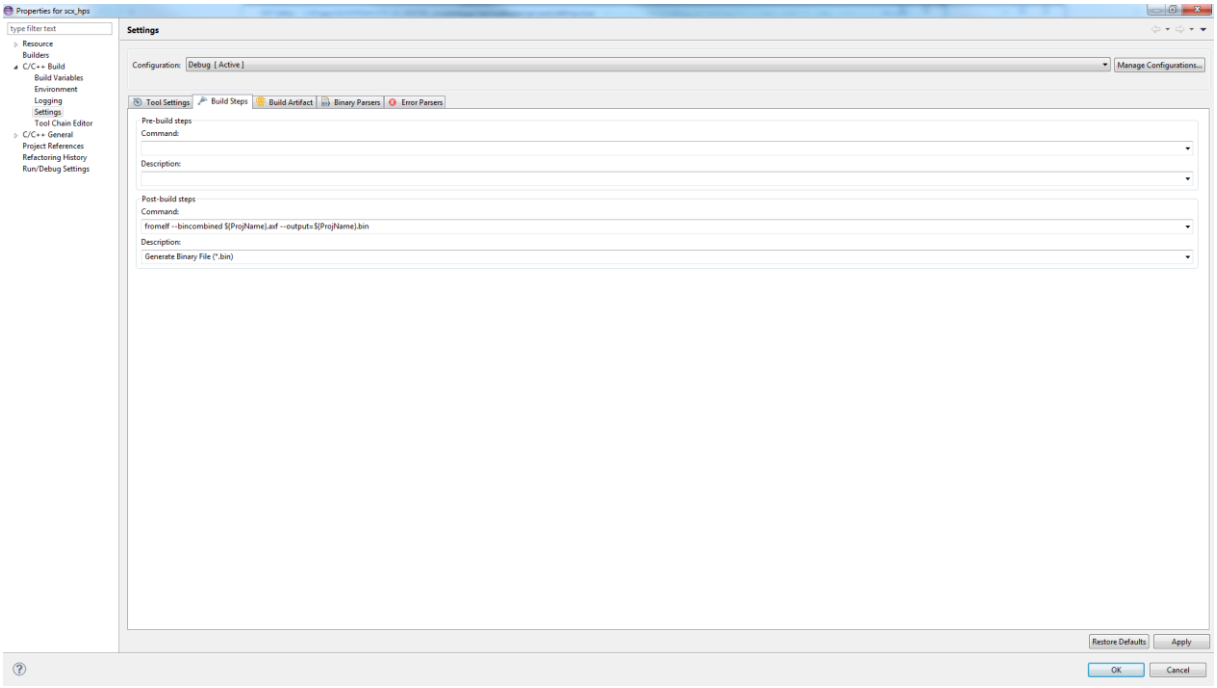


Abbildung 2: onchip for interrupt and the remaining program from DDR3

6. **In the DS-5 the project settings use the fromelf as shown below this will generate the binary file after you compile the baremetal code.**

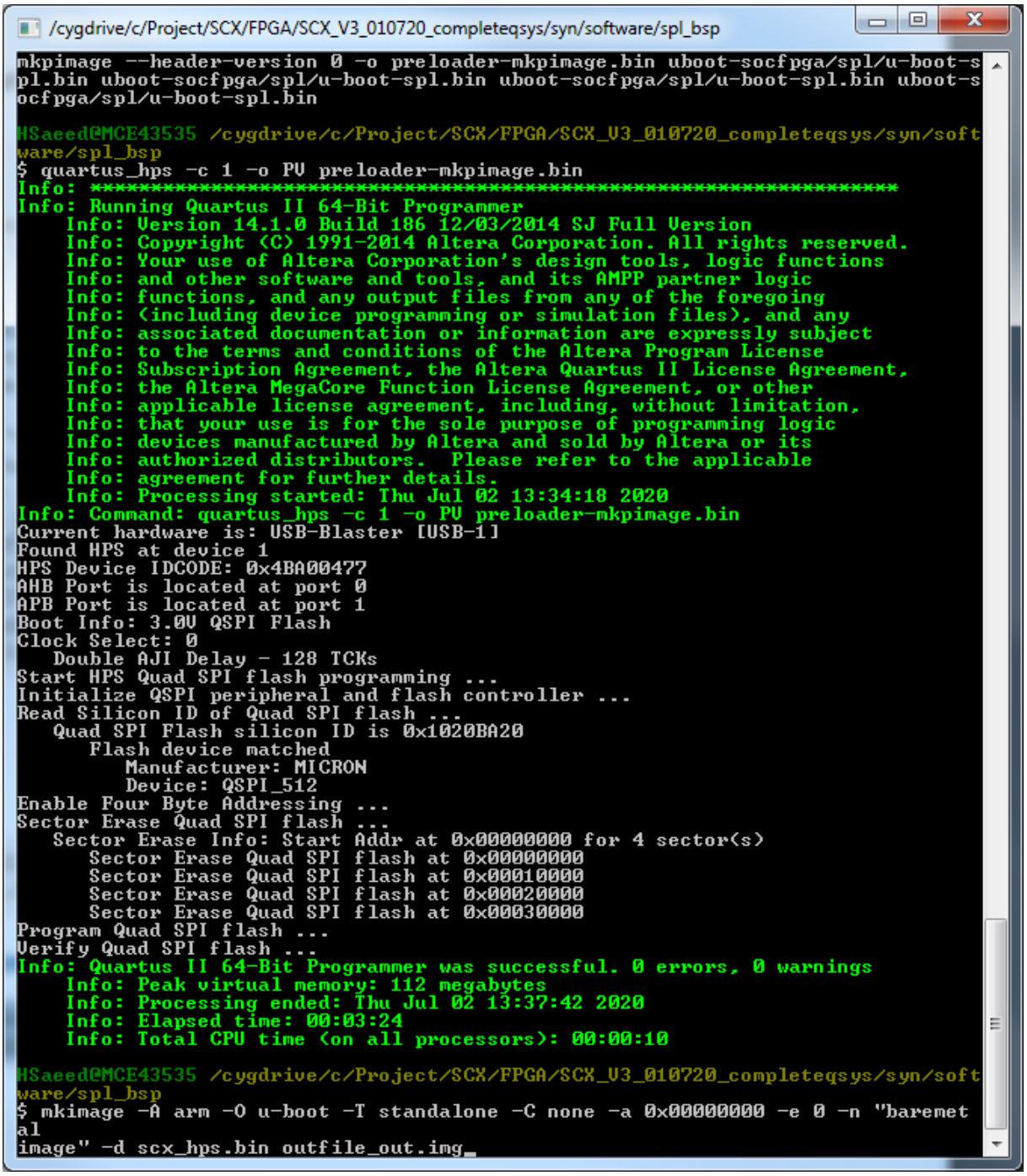


7. **After getting the out.bin file add the boot header using the following command**

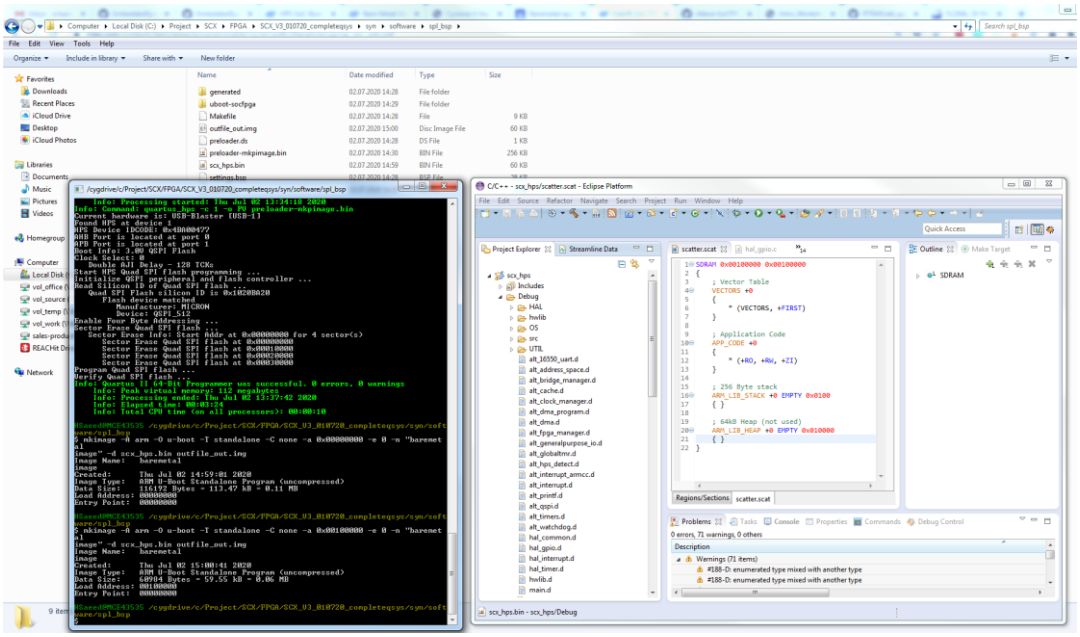
mkimage -A arm -O u-boot -T standalone -C none -a 0x02100000 -e 0 -n "baremetal image" -d hello_world.bin hello_world.img

here “0x02100000” depends on the scatter file used in the project

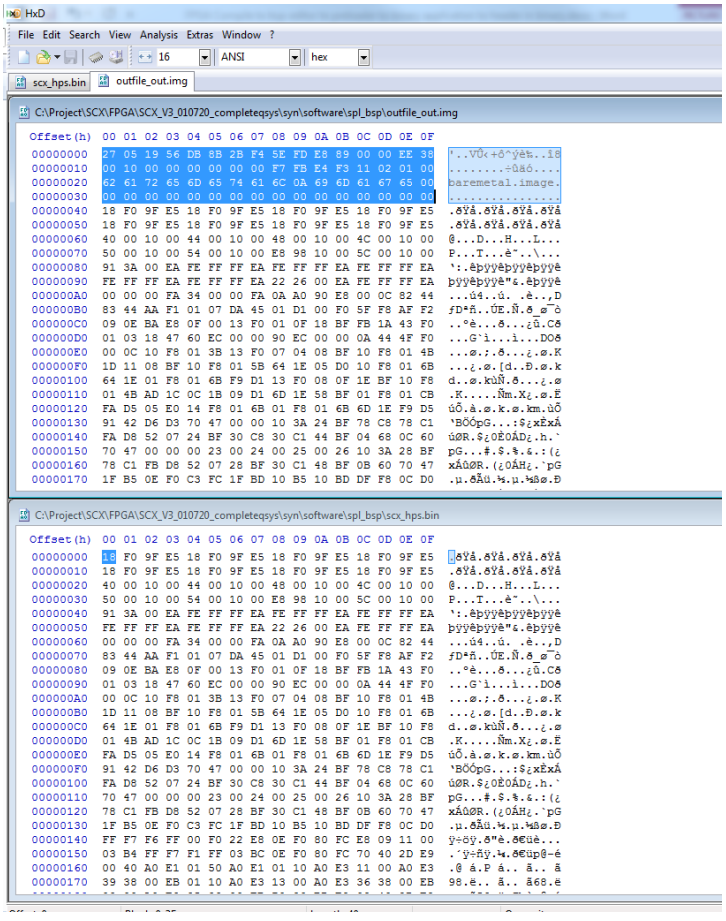
I used the following command for the scatter file shown in Abbildung 2



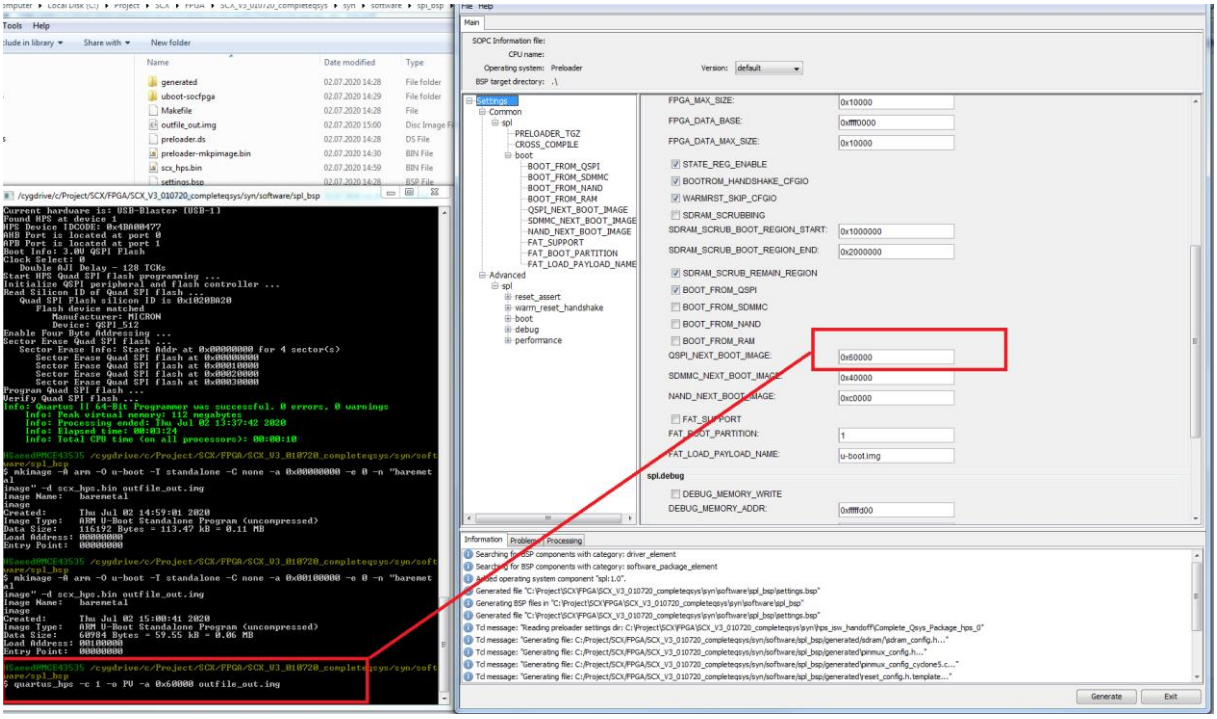
8. **After executing command for the shown scatter file will add the header information and generate outfile_out.img**



The following header is added in the binary file



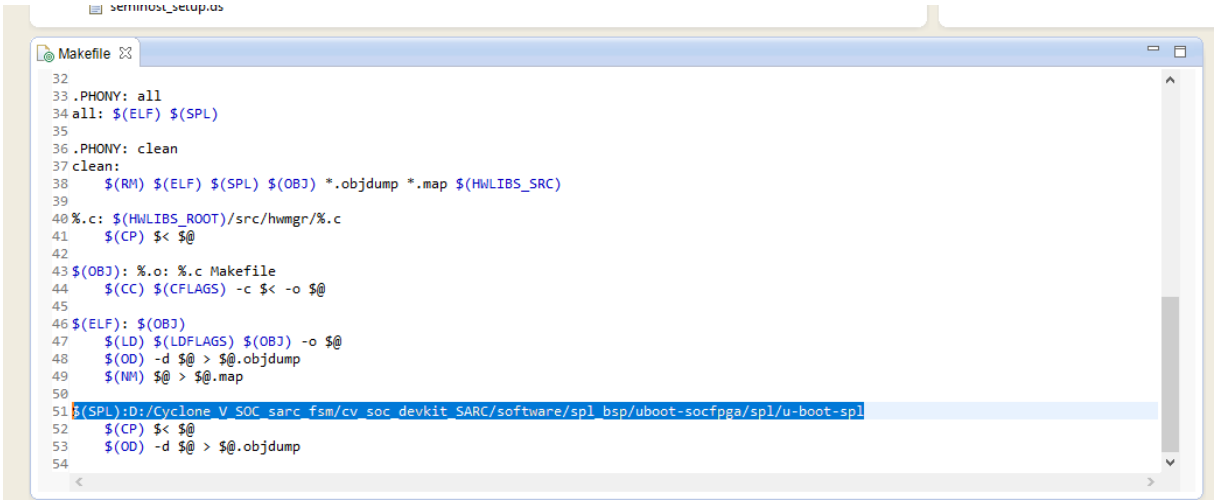
9. **Flash this image which we just created on the QSPI using the following command.**



Power on the device and it should start up with your application program.

Extra information if needed.

The preloader ELF file is now generated and can be imported to the DS-5 debugger through a makefile (available in my DS-5 project).



You need then to load the (.svd) file to have the features of accessing to soft IP register.

This file is also generated after the Qsys is compiled. To load this file **(.svd)** to DS-debugger, open **(Debugger configuration -- > files)** , and load the **(.svd file)** which located in **synthesis folder** (please see the next screen shot).

The following handoff files are created when the hardware project is compiled:

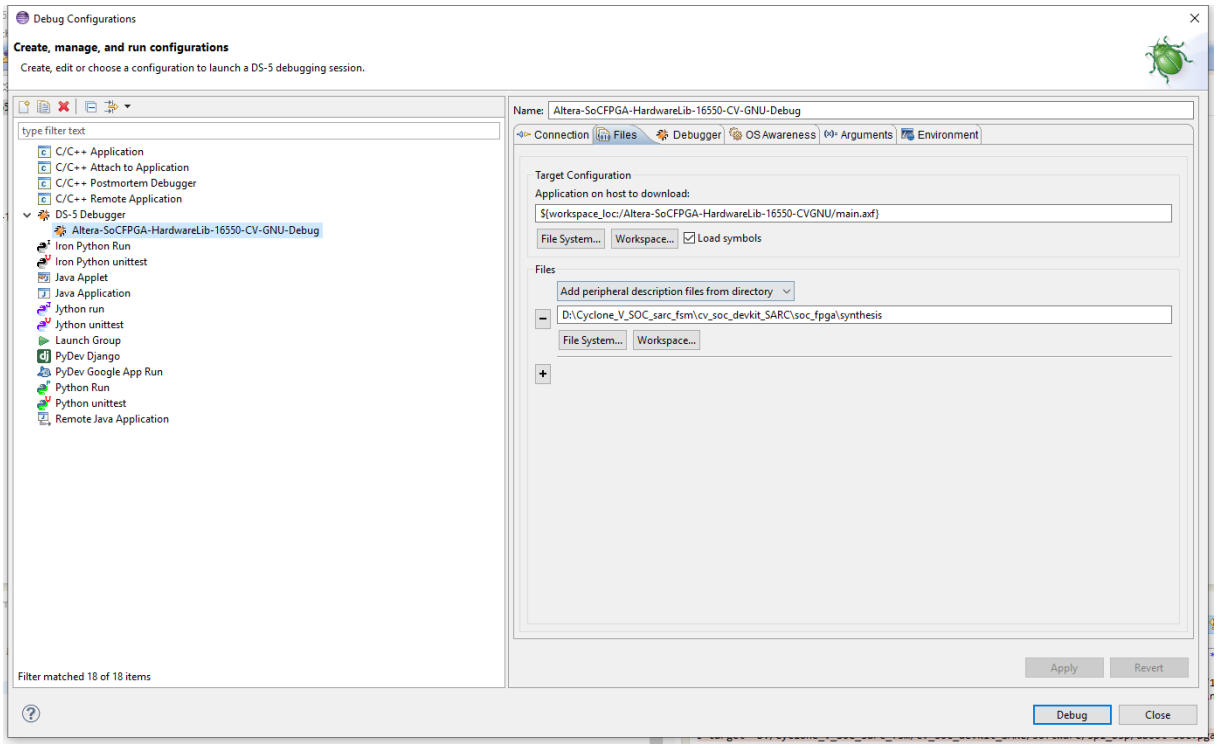
- **Handoff** folder – contains information about how the HPS component is configured, including things like which peripherals are enabled, the pin muxing and IOCSR settings, memory parameters, etc
- **.svd** file – contains descriptions of the HPS registers and of the soft IP registers on FPGA side
- **.sopcinfo** file – contains a description of the whole system

The handoff folder is used by the preloader generator to create the Preloader.

The **.svd** file contains the description of the registers of the HPS peripheral registers and registers for soft IP components in the FPGA portion of the SoC. This file is used by the ARM DS-5 Debugger to allow these registers to be inspected and modified by the user.

SOPC Information (**.sopcinfo**) file, containing a description of the entire system, is used by the Device Tree Generator to create the Device Tree used by the Linux kernel.

Note: The soft IP register descriptions are not generated for all soft IP cores.

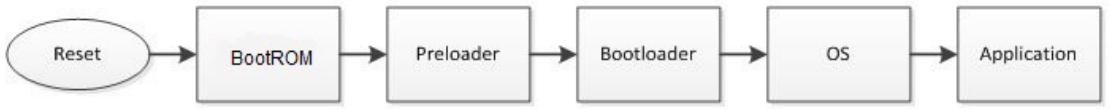


Loading the . SVD file

Additional information about Boot ROM, Preloader, and BootLoader

The following figure depicts the typical boot flow:

Figure 1. Typical Boot Flow



Boot ROM

The HPS boot process starts when the processor is released from reset, and jumps to the reset vector address, located in the Boot ROM address space.

Typically, the main responsibilities of the Boot ROM are:

- Detect the selected boot source
- Perform minimal HPS initialization
- Load the next boot stage (typically the Preloader) from Flash to OCRAM and jump to it

The behavior of the Boot ROM is influenced by the BSEL and CSEL options, and also by the registers in System Manger (for RAM boot) as shown later in the document.

For the scenarios where the next boot stage is located in Flash, the Boot ROM can use up to four different images:

Preloader

Typically, the main responsibilities of the Preloader are:

- Perform additional HPS initialization
- Bring up SDRAM
- Load the next boot stage from Flash to SDRAM and jump to it

Currently, two different Preloader options are available:

- SPL – part of U-Boot. Provided with SoC EDS under GPL (Open Source) License
- MPL – provided with SoC EDS as an example using the HWLibs (Altera bare-metal libraries). Uses BSD license.

Note: The Preloader requires a special header to be placed at the beginning of the next stage boot image. Also, the header contains a CRC value used to validate the image. The header can be attached to an image by using the `mkimage` utility that is included with the SoC EDS.

Bootloader

The Bootloader has typical responsibilities that are similar with the Preloader, except it does not need to bring up SDRAM.

Because the Bootloader is already residing in SDRAM, it is not limited by the size of the OCRAM. Therefore, it can provide a lot of features, such as network stack support.