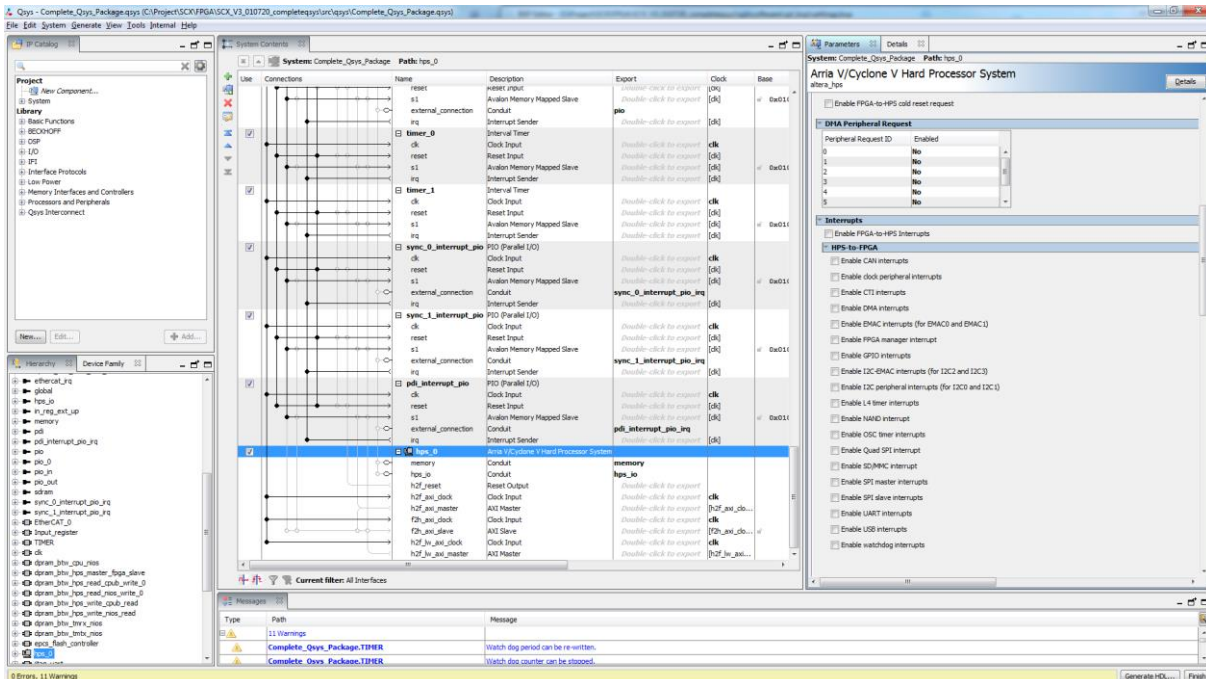
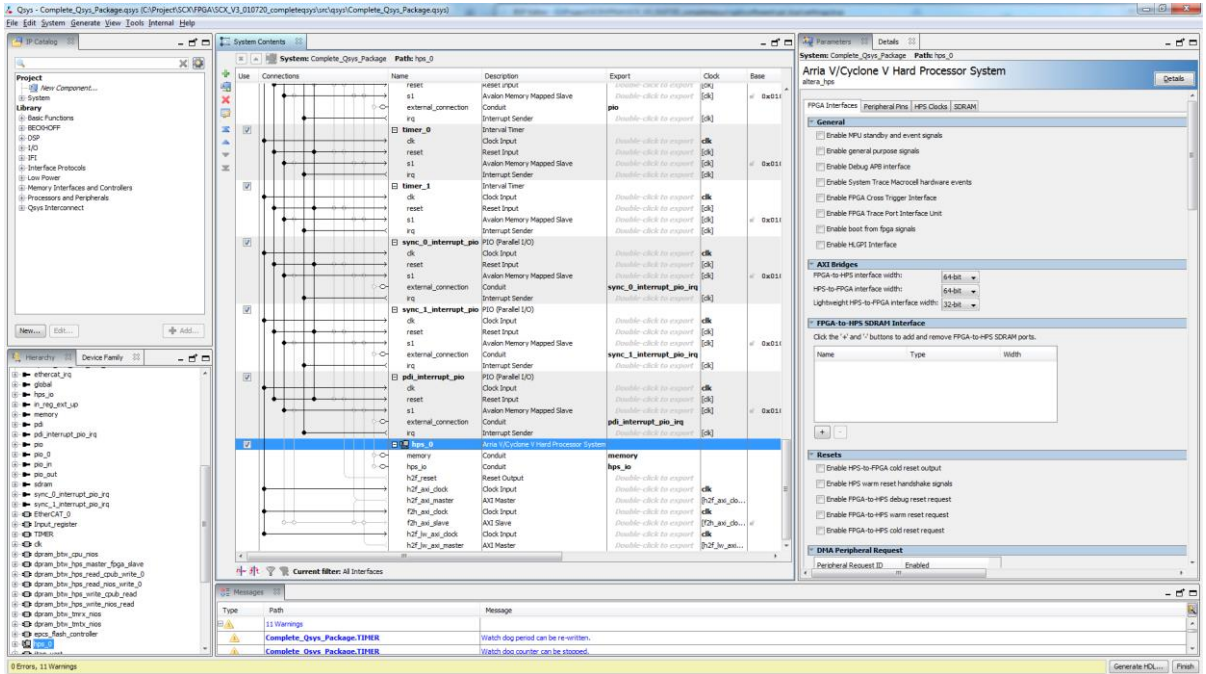


1. HPS in the qsys and its settings

We are using almost empty hps with only basic settings for the DDR3. Following is the settings of the QSPI and the HPS in QSYS project.



As we are flashing from QSPI we need only QSPI flash controller

Qsys - Complete_Qsys_Package.qsys (C:\Project\Qsys\FPGA\SCX_V3_010720_completeqsys\qsys\Complete_Qsys_Package.qsys)

File Edit System Generate View Tools Internal Help

Project

- New Component...
- System
- Block Functions
- BECONOFF
- DSP
- LD
- IP
- Interface Protocols
- Low Power
- Memory Interfaces and Controllers
- Processors and Peripherals
- Qsys Interconnect

System Contents

System: Complete_Qsys_Package Path: top_0

Name	Description	Export	Clock	Base
reset	Reset Input	reset	clk	Ea011
external_connection	Conduit	external_connection	clk	Ea011
timer_0	Interval Timer	timer_0	clk	Ea011
timer_1	Interval Timer	timer_1	clk	Ea011
sync_0_interrupt_pio	PIO (Parallel IO)	sync_0_interrupt_pio	clk	Ea011
sync_1_interrupt_pio	PIO (Parallel IO)	sync_1_interrupt_pio	clk	Ea011
pio_interrupt_pio	PIO (Parallel IO)	pio_interrupt_pio	clk	Ea011
top_0	Arria V/Cyclone V Hard Processor System	memory	clk	Ea011

Parameters

System: Complete_Qsys_Package Path: top_0

Arria V/Cyclone V Hard Processor System

Peripherals: IPFS Clouds | SDRAM

- Ethernet Media Access Controller**
 - EMAC0 pins: Unused
 - EMAC1 pins: N/A
 - EMAC2 pins: N/A
- NAND Flash Controller**
 - NAND pins: Unused
 - NAND mode: N/A
- Quad SPI Flash Controller**
 - QSPI pins: JPS LIO Set 0
 - QSPI mode: 1SS
- SD/HPC Controller**
 - SDIO pins: Unused
 - SDIO mode: N/A
- USB Controllers**
 - USB0 pins: Unused
 - USB0 PHY interface mode: N/A
 - USB1 pins: Unused
 - USB1 PHY interface mode: N/A
- SPI Controllers**
 - SP10 pins: Unused
 - SP10 mode: N/A
 - SP11 pins: Unused
 - SP11 mode: N/A
 - SP12 pins: Unused
 - SP12 mode: N/A
 - SP13 pins: Unused
 - SP13 mode: N/A
- UART Controllers**
 - UART0 pins: Unused
 - UART0 mode: N/A
 - UART1 pins: N/A

Messages

Type	Path	Message
Warning	Complete_Qsys_Package.TPHER	Watch dog period can be re-written.
Warning	Complete_Qsys_Package.TPHER	Watch dog counter can be stopped.

0 Errors, 11 Warnings

Generate HDL... Refresh

Qsys - Complete_Qsys_Package.qsys (C:\Project\Qsys\FPGA\SCX_V3_010720_completeqsys\qsys\Complete_Qsys_Package.qsys)

File Edit System Generate View Tools Internal Help

Project

- New Component...
- System
- Block Functions
- BECONOFF
- DSP
- LD
- IP
- Interface Protocols
- Low Power
- Memory Interfaces and Controllers
- Processors and Peripherals
- Qsys Interconnect

System Contents

System: Complete_Qsys_Package Path: top_0

Name	Description	Export	Clock	Base
reset	Reset Input	reset	clk	Ea011
external_connection	Conduit	external_connection	clk	Ea011
timer_0	Interval Timer	timer_0	clk	Ea011
timer_1	Interval Timer	timer_1	clk	Ea011
sync_0_interrupt_pio	PIO (Parallel IO)	sync_0_interrupt_pio	clk	Ea011
sync_1_interrupt_pio	PIO (Parallel IO)	sync_1_interrupt_pio	clk	Ea011
pio_interrupt_pio	PIO (Parallel IO)	pio_interrupt_pio	clk	Ea011
top_0	Arria V/Cyclone V Hard Processor System	memory	clk	Ea011

Parameters

System: Complete_Qsys_Package Path: top_0

Arria V/Cyclone V Hard Processor System

Peripherals: IPFS Clouds | SDRAM

- UART Controllers**
 - UART0 pins: Unused
 - UART0 mode: N/A
 - UART1 pins: Unused
 - UART1 mode: N/A
- I2C Controllers**
 - I2C0 pins: Unused
 - I2C1 pins: Unused
 - I2C1 mode: N/A
 - I2C2 pins: Unused
 - I2C2 mode: N/A
 - I2C3 pins: Unused
 - I2C3 mode: N/A
- CAN Controllers**
 - CAN0 pins: Unused
 - CAN0 mode: N/A
 - CAN1 pins: Unused
 - CAN1 mode: N/A
- Trace Port Interface Unit**
 - TRACE pins: Unused
 - TRACE mode: N/A
- Peripherals Hex Table**

ROM0_T0_CLK	0001 01 (G40)
ROM0_T000	0001 01 (G40)
ROM0_T101	0001 02 (G40)
ROM0_T102	0001 02 (G40)
ROM0_T103	0001 02 (G40)
ROM0_T108	0001 04 (G40)
ROM0_T109	0001 04 (G40)
ROM0_T110	0001 04 (G40)
ROM0_T111	0001 04 (G40)
ROM0_T112	0001 04 (G40)
ROM0_T113	0001 04 (G40)
ROM0_T114	0001 04 (G40)
ROM0_T115	0001 04 (G40)
ROM0_T116	0001 04 (G40)
ROM0_T117	0001 04 (G40)
ROM0_T118	0001 04 (G40)
ROM0_T119	0001 04 (G40)
ROM0_T120	0001 04 (G40)
ROM0_T121	0001 04 (G40)
ROM0_T122	0001 04 (G40)
ROM0_T123	0001 04 (G40)
ROM0_T124	0001 04 (G40)
ROM0_T125	0001 04 (G40)
ROM0_T126	0001 04 (G40)
ROM0_T127	0001 04 (G40)
ROM0_T128	0001 04 (G40)
ROM0_T129	0001 04 (G40)
ROM0_T130	0001 04 (G40)
ROM0_T131	0001 04 (G40)
ROM0_T132	0001 04 (G40)
ROM0_T133	0001 04 (G40)
ROM0_T134	0001 04 (G40)
ROM0_T135	0001 04 (G40)
ROM0_T136	0001 04 (G40)
ROM0_T137	0001 04 (G40)
ROM0_T138	0001 04 (G40)
ROM0_T139	0001 04 (G40)
ROM0_T140	0001 04 (G40)
ROM0_T141	0001 04 (G40)
ROM0_T142	0001 04 (G40)
ROM0_T143	0001 04 (G40)
ROM0_T144	0001 04 (G40)
ROM0_T145	0001 04 (G40)
ROM0_T146	0001 04 (G40)
ROM0_T147	0001 04 (G40)
ROM0_T148	0001 04 (G40)
ROM0_T149	0001 04 (G40)
ROM0_T150	0001 04 (G40)
ROM0_T151	0001 04 (G40)
ROM0_T152	0001 04 (G40)
ROM0_T153	0001 04 (G40)
ROM0_T154	0001 04 (G40)
ROM0_T155	0001 04 (G40)
ROM0_T156	0001 04 (G40)
ROM0_T157	0001 04 (G40)
ROM0_T158	0001 04 (G40)
ROM0_T159	0001 04 (G40)
ROM0_T160	0001 04 (G40)
ROM0_T161	0001 04 (G40)
ROM0_T162	0001 04 (G40)
ROM0_T163	0001 04 (G40)
ROM0_T164	0001 04 (G40)
ROM0_T165	0001 04 (G40)
ROM0_T166	0001 04 (G40)
ROM0_T167	0001 04 (G40)
ROM0_T168	0001 04 (G40)
ROM0_T169	0001 04 (G40)
ROM0_T170	0001 04 (G40)
ROM0_T171	0001 04 (G40)
ROM0_T172	0001 04 (G40)
ROM0_T173	0001 04 (G40)
ROM0_T174	0001 04 (G40)
ROM0_T175	0001 04 (G40)
ROM0_T176	0001 04 (G40)
ROM0_T177	0001 04 (G40)
ROM0_T178	0001 04 (G40)
ROM0_T179	0001 04 (G40)
ROM0_T180	0001 04 (G40)
ROM0_T181	0001 04 (G40)
ROM0_T182	0001 04 (G40)
ROM0_T183	0001 04 (G40)
ROM0_T184	0001 04 (G40)
ROM0_T185	0001 04 (G40)
ROM0_T186	0001 04 (G40)
ROM0_T187	0001 04 (G40)
ROM0_T188	0001 04 (G40)
ROM0_T189	0001 04 (G40)
ROM0_T190	0001 04 (G40)
ROM0_T191	0001 04 (G40)
ROM0_T192	0001 04 (G40)
ROM0_T193	0001 04 (G40)
ROM0_T194	0001 04 (G40)
ROM0_T195	0001 04 (G40)
ROM0_T196	0001 04 (G40)
ROM0_T197	0001 04 (G40)
ROM0_T198	0001 04 (G40)
ROM0_T199	0001 04 (G40)
ROM0_T200	0001 04 (G40)
ROM0_T201	0001 04 (G40)
ROM0_T202	0001 04 (G40)
ROM0_T203	0001 04 (G40)
ROM0_T204	0001 04 (G40)
ROM0_T205	0001 04 (G40)
ROM0_T206	0001 04 (G40)
ROM0_T207	0001 04 (G40)
ROM0_T208	0001 04 (G40)
ROM0_T209	0001 04 (G40)
ROM0_T210	0001 04 (G40)
ROM0_T211	0001 04 (G40)
ROM0_T212	0001 04 (G40)
ROM0_T213	0001 04 (G40)
ROM0_T214	0001 04 (G40)
ROM0_T215	0001 04 (G40)
ROM0_T216	0001 04 (G40)
ROM0_T217	0001 04 (G40)
ROM0_T218	0001 04 (G40)
ROM0_T219	0001 04 (G40)
ROM0_T220	0001 04 (G40)
ROM0_T221	0001 04 (G40)
ROM0_T222	0001 04 (G40)
ROM0_T223	0001 04 (G40)
ROM0_T224	0001 04 (G40)
ROM0_T225	0001 04 (G40)
ROM0_T226	0001 04 (G40)
ROM0_T227	0001 04 (G40)
ROM0_T228	0001 04 (G40)
ROM0_T229	0001 04 (G40)
ROM0_T230	0001 04 (G40)
ROM0_T231	0001 04 (G40)
ROM0_T232	0001 04 (G40)
ROM0_T233	0001 04 (G40)
ROM0_T234	0001 04 (G40)
ROM0_T235	0001 04 (G40)
ROM0_T236	0001 04 (G40)
ROM0_T237	0001 04 (G40)
ROM0_T238	0001 04 (G40)
ROM0_T239	0001 04 (G40)
ROM0_T240	0001 04 (G40)
ROM0_T241	0001 04 (G40)
ROM0_T242	0001 04 (G40)
ROM0_T243	0001 04 (G40)
ROM0_T244	0001 04 (G40)
ROM0_T245	0001 04 (G40)
ROM0_T246	0001 04 (G40)
ROM0_T247	0001 04 (G40)
ROM0_T248	0001 04 (G40)
ROM0_T249	0001 04 (G40)
ROM0_T250	0001 04 (G40)

Messages

Type	Path	Message
Warning	Complete_Qsys_Package.TPHER	Watch dog period can be re-written.
Warning	Complete_Qsys_Package.TPHER	Watch dog counter can be stopped.

0 Errors, 11 Warnings

Generate HDL... Refresh

Qsys - Complete_Qsys_Package.qsys (C:\Project\QCK\FPGA\SCX_V3_010720_completeqsys\qsys\Complete_Qsys_Package.qsys)

File Edit System Generate View Tools Internal Help

Project

- System
- Library
- Base Functions
- BECONOFF
- DSP
- IO
- IP
- Interface Protocols
- Low Power
- Memory Interfaces and Controllers
- Processors and Peripherals
- Qsys Interconnect

System Connections: Complete_Qsys_Package Path: top_0

Name	Description	Export	Clock	Base
external_connection	Conduit			
timer_0	Interval Timer			
timer_1	Interval Timer			
ip2p_interrupt_pio	IP2P (Parallel IO)			
ip2p_interrupt_pio_irq	Interrupt Sender			
ip2p_interrupt_pio_irq	Interrupt Sender			
ip2p_interrupt_pio_irq	Interrupt Sender			
ip2p_interrupt_pio_irq	Interrupt Sender			

Current filter: All Interfaces

Messages:

- 11 Warnings
- Complete_Qsys_Package.TPHER Watch dog period can be rewritten.
- Complete_Qsys_Package.TPHER Watch dog counter can be stopped.

Parameters

System: Complete_Qsys_Package Path: top_0

Arria V/Cyclone V Hard Processor System

alters_tps

External Clock Sources

- EDSIC clock frequency: 25.0 MHz
- EDSIC clock frequency: 25.0 MHz

Enable FPGA-to-HPS SDRAM PLL reference clock

Enable FPGA-to-HPS peripheral PLL reference clock

FPGA-to-HPS SDRAM PLL reference clock frequency: 0.0 MHz

FPGA-to-HPS peripheral PLL reference clock frequency: 0.0 MHz

Peripheral FPGA Clocks

- EMAC0 emac0_clk clock frequency: 100 MHz
- EMAC0 emac0_clk clock frequency: 100 MHz
- EMAC1 emac1_clk clock frequency: 100 MHz
- EMAC1 emac1_clk clock frequency: 100 MHz
- QSPI qspi_clk clock frequency: 100 MHz
- SPI0 spi0_clk clock frequency: 100 MHz
- SPI1 spi1_clk clock frequency: 100 MHz
- IOCO io_c0_clk clock frequency: 100 MHz
- IOCO io_c1_clk clock frequency: 100 MHz
- IOCO io_c2_clk clock frequency: 100 MHz
- IOCO io_c3_clk clock frequency: 100 MHz

Qsys - Complete_Qsys_Package.qsys (C:\Project\QCK\FPGA\SCX_V3_010720_completeqsys\qsys\Complete_Qsys_Package.qsys)

File Edit System Generate View Tools Internal Help

Project

- System
- Library
- Base Functions
- BECONOFF
- DSP
- IO
- IP
- Interface Protocols
- Low Power
- Memory Interfaces and Controllers
- Processors and Peripherals
- Qsys Interconnect

System Connections: Complete_Qsys_Package Path: top_0

Name	Description	Export	Clock	Base
external_connection	Conduit			
timer_0	Interval Timer			
timer_1	Interval Timer			
ip2p_interrupt_pio	IP2P (Parallel IO)			
ip2p_interrupt_pio_irq	Interrupt Sender			
ip2p_interrupt_pio_irq	Interrupt Sender			
ip2p_interrupt_pio_irq	Interrupt Sender			
ip2p_interrupt_pio_irq	Interrupt Sender			

Current filter: All Interfaces

Messages:

- 11 Warnings
- Complete_Qsys_Package.TPHER Watch dog period can be rewritten.
- Complete_Qsys_Package.TPHER Watch dog counter can be stopped.

Parameters

System: Complete_Qsys_Package Path: top_0

Arria V/Cyclone V Hard Processor System

alters_tps

Clock Sources

Peripheral PLL reference clock source: EDSIC clock

SDMHC clock source: Peripheral NAND SDMHC clock

NAND clock source: Peripheral NAND SDMHC clock

QSPI clock source: Main QSPI clock

L4-MP clock source: Peripheral base clock

L4-SP clock source: Peripheral base clock

Main PLL Output Clocks - Desired Frequencies

Default MPU clock frequency: 800.0 MHz

MPU clock frequency: 800.0 MHz

L3-MP clock frequency: 200.0 MHz

L3-SP clock frequency: 100.0 MHz

Debug AT clock frequency: 25.0 MHz

Debug trace clock frequency: 12.5 MHz

L4-MP clock frequency: 100.0 MHz

L4-SP clock frequency: 100.0 MHz

Configuration/HPS-to-FPGA user 0 clock frequency: 100.0 MHz

Peripheral PLL Output Clocks - Desired Frequencies

SDMHC clock frequency: 200.0 MHz

NAND clock frequency: 12.5 MHz

QSPI clock frequency: 400.0 MHz

EMAC0 clock frequency: 250.0 MHz

EMAC1 clock frequency: 250.0 MHz

USB clock frequency: 200.0 MHz

SPI clock frequency: 200.0 MHz

CAN0 clock frequency: 100.0 MHz

CAN1 clock frequency: 100.0 MHz

GPIO absence clock frequency: 32000 Hz

HPS-to-FPGA User Clocks

System Contents

Use	Connections	Name	Description	Export	Clock	Base
		reset	Reset Input	memory	clk	0
		s1	Avalon Memory Mapped Slave	memory	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		Interval_Timer	Interval Timer	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		Interval_Timer	Interval Timer	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		sync_0_interrupt_pio	PID (Parallel I/O)	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		sync_1_interrupt_pio	PID (Parallel I/O)	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		pid_interrupt_pio	PID (Parallel I/O)	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		hps_0	Arria V/Cyclone V Hard Processor System	memory	clk	0
		memory	Conduit	memory	clk	0
		hps_0	Conduit	memory	clk	0
		h2f_reset	Reset Output	memory	clk	0
		h2f_axi_clock	Clock Input	memory	clk	0
		h2f_axi_master	AXI Master	memory	clk	0
		f2h_axi_clock	Clock Input	memory	clk	0
		f2h_axi_slave	AXI Slave	memory	clk	0
		h2f_axi_clock	Clock Input	memory	clk	0
		h2f_axi_master	AXI Master	memory	clk	0

Parameters

Arria V/Cyclone V Hard Processor System

1.3 SP clock frequency: 100.0 MHz

Debug AT clock frequency: 25.0 MHz

Debug clock frequency: 12.5 MHz

Debug trace clock frequency: 25.0 MHz

L4MP clock frequency: 100.0 MHz

L4 SP clock frequency: 100.0 MHz

Configuration-FPGA-to-FPGA user 0 clock frequency: 100.0 MHz

Peripheral PLL Output Clocks - Desired Frequencies

SDMMC clock frequency: 200.0 MHz

NAND clock frequency: 12.5 MHz

QSPI clock frequency: 400.0 MHz

EMAC0 clock frequency: 250.0 MHz

EMAC1 clock frequency: 250.0 MHz

USB clock frequency: 200.0 MHz

SPI clock frequency: 100.0 MHz

CAN0 clock frequency: 100.0 MHz

CAN1 clock frequency: 100.0 MHz

GPIO debounce clock frequency: 32000 Hz

HPS-to-FPGA User Clocks

Enable HPS-to-FPGA user 0 dock:

Enable HPS-to-FPGA user 1 dock:

HPS-to-FPGA user 0 dock frequency: 100.0 MHz

HPS-to-FPGA user 1 dock frequency: 100.0 MHz

Messages

Type	Path	Message
Warning	Complete_Qsys_Package.TPHER	Watch dog period can be re-written.
Warning	Complete_Qsys_Package.TPHER	Watch dog counter can be stopped.

System Contents

Use	Connections	Name	Description	Export	Clock	Base
		reset	Reset Input	memory	clk	0
		s1	Avalon Memory Mapped Slave	memory	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		Interval_Timer	Interval Timer	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		Interval_Timer	Interval Timer	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		sync_0_interrupt_pio	PID (Parallel I/O)	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		sync_1_interrupt_pio	PID (Parallel I/O)	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		pid_interrupt_pio	PID (Parallel I/O)	pio	clk	0
		ck	Clock Input	pio	clk	0
		reset	Reset Input	pio	clk	0
		s1	Avalon Memory Mapped Slave	pio	clk	0
		external_connection	Conduit	pio	clk	0
		irq	Interrupt Sender	pio	clk	0
		hps_0	Arria V/Cyclone V Hard Processor System	memory	clk	0
		memory	Conduit	memory	clk	0
		hps_0	Conduit	memory	clk	0
		h2f_reset	Reset Output	memory	clk	0
		h2f_axi_clock	Clock Input	memory	clk	0
		h2f_axi_master	AXI Master	memory	clk	0
		f2h_axi_clock	Clock Input	memory	clk	0
		f2h_axi_slave	AXI Slave	memory	clk	0
		h2f_axi_clock	Clock Input	memory	clk	0
		h2f_axi_master	AXI Master	memory	clk	0

Parameters

Arria V/Cyclone V Hard Processor System

FPGA Interfaces

SDRAM Protocol: cpld3

PLL Settings

Memory clock frequency: 400.0 MHz

Use specified frequency instead of calculated frequency:

Advanced memory clock frequency: 400.0 MHz

PLL reference clock frequency: 25.0 MHz

Advanced PLL Settings

Supply voltage: 1.8V DDR3

I/O standard: SSTL15

Messages

Type	Path	Message
Warning	Complete_Qsys_Package.TPHER	Watch dog period can be re-written.
Warning	Complete_Qsys_Package.TPHER	Watch dog counter can be stopped.

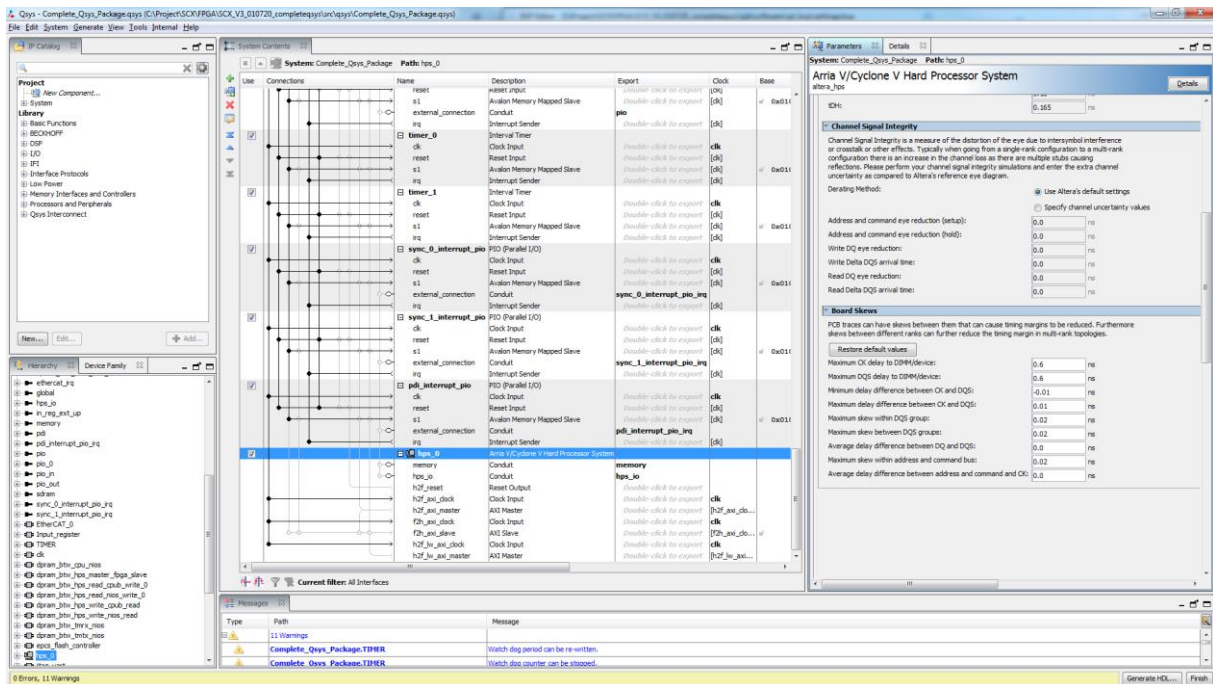
Qsys - Complete_Quys_Package.qsys (C:\Project\Qsys\FPGA\SCX_V3_010720_completeqsys\qsys\Complete_Quys_Package.qsys)
File Edit System Generate View Tools Internal Help

The screenshot displays the Qsys GUI interface. The **System Contents** pane on the left shows a hierarchical tree of components. The **System Contents** table in the center lists components with columns for Name, Description, Export, Clock, and Base. The **Parameters** pane on the right shows configuration options for the **Arria V/Cyclone V Hard Processor System**, including memory format, timing, and initialization options. The **Messages** pane at the bottom shows 11 warnings, two of which are highlighted:

- Complete_Quys_Package.TPHER: Watch dog period can be re-written.
- Complete_Quys_Package.TPHER: Watch dog counter can be stopped.

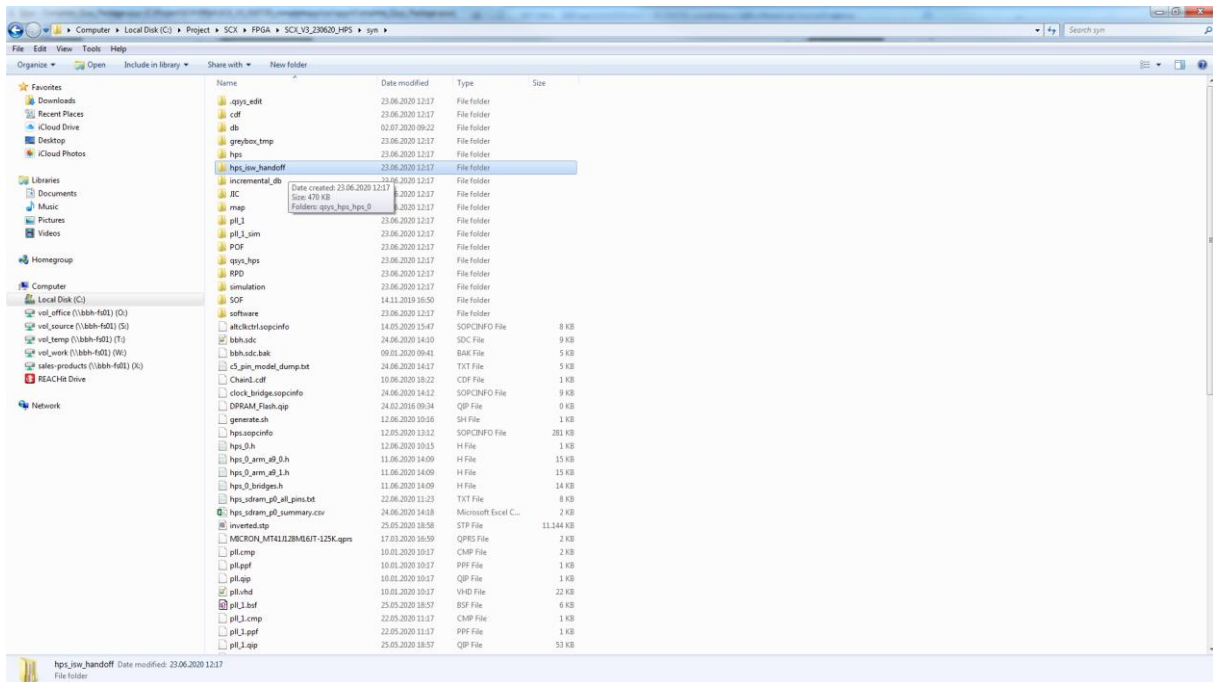
Qsys - Complete_Quys_Package.qsys (C:\Project\Qsys\FPGA\SCX_V3_010720_completeqsys\qsys\Complete_Quys_Package.qsys)
File Edit System Generate View Tools Internal Help

This screenshot is identical to the first one, showing the same Qsys GUI interface with the system configuration and warning messages displayed.

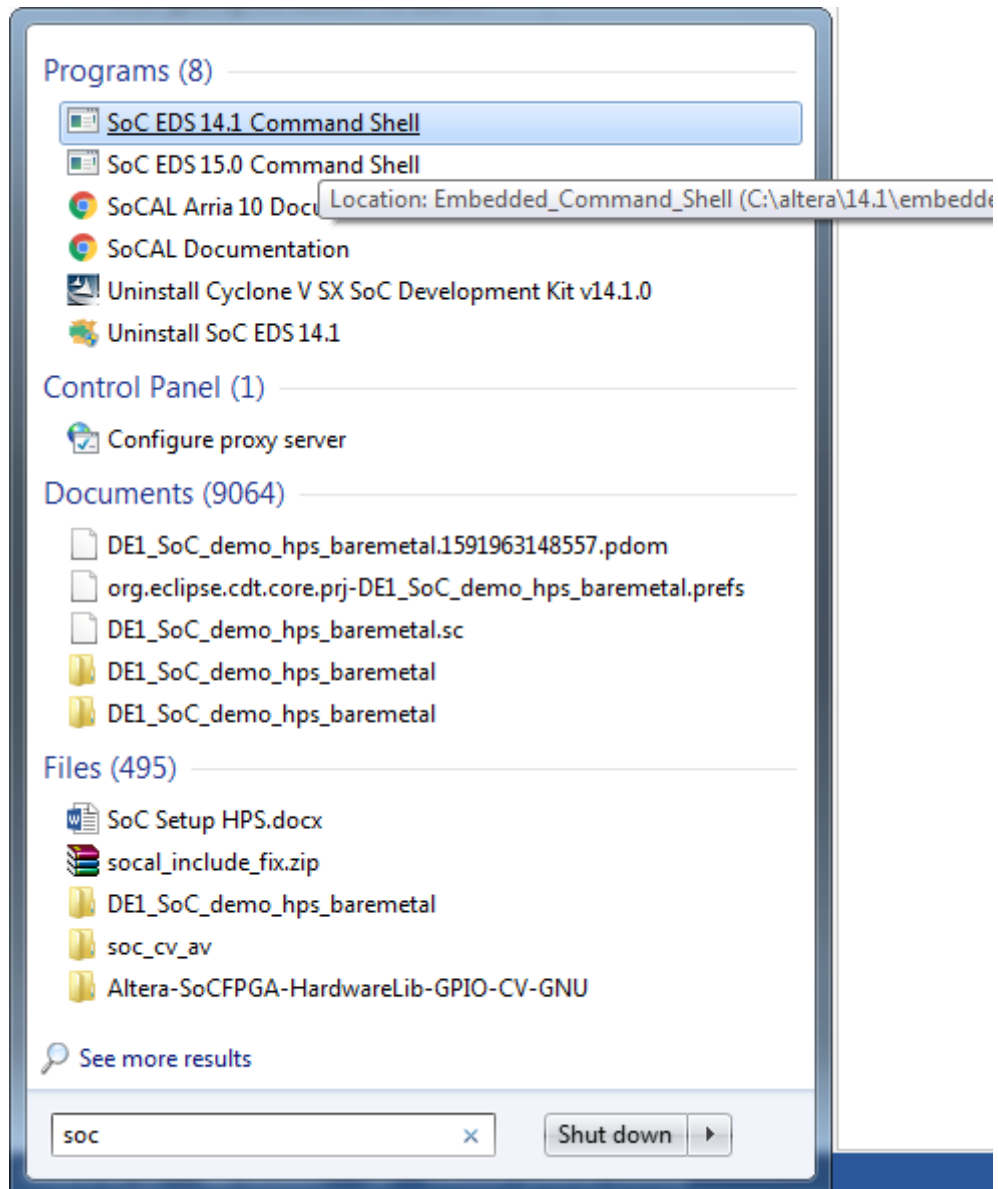


After compiling the FPGA we get the following folder.

Hps_isw_handoff



2. Now open SoC command shell



3. **OPEN** the bsp-editor
By using bsp-editor&

```
image
Created: Thu Jul 02 15:00:41 2020
Image Type: ARM U-Boot Standalone Program (uncompressed)
Data Size: 60984 Bytes = 59.55 kB = 0.06 MB
Load Address: 00100000
Entry Point: 00000000

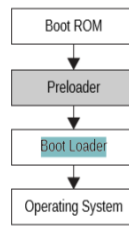
HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp
$ quartus_hps -c 1 -o PU -a 0x60000 outfile_out.img
Info: ****
Info: Running Quartus II 64-Bit Programmer
Info: Version 14.1.0 Build 186 12/03/2014 SJ Full Version
Info: Copyright (C) 1991-2014 Altera Corporation. All rights reserved.
Info: Your use of Altera Corporation's design tools, logic functions
Info: and other software and tools, and its AMPP partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Altera Program License
Info: Subscription Agreement, the Altera Quartus II License Agreement,
Info: the Altera MegaCore Function License Agreement, or other
Info: applicable license agreement, including, without limitation,
Info: that your use is for the sole purpose of programming logic
Info: devices manufactured by Altera and sold by Altera or its
Info: authorized distributors. Please refer to the applicable
Info: agreement for further details.
Info: Processing started: Thu Jul 02 14:07:38 2020
Info: Command: quartus_hps -c 1 -o PU -a 0x60000 outfile_out.img
Current hardware is: USB-Blaster [USB-1]
Found HPS at device 1
HPS Device IDCODE: 0x4BA00477
AHB Port is located at port 0
APB Port is located at port 1
Boot Info: 3.0U QSPI Flash
Clock Select: 0
Double AFI Delay - 128 TCKs
Start HPS Quad SPI flash programming ...
Initialize QSPI peripheral and flash controller ...
Read Silicon ID of Quad SPI flash ...
Quad SPI Flash silicon ID is 0x1020BA20
Flash device matched
Manufacturer: MICRON
Device: QSPI_512
Enable Four Byte Addressing ...
Sector Erase Quad SPI flash ...
Sector Erase Info: Start Addr at 0x00060000 for 1 sector(s)
Sector Erase Quad SPI flash at 0x00060000
Program Quad SPI flash ...
Verify Quad SPI flash ...
Info: Quartus II 64-Bit Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 115 megabytes
Info: Processing ended: Thu Jul 02 14:08:29 2020
Info: Elapsed time: 00:00:51
Info: Total CPU time (on all processors): 00:00:03

HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp
$ hsp-editor&_
```

4. The rules of Preloader

There are four stages of the hard processor system (HPS) booting process; the preloader is the second stage.

Figure 8-1: Typical Boot Flow



The Preloader configures the HPS component based on the information from the handoff folder, initializes the SDRAM and then loads the next stage of the boot process into SDRAM and passes control to it.

The preloader can directly load your final application for Bare Metal applications and simple RTOSes.

Typically, a boot ROM loads the preloader from a flash device into the on-chip RAM and executes the preloader. The preloader can also be executed directly from the FPGA memory.

5. Handoff Files (this files is generated by Qsys)

Hardware Handoff Files

Use the Qsys system integration tool in the Quartus II software to generate a set of handoff files containing the hardware information required by the preloader.

The handoff files from the Qsys compilation are located in the `<quartus project directory>/hps_isw_handoff/<hps entity name>` directory (where **hps entity name** is the HPS component name in Qsys).

Note: You must update the hardware handoff files and regenerate the preloader support package each time a hardware change impacts the HPS, such as after pin multiplexing or pin assignment.

1. The preloader can be generated by using the bsp-editor (please see the next 2 screen shot)

5-4 Getting Started with Preloader

In this example, you will re-create the **Preloader** in the folder `<SoC EDS installation directory>\examples\hardware\cv_soc_devkit_ghrd\software\spl_bsp`.

The screen snapshots presented in this section were created using the Windows version of SoC EDS, but the example can be run in a very similar way on a Linux host PC.

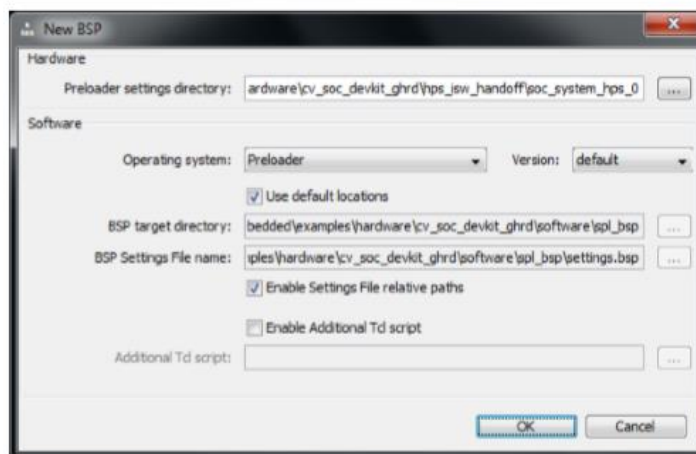
The steps to create the **Preloader** are:

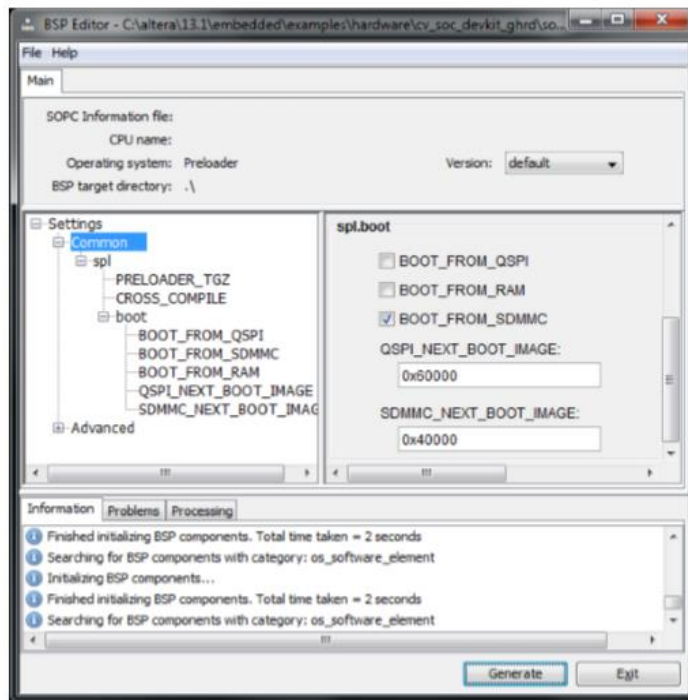
1. Start an Embedded Command Shell by executing `<SoC EDS installation directory>\Embedded_Command_Shell.bat`.
2. Run the command, `bsp-editor`. The **BSP Editor** dialog box appears.

Note: The tool that generates a **preloader** support package is the **BSP Editor**, also used to generate BSPs for other Altera products.

3. Select **File > New BSP**. The **New BSP** dialog opens.
4. Click the "..." button to browse for the **Preloader** settings directory in the **New BSP** dialog box.
5. Browse `<SoCEDS folder>\examples\hardware\cv_soc_devkit_ghrd\hps_isw_handoff\soc_system_hps_0` for the hardware handoff folder. The rest of the **Preloader** settings are populated automatically.

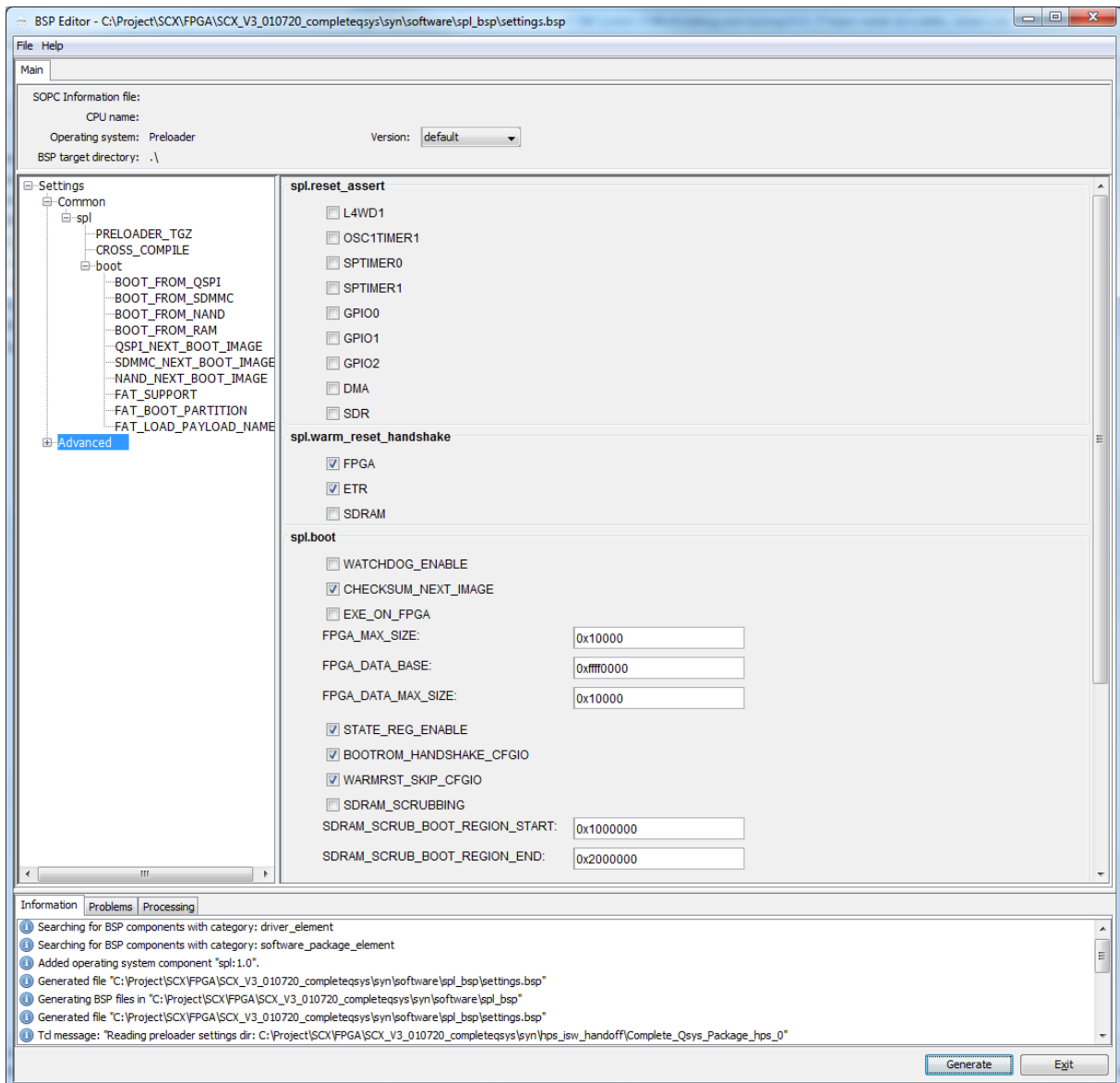
Figure 5-2: Populated Options in the New BSP window

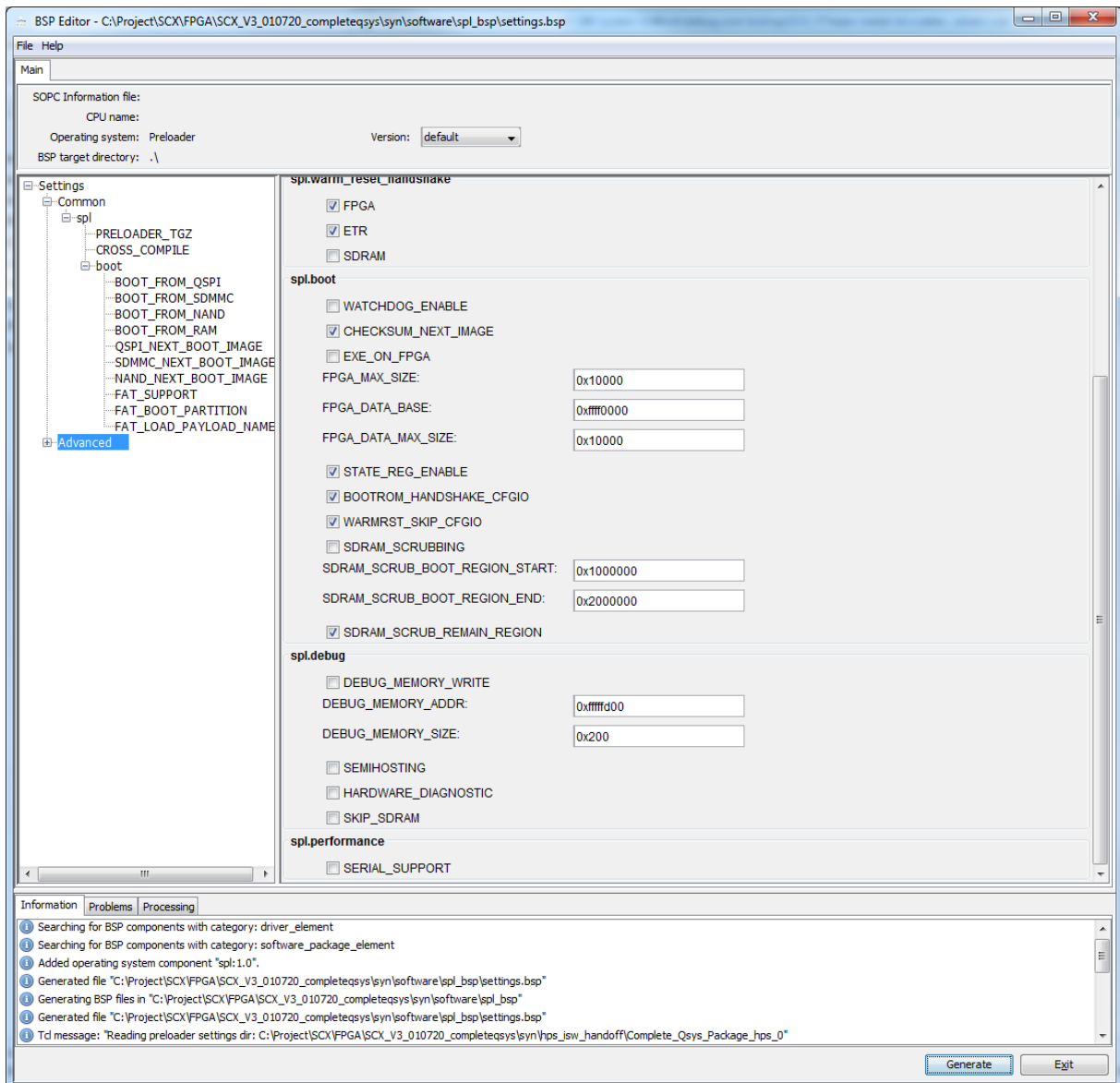




7. Click **Generate** in the **BSP Editor** dialog box to generate the **Preloader** files.
8. Click **Exit** in the **BSP Editor** dialog box to exit the application.
9. In the **Embedded Command Shell**, execute the following commands:
 - `cd <SoC EDS installation directory>\examples\hardware\cv_soc_devkit_ghrd\software\spl_bsp`
 - `make`
10. The **Preloader** is ready to be used in the above folder. Some of the more relevant files that are created:
 - **preloader-mkpimage.bin** – Preloader with the proper header to be loaded by BootROM
 - **uboot-socfpga \spl \u-boot- spl** – Preloader ELF file, to be used for debugging purposes
 - **uboot-socfpga \tools\mkimage.exe** – Utility to add the header needed by the **Preloader** to recognize the next boot stage

2. see the following boot loader settings for booting from qspi





3. For the debugging, the preloader ELF file (u-boot-spl) should be imported to the DS-5 debugger

after generate the preloader, use the embedded shall to generate the preloader ELF file.

First, specify the path of preloader (cd:) that it is already generated, then write “make clean” or “make clean-all”, then “make uboot”.

```

/cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp
GA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/board/alter
a/socfpga/sdram/libsocfpga-sdram.o /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_co
mpleteqsys/syn/software/spl_bsp/uboot-socfpga/spl/common/libcommon.o /cygdrive/c
/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga
/spl/common/spl/libspl.o /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys
/syn/software/spl_bsp/uboot-socfpga/spl/drivers/dma/libdma.o /cygdrive/c/Project
/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/drive
rs/mtd/spi/libspi_flash.o /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsy
s/syn/software/spl_bsp/uboot-socfpga/spl/drivers/spi/libspi.o /cygdrive/c/Projec
t/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/lib
/libgeneric.o | sed -n -e '/.*\.u_boot_list\|! <d;n>' -e 's/.*\(\.u_boot_l
ist\|^ \|+\).*$\^1/' -e 's/.*\(\. \|+\)$/' -e 's/.*\^+$/ { p;s/(\.*)\.[^\.]*$\^1
/b;s }' | sed -n -e 'h;s/$\^a/p;g;s/$\^@/p;g;s/$\^~/p;' | LC_COLLATE=C sort -u |
sed -n -e '\^a$/ { s/./g;s/\^a$/_start = .;p; }' -e '/\^$/ { s/./g;s/\^$/
end = .;p; }' -e '/@$/ { s/(\.*)@$/*(SORT(\1.*));p }' > /cygdrive/c/Project/
SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/u-boo
t.lst
arm-altera-eabi-gcc -E -g -Os -fno-common -ffixed-r8 -msoft-float -I/cygdriv
e/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpg
a/board/altera/socfpga -I/cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsy
s/syn/software/spl_bsp/uboot-socfpga/board/altera/socfpga/sdram -D_KERNEL -ff
unction-sections -fdata-sections -DCONFIG_SYS_TEXT_BASE=0x01000040 -DCONFIG_SPL
TEXT_BASE=0xFFFF0000 -DCONFIG_SPL_BUILD -I/cygdrive/c/Project/SCX/FPGA/SCX_U3_01
0720_completeqsys/syn/software/spl_bsp/uboot-socfpga/include -fno-builtin -ffree
standing -nostdinc -isystem c:/altera/14.1/embedded/host_tools/mentor/gnu/arm/ba
remetal/bin/./lib/gcc/arm-altera-eabi/4.9.1/include -pipe -DCONFIG_ARM -D_ARM
__ -mthumb -mthumb-interwork -mabi=aapcs-linux -march=armv7-a -include /cygdrive
/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpg
a/include/u-boot/u-boot.lds.h -include /cygdrive/c/Project/SCX/FPGA/SCX_U3_01072
0_completeqsys/syn/software/spl_bsp/uboot-socfpga/include/config.h -DCPUIDR=arch
/arm/cpu/armv7 -I/cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/so
ftware/spl_bsp/uboot-socfpga/spl/. -ansi -D_ASSEMBLY__ -P -< /cygdrive/c/Proje
ct/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/arch/a
rm/cpu/armv7/socfpga/u-boot-spl.lds > /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720
_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/u-boot-spl.lds
cd /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp
/uboot-socfpga/spl/ && arm-altera-eabi-ld -I /cygdrive/c/Project/SCX/FPGA/SCX_U3
_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/u-boot-spl.lds -gc
-sections -Bstatic -Ttext 0xFFFF0000 arch/arm/cpu/armv7/start.o --start-group arc
h/arm/cpu/armv7/libarmv7.o arch/arm/cpu/armv7/socfpga/libsocfpga.o arch/arm/lib/
libarm.o board/altera/socfpga/libsocfpga.o board/altera/socfpga/sdram/libsocfpga
-sdram.o common/libcommon.o common/spl/libspl.o drivers/dma/libdma.o drivers/mtd
/spi/libspi_flash.o drivers/spi/libspi.o lib/libgeneric.o --end-group /cygdrive/
c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga
/spl/arch/arm/lib/eabi_compat.o -L c:/altera/14.1/embedded/host_tools/mentor/gnu
/arm/baremetal/bin/./lib/gcc/arm-altera-eabi/4.9.1 -lgcc -Map u-boot-spl.map -o
u-boot-spl
arm-altera-eabi-objcopy --gap-fill=0xff -O binary /cygdrive/c/Project/SCX/FPGA/S
CX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-socfpga/spl/u-boot-spl /cyg
drive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/software/spl_bsp/uboot-s
ocfpga/spl/u-boot-spl.bin
make[2]: Leaving directory '/cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_complet
eqsys/syn/software/spl_bsp/uboot-socfpga/spl'
make[1]: Leaving directory '/cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_complet
eqsys/syn/software/spl_bsp/uboot-socfpga'
mkpimage --header-version 0 -o preloader-mkpimage.bin uboot-socfpga/spl/u-boot-s
pl.bin uboot-socfpga/spl/u-boot-spl.bin uboot-socfpga/spl/u-boot-spl.bin uboot-s
ocfpga/spl/u-boot-spl.bin
HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_U3_010720_completeqsys/syn/soft
ware/spl_bsp

```

- Flash this generated preloader-mkpimage.bin to QSPI flash using the following command

```

/cygdrive/c/Project/SCX/FPGA/SCX_V3_010720_completeqsys/syn/software/spl_bsp
make[1]: Leaving directory '/cygdrive/c/Project/SCX/FPGA/SCX_V3_010720_completeq
sys/syn/software/spl_bsp/u-boot-socfpga'
mkpimage --header-version 0 -o preloader-mkpimage.bin uboot-socfpga/spl/u-boot-s
pl.bin uboot-socfpga/spl/u-boot-spl.bin uboot-socfpga/spl/u-boot-spl.bin uboot-s
ocfpga/spl/u-boot-spl.bin

HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_V3_010720_completeqsys/syn/soft
ware/spl_bsp
$ quartus_hps -c 1 -o PU preloader-mkpimage.bin
Info: *****
Info: Running Quartus II 64-Bit Programmer
Info: Version 14.1.0 Build 186 12/03/2014 SJ Full Version
Info: Copyright (C) 1991-2014 Altera Corporation. All rights reserved.
Info: Your use of Altera Corporation's design tools, logic functions
Info: and other software and tools, and its AMPP partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Altera Program License
Info: Subscription Agreement, the Altera Quartus II License Agreement,
Info: the Altera MegaCore Function License Agreement, or other
Info: applicable license agreement, including, without limitation,
Info: that your use is for the sole purpose of programming logic
Info: devices manufactured by Altera and sold by Altera or its
Info: authorized distributors. Please refer to the applicable
Info: agreement for further details.
Info: Processing started: Thu Jul 02 13:34:18 2020
Info: Command: quartus_hps -c 1 -o PU preloader-mkpimage.bin
Current hardware is: USB-Blaster IUSB-11
Found HPS at device 1
HPS Device IDCODE: 0x4BA00477
AHB Port is located at port 0
APB Port is located at port 1
Boot Info: 3.00 QSPI Flash
Clock Select: 0
Double AFI Delay - 128 TCKs
Start HPS Quad SPI flash programming ...
Initialize QSPI peripheral and flash controller ...
Read Silicon ID of Quad SPI flash ...
Quad SPI Flash silicon ID is 0x1020BA20
Flash device matched
Manufacturer: MICRON
Device: QSPI_512
Enable Four Byte Addressing ...
Sector Erase Quad SPI flash ...
Sector Erase Info: Start Addr at 0x00000000 for 4 sector(s)
Sector Erase Quad SPI flash at 0x00000000
Sector Erase Quad SPI flash at 0x00010000
Sector Erase Quad SPI flash at 0x00020000
Sector Erase Quad SPI flash at 0x00030000
Program Quad SPI flash ...
Verify Quad SPI flash ...
Info: Quartus II 64-Bit Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 112 megabytes
Info: Processing ended: Thu Jul 02 13:37:42 2020
Info: Elapsed time: 00:03:24
Info: Total CPU time (on all processors): 00:00:10

HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_V3_010720_completeqsys/syn/soft
ware/spl_bsp
$

```

5. Add the scatter file to your DS-5 project. The scatter file which we are using will support the interrupts too. The interrupt is also called from the DDR3 memory. It makes no difference in the time If we use the onchip scatter file for interrupt or the DDR3 scatter file for the interrupt. The problem to use onchip scatter with DDR3 scatter makes a very big out.bin file.

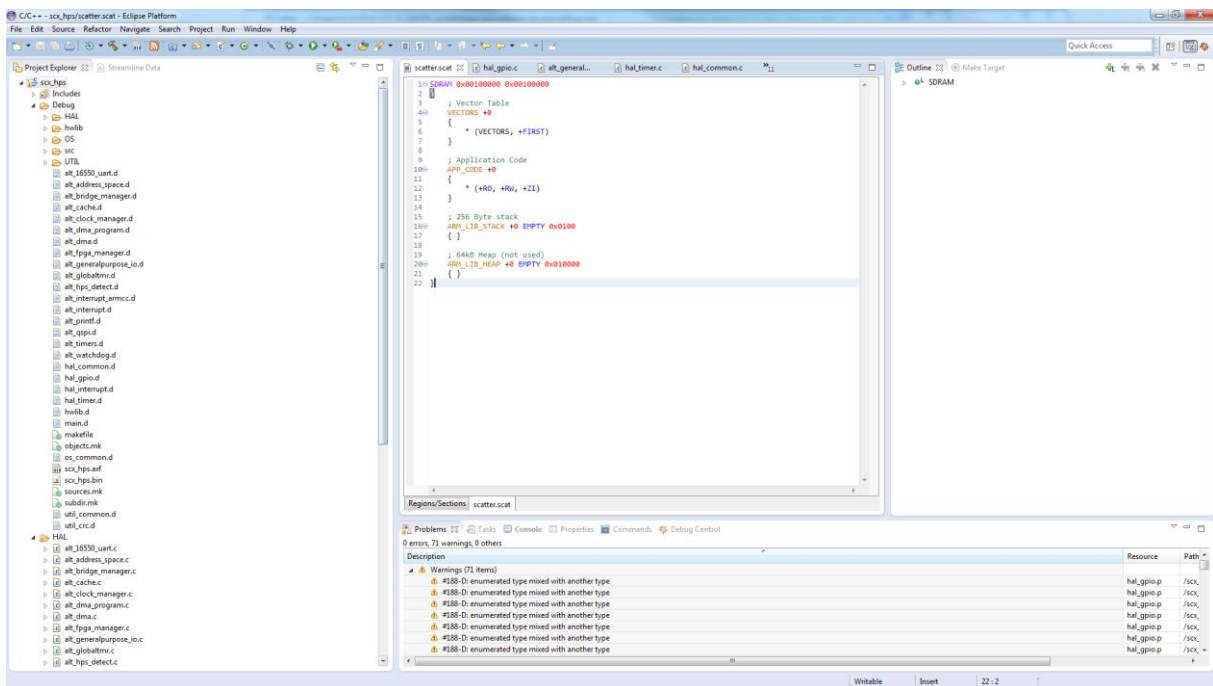
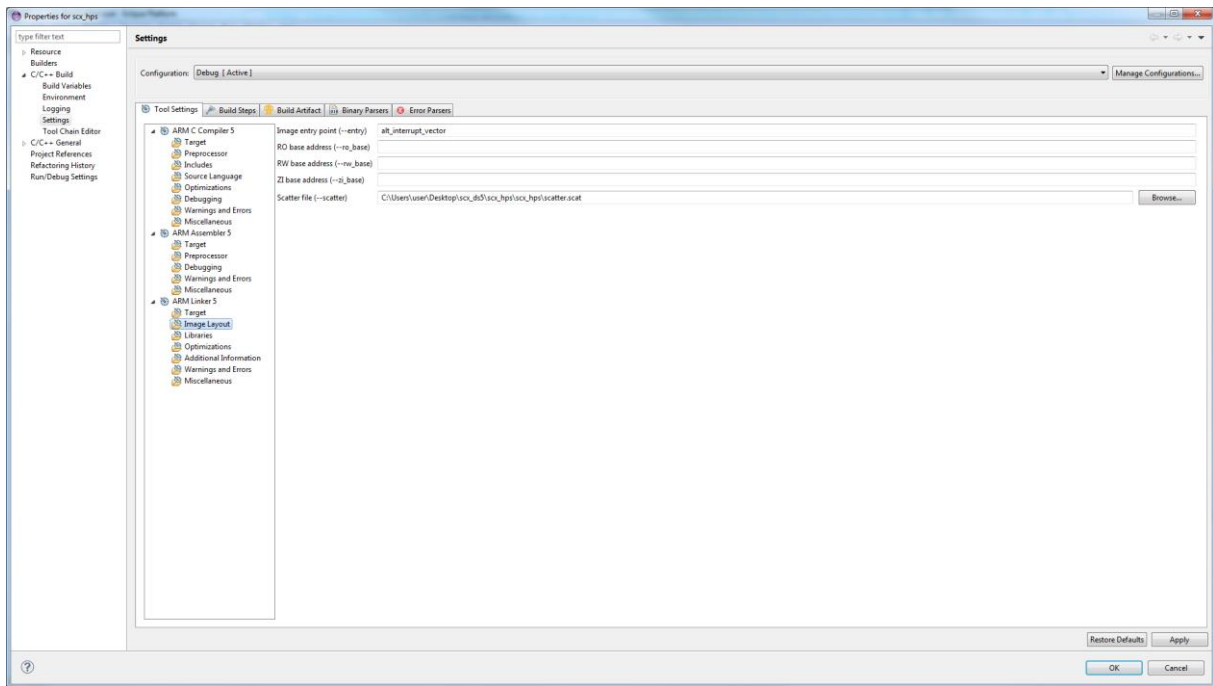


Abbildung 1: DDR3 interrupt

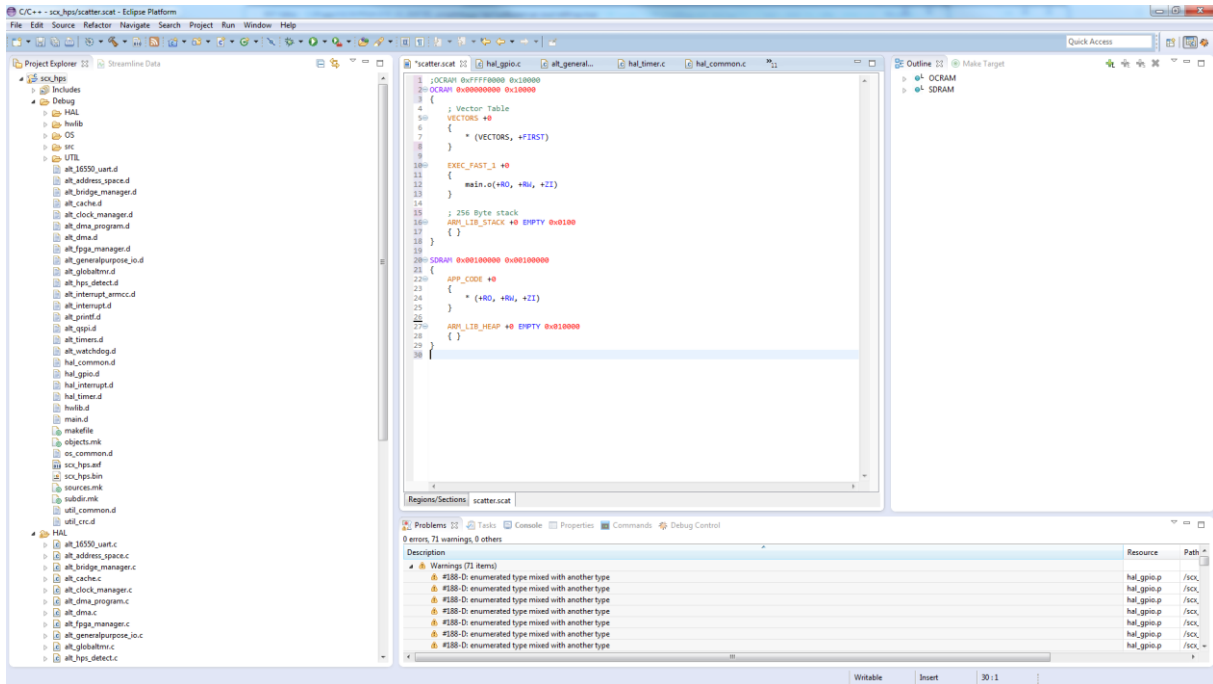
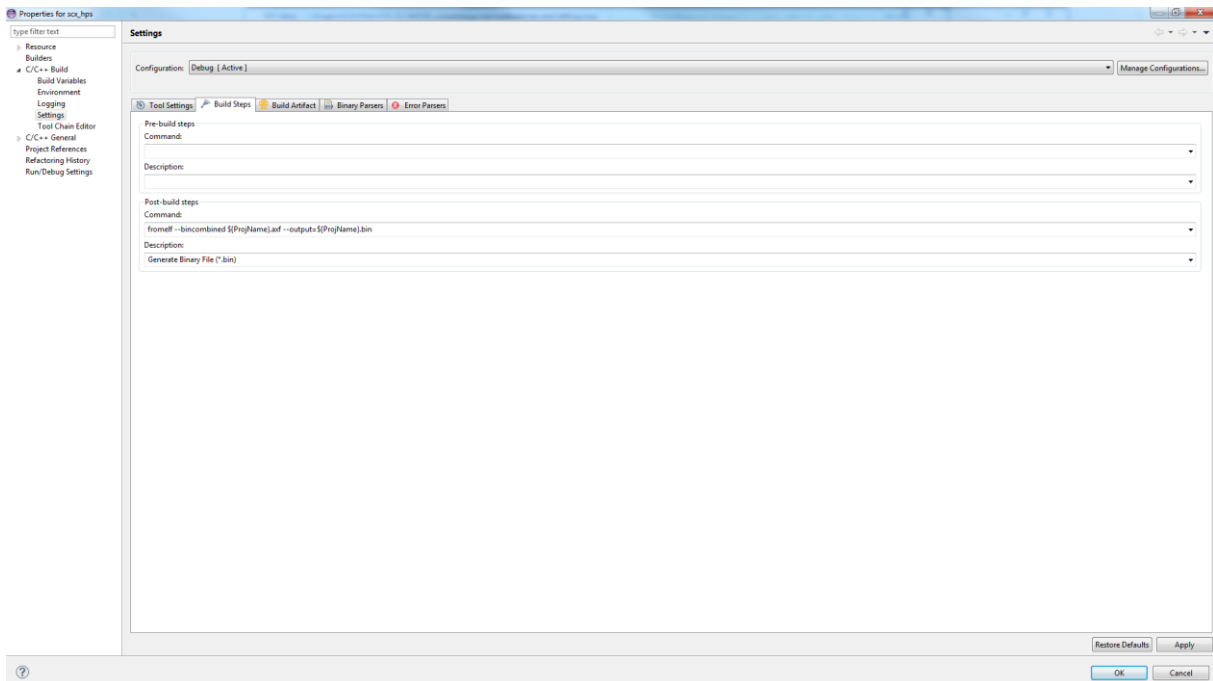


Abbildung 2: onchip for interrupt and the remaining program from DDR3

6. In the DS-5 the project settings use the fromelf as shown below this will generate the binary file after you compile the baremetal code.



7. After getting the out.bin file add the boot header using the following command

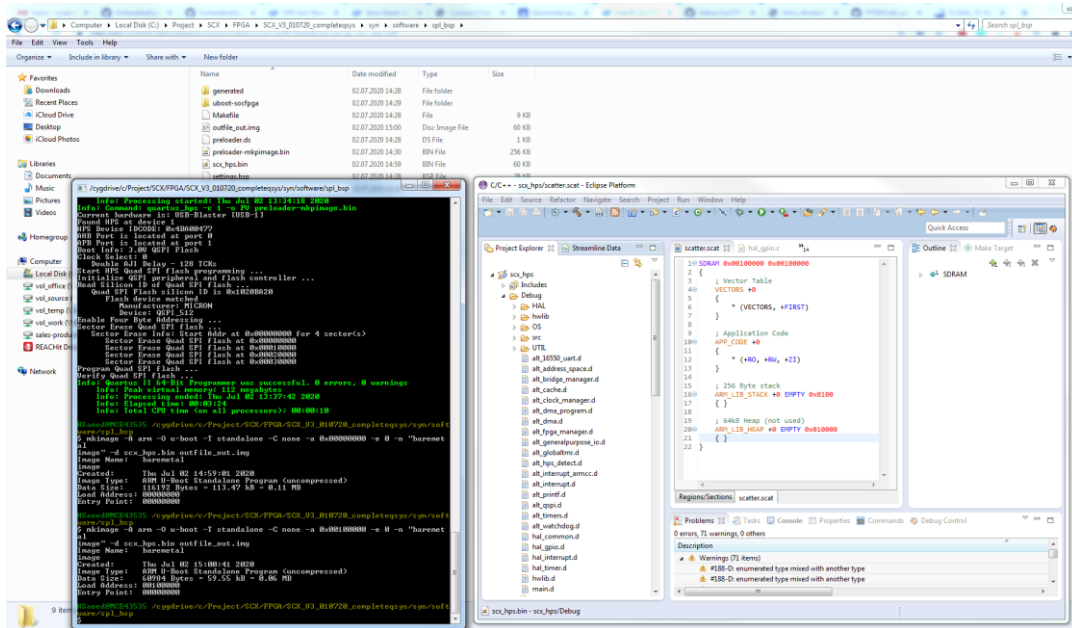
```
mkimage -A arm -O u-boot -T standalone -C none -a 0x02100000 -e 0 -n "baremetal image" -d hello_world.bin hello_world.img
```

here "0x02100000" depends on the scatter file used in the project

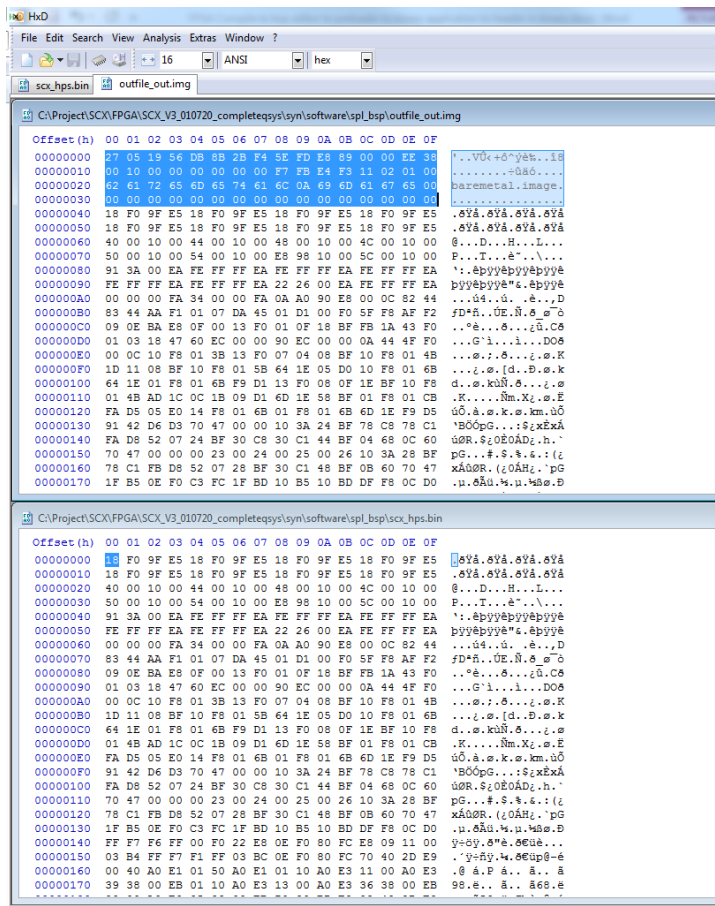
I used the following command for the scatter file shown in Abbildung 2

```
mkpimage --header-version 0 -o preloader-mkpimage.bin uboot-socfpga/spl/u-boot-spl.bin uboot-socfpga/spl/u-boot-spl.bin uboot-socfpga/spl/u-boot-spl.bin
HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_V3_010720_completeqsys/syn/software/spl_bsp
$ quartus_hps -c 1 -o PU preloader-mkpimage.bin
Info: ****
Info: Running Quartus II 64-Bit Programmer
Info: Version 14.1.0 Build 186 12/03/2014 SJ Full Version
Info: Copyright (C) 1991-2014 Altera Corporation. All rights reserved.
Info: Your use of Altera Corporation's design tools, logic functions
Info: and other software and tools, and its AMPP partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Altera Program License
Info: Subscription Agreement, the Altera Quartus II License Agreement,
Info: the Altera MegaCore Function License Agreement, or other
Info: applicable license agreement, including, without limitation,
Info: that your use is for the sole purpose of programming logic
Info: devices manufactured by Altera and sold by Altera or its
Info: authorized distributors. Please refer to the applicable
Info: agreement for further details.
Info: Processing started: Thu Jul 02 13:34:18 2020
Info: Command: quartus_hps -c 1 -o PU preloader-mkpimage.bin
Current hardware is: USB-Blaster IUSB-11
Found HPS at device 1
HPS Device IDCODE: 0x4BA00477
AHB Port is located at port 0
APB Port is located at port 1
Boot Info: 3.00 QSPI Flash
Clock Select: 0
Double AJI Delay - 128 TCKs
Start HPS Quad SPI flash programming ...
Initialize QSPI peripheral and flash controller ...
Read Silicon ID of Quad SPI flash ...
Quad SPI Flash silicon ID is 0x1020BA20
Flash device matched
Manufacturer: MICRON
Device: QSPI_512
Enable Four Byte Addressing ...
Sector Erase Quad SPI flash ...
Sector Erase Info: Start Addr at 0x00000000 for 4 sector(s)
Sector Erase Quad SPI flash at 0x00000000
Sector Erase Quad SPI flash at 0x00010000
Sector Erase Quad SPI flash at 0x00020000
Sector Erase Quad SPI flash at 0x00030000
Program Quad SPI flash ...
Verify Quad SPI flash ...
Info: Quartus II 64-Bit Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 112 megabytes
Info: Processing ended: Thu Jul 02 13:37:42 2020
Info: Elapsed time: 00:03:24
Info: Total CPU time (on all processors): 00:00:10
HSaeed@MCE43535 /cygdrive/c/Project/SCX/FPGA/SCX_V3_010720_completeqsys/syn/software/spl_bsp
$ mkimage -A arm -O u-boot -T standalone -C none -a 0x00000000 -e 0 -n "baremetal
image" -d scx_hps.bin outfile_out.img_
```

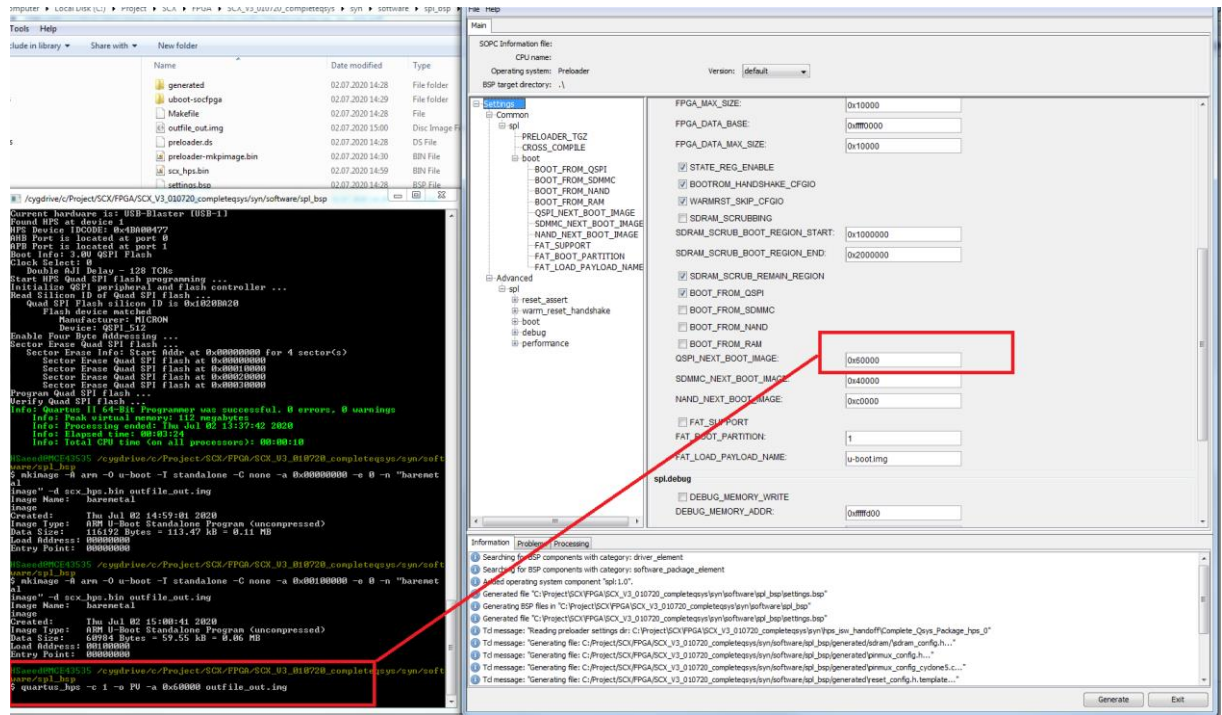
8. After executing command for the shown scatter file will add the header information and generate outfile_out.img



The following header is added in the binary file



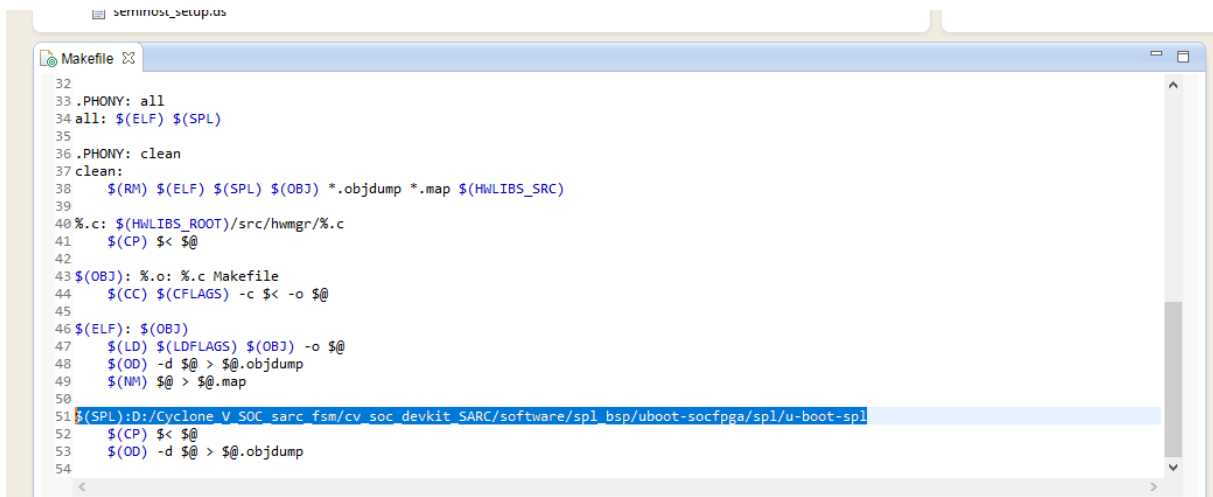
9. Flash this image which we just created on the QSPI using the following command.



Power on the device and it should start up with your application program.

Extra information if needed.

The preloader ELF file is now generated and can be imported to the DS-5 debugger through a makefile (available in my DS-5 project).



You need then to load the (.svd) file to have the features of accessing to soft IP register.

This file is also generated after the Qsys is compiled. To load this file (**.svd**) to DS-debugger, open (**Debugger configuration --> files**), and load the (**.svd file**) which located in **synthesis folder** (please see the next screen shot).

The following handoff files are created when the hardware project is compiled:

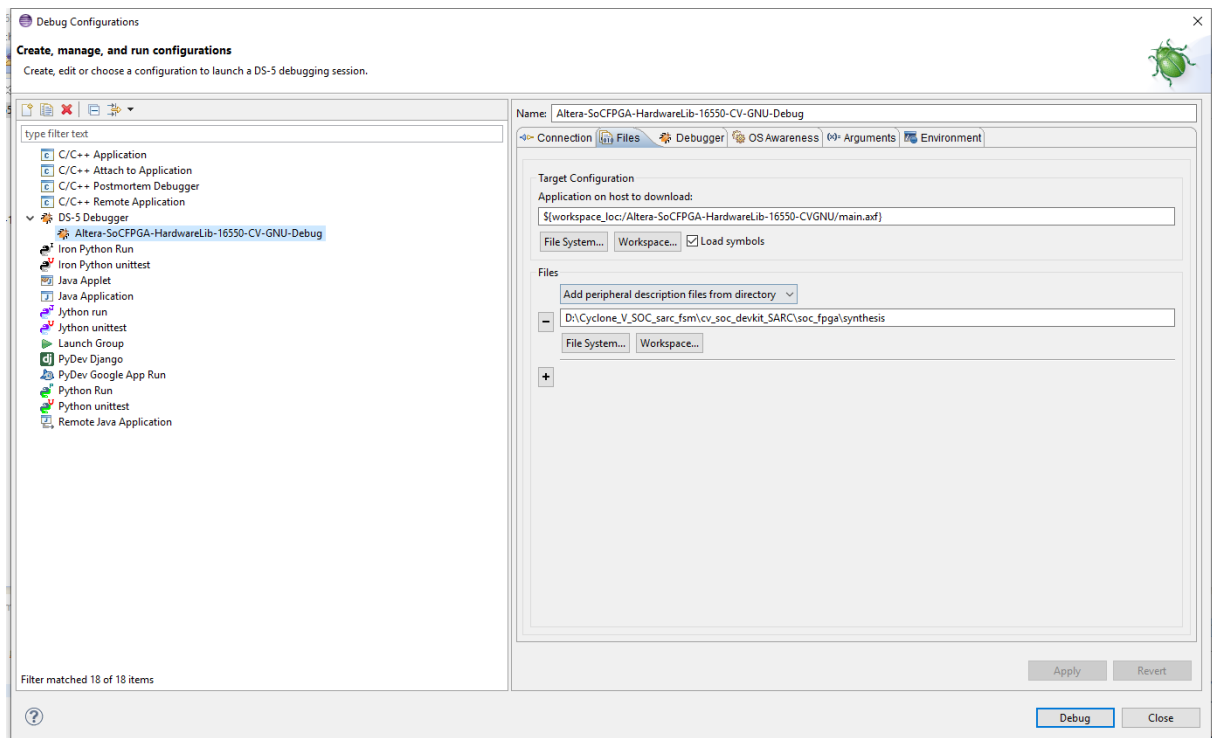
- **Handoff** folder – contains information about how the HPS component is configured, including things like which peripherals are enabled, the pin muxing and IOCSR settings, memory parameters, etc
- **.svd** file – contains descriptions of the HPS registers and of the soft IP registers on FPGA side
- **.sopcinfo** file – contains a description of the whole system

The handoff folder is used by the preloader generator to create the Preloader.

The **.svd** file contains the description of the registers of the HPS peripheral registers and registers for soft IP components in the FPGA portion of the SoC. This file is used by the ARM DS-5 Debugger to allow these registers to be inspected and modified by the user.

SOPC Information (**.sopcinfo**) file, containing a description of the entire system, is used by the Device Tree Generator to create the Device Tree used by the Linux kernel.

Note: The soft IP register descriptions are not generated for all soft IP cores.

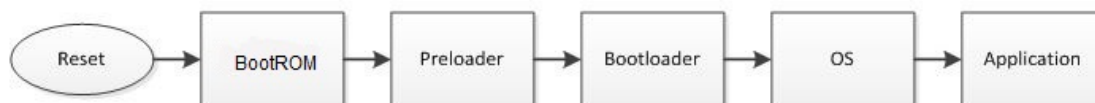


Loading the . SVD file

Additional information about Boot ROM, Preloader, and BootLoader

The following figure depicts the typical boot flow:

Figure 1. Typical Boot Flow



Boot ROM

The HPS boot process starts when the processor is released from reset, and jumps to the reset vector address, located in the Boot ROM address space.

Typically, the main responsibilities of the Boot ROM are:

- Detect the selected boot source
- Perform minimal HPS initialization
- Load the next boot stage (typically the Preloader) from Flash to OCRAM and jump to it

The behavior of the Boot ROM is influenced by the BSEL and CSEL options, and also by the registers in System Manager (for RAM boot) as shown later in the document.

For the scenarios where the next boot stage is located in Flash, the Boot ROM can use up to four different images:

Preloader

Typically, the main responsibilities of the Preloader are:

- Perform additional HPS initialization
- Bring up SDRAM
- Load the next boot stage from Flash to SDRAM and jump to it

Currently, two different Preloader options are available:

- SPL – part of U-Boot. Provided with SoC EDS under GPL (Open Source) License
- MPL – provided with SoC EDS as an example using the HWLibs (Altera bare-metal libraries). Uses BSD license.

Note: The Preloader requires a special header to be placed at the beginning of the next stage boot image. Also, the header contains a CRC value used to validate the image. The header can be attached to an image by using the `mkimage` utility that is included with the SoC EDS.

Bootloader

The Bootloader has typical responsibilities that are similar with the Preloader, except it does not need to bring up SDRAM.

Because the Bootloader is already residing in SDRAM, it is not limited by the size of the OCRAM. Therefore, it can provide a lot of features, such as network stack support.