Using Cylcone V HMCPHY DQ pins as high frequency inputs

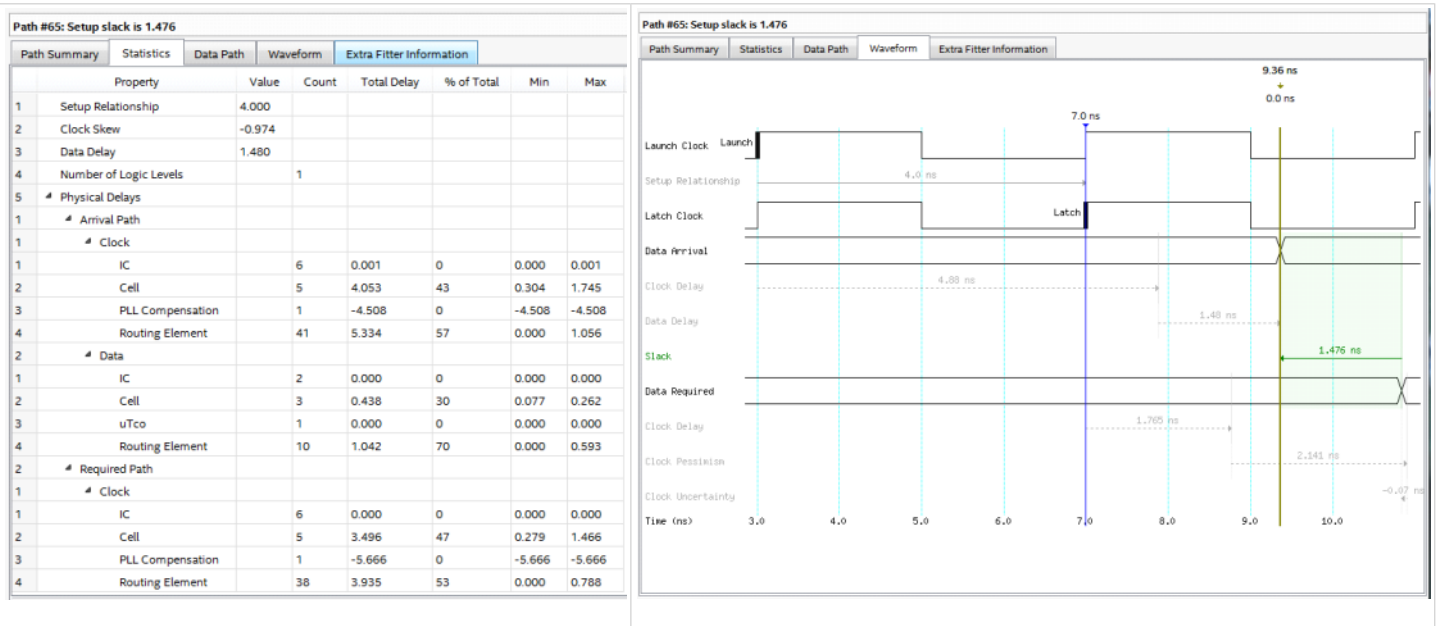
dinsdag 30 mei 2017 9:33

I am working on a design that uses two 500MSps ADCs with a DDR interface clocked at 250MHz. The ADC supplies the 250MHz clock to clock the signals into the FPGA. I am using the ADLTDDIO_IN IP block to clock the DDR signal into the FPGA. This results in a DATA_l and a DATA_h signal which is processed in two parallel paths. This is working without timing problems for one of the ADCs.

The problem is that some of the data lines of the second ADC are connected to multi-function pins that can also be used in combination with the Hard Memory Controller (HMCPHY). The Cyclone V Device Handbook states that one should avoid using these pins (HMC DQ pins) as input pins for signals faster than 200MHz. The problem is that all hardware (boards) are finished and I have to solve this problem in the FPGA.

When building the project I get timing issues on the multi-function pins. When checking the timing in detail I discovered that the timing problems are caused by the fact that these signals are routed through the HMC causing an extra routing delay of about 3.0 to 3.5 ns. This results in the following waveforms:

ADC_DI_DDR_data_h[3] (not a HMC pin) to VectorRegister[3]:

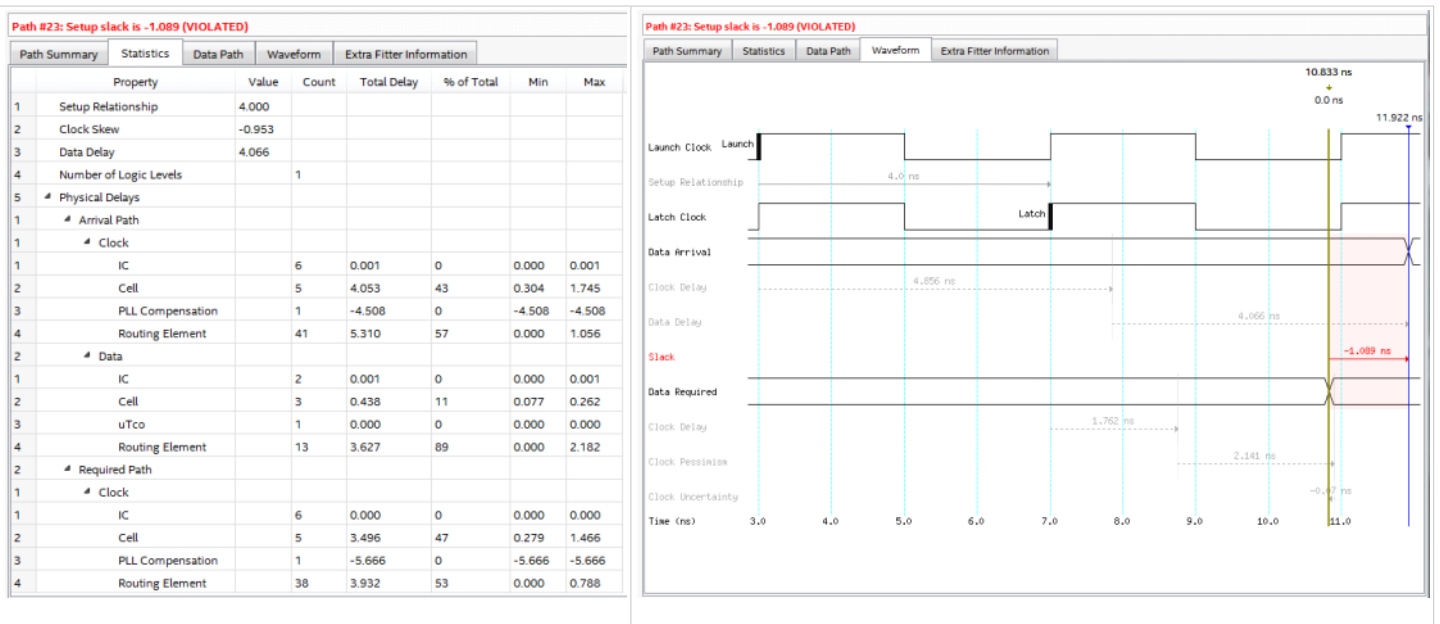


Path #65: Setup slack is 1.476

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	4.000					
2	Clock Skew	-0.974					
3	Data Delay	1.480					
4	Number of Logic Levels		1				
5	◢ Physical Delays						
1	◢ Arrival Path						
1	◢ Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.334	57	0.000	1.056
2	◢ Data						
1	IC		2	0.000	0	0.000	0.000
2	Cell		3	0.438	30	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		10	1.042	70	0.000	0.593
2	◢ Required Path						
1	◢ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.935	53	0.000	0.788

ADC_DI_DDR_data_h[4] (HMC pin) to VectorRegister[4]:



Path #23: Setup slack is -1.089 (VIOLATED)

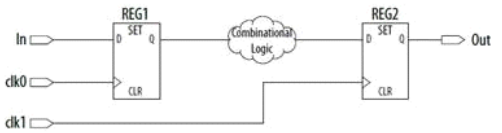
Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	4.000					
2	Clock Skew	-0.953					
3	Data Delay	4.066					
4	Number of Logic Levels		1				
5	◢ Physical Delays						
1	◢ Arrival Path						
1	◢ Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.310	57	0.000	1.056
2	◢ Data						
1	IC		2	0.001	0	0.000	0.001
2	Cell		3	0.438	11	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		13	3.627	89	0.000	2.182
2	◢ Required Path						
1	◢ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.932	53	0.000	0.788

Because the highest worst-case slack for these signals is -1.315 ns, I tried to use a second clock to clock the first register (VectorRegister) in the FPGA fabric (first register after the ALTDDIO_IN). This second clock is the 4ns clock used for the ALTDDIO_IN shifted with 90 degrees. The idea is to have 1 ns extra setup time. Of course the next data will be clocked into the ALTDDIO_IN when the output of the previous bit isn't clocked into the VectorRegister, but I assume that due to the propagation delay the right data will be clocked into this register. I am even considering adding `a set_min_delay` on the signal.

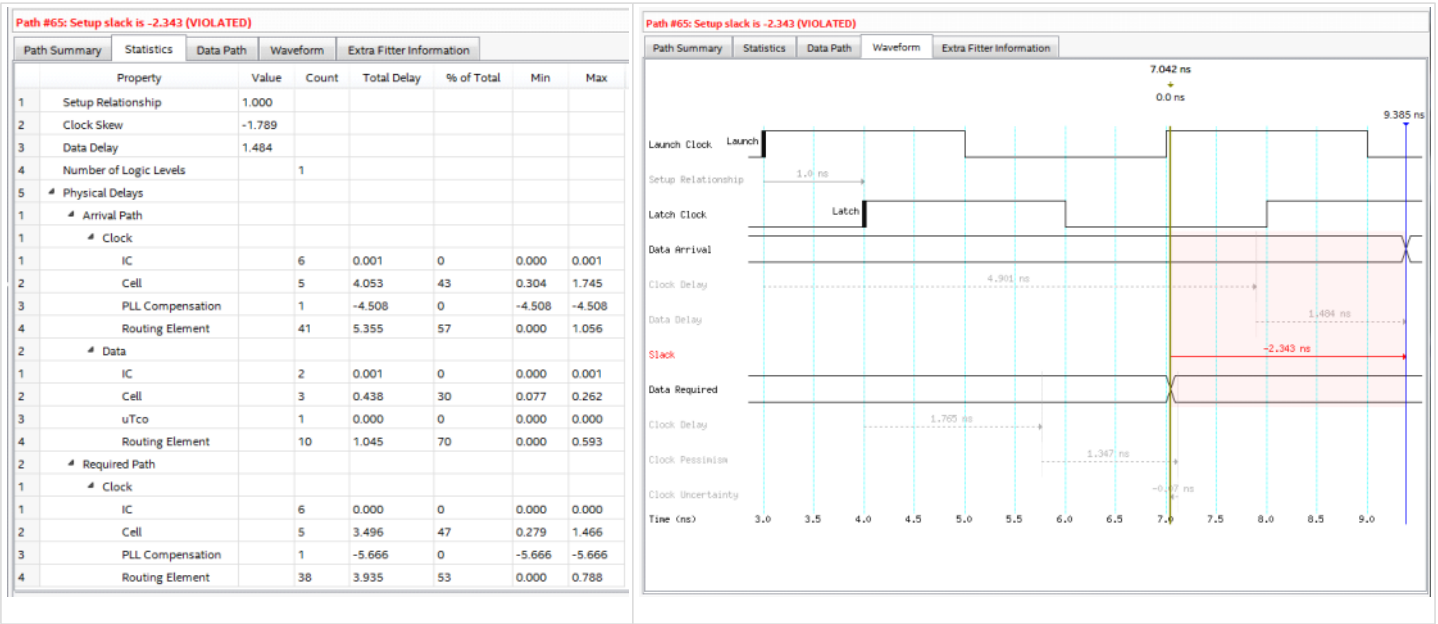
This idea is based on "Same frequency clocks with destimation clock offset" application example described in the Quartus Prime handbook - Volume 3 (QPS5V3 page 7-42) see figure below:

Figure 7-35: Same Frequency Clocks with Destination Clock Offset



Without setting any additional constraints there are a lot of timing issues due to the fact that Quartus tries to accommodate for a latch edge that is 1ns after the launch edge. The waveforms for the signals shown above are now:

ADC_DI_DDR_data_h[3] (not a HMC pin) to VectorRegister[3]:

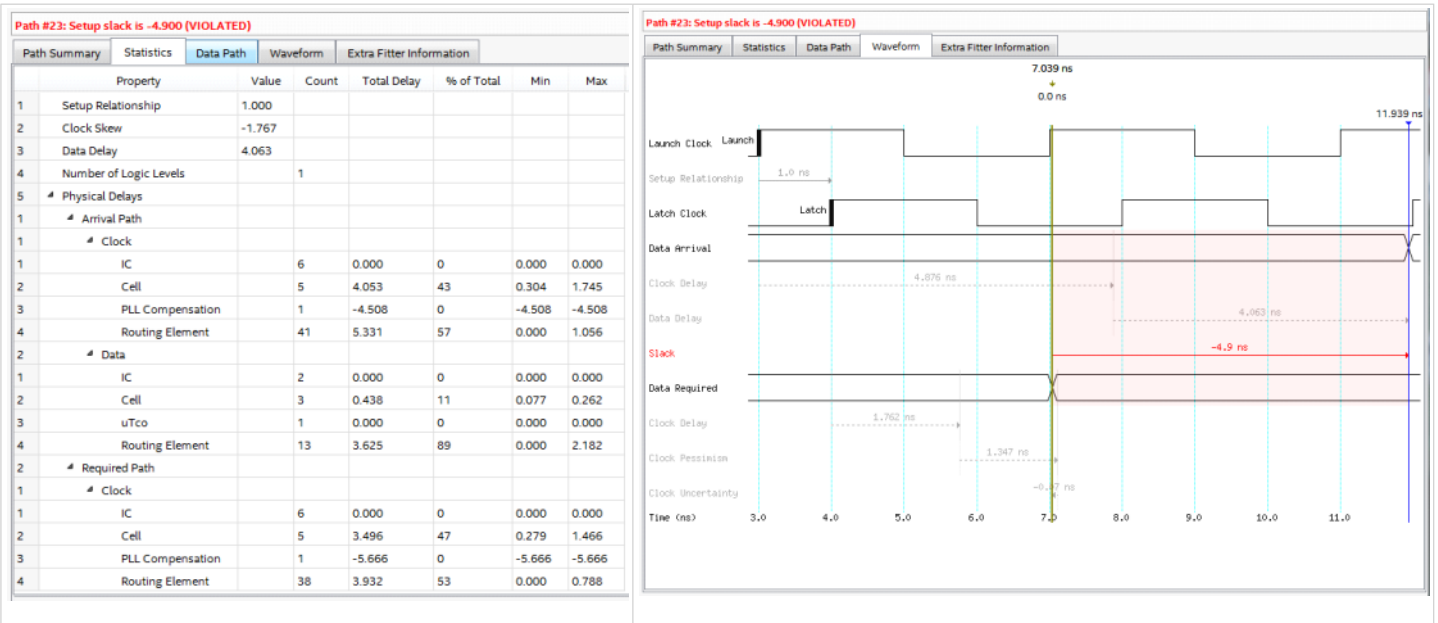


Path #65: Setup slack is -2.343 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	1.000					
2	Clock Skew	-1.789					
3	Data Delay	1.484					
4	Number of Logic Levels		1				
5	◢ Physical Delays						
1	◢ Arrival Path						
1	◢ Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.355	57	0.000	1.056
2	◢ Data						
1	IC		2	0.001	0	0.000	0.001
2	Cell		3	0.438	30	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		10	1.045	70	0.000	0.593
2	◢ Required Path						
1	◢ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.935	53	0.000	0.788

ADC_DI_DDR_data_h[4] (HMC pin) to VectorRegister[4]:



Path #23: Setup slack is -4.900 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	1.000					
2	Clock Skew	-1.767					
3	Data Delay	4.063					
4	Number of Logic Levels		1				
5	◢ Physical Delays						
1	◢ Arrival Path						
1	◢ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.331	57	0.000	1.056
2	◢ Data						
1	IC		2	0.000	0	0.000	0.000
2	Cell		3	0.438	11	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		13	3.625	89	0.000	2.182
2	◢ Required Path						
1	◢ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.932	53	0.000	0.788

Based on the negative slack of -4.9 ns one could argue that moving the Latch edge by 4.0 ns will not solve the problem for the signal using the HMC pin. It would be sufficient for the ADC_DI_DDR_data_h[3] signal which has a negative slack of -2.343 ns.

To use the second rising edge of the second clock (with a phase shift of 90 degrees) I added a `set_multicycle_path -from [...] -to [...] -setup -end 2` constraint. In my opinion this should use the second rising edge of the Latch clock which should cause the timing of the ADC_DI_DDR_data_h[3] on the non HMC pin to be within timing limits again.

Entering the set_multicycle_path constraint in TimeQuest and report timing again (without rebuilding the design) results in the following:

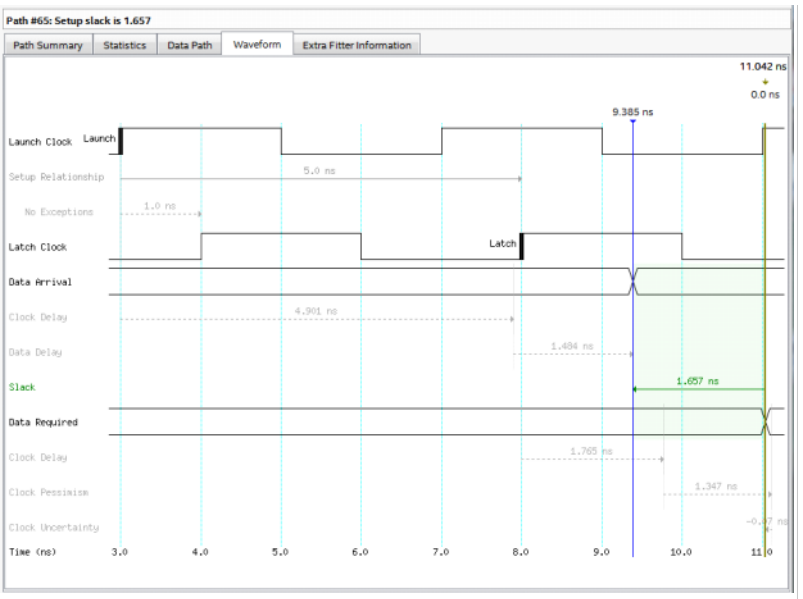
```
set_multicycle_path -from [get_clocks *pll_1*general\[0\].gpll~PLL_OUTPUT_COUNTER\|divclk] -to   [get_clocks *pll_1*general\[1\].gpll~PLL_OUTPUT_COUNTER\|divclk] -setup -end 2
```

ADC_DI_DDR_data_h[3] (not a HMC pin) to VectorRegister[3]:

Path #65: Setup slack is 1.657

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.789					
3	Data Delay	1.484					
4	Number of Logic Levels		1				
5	▲ Physical Delays						
1	▲ Arrival Path						
1	▲ Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.355	57	0.000	1.056
2	▲ Data						
1	IC		2	0.001	0	0.000	0.001
2	Cell		3	0.438	30	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		10	1.045	70	0.000	0.593
2	▲ Required Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.935	53	0.000	0.788

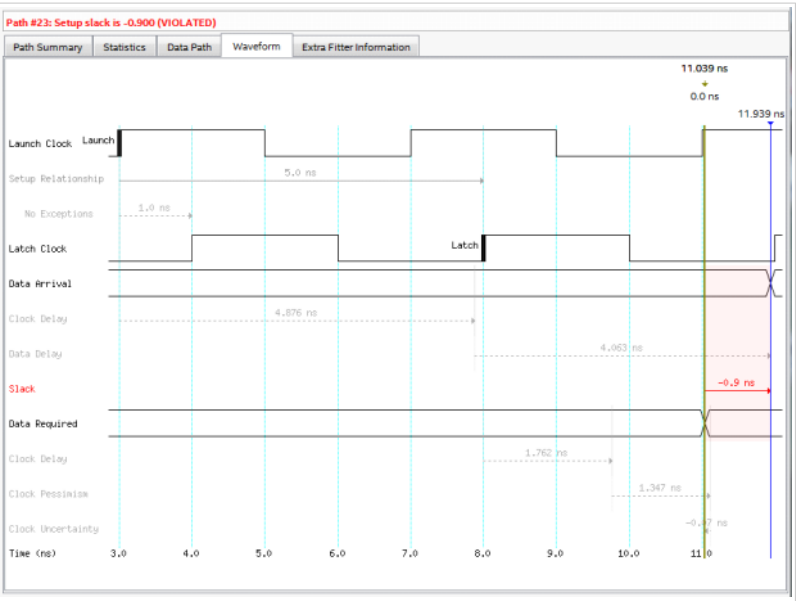


ADC_DI_DDR_data_h[4] (HMC pin) to VectorRegister[4]:

Path #23: Setup slack is -0.900 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.767					
3	Data Delay	4.063					
4	Number of Logic Levels		1				
5	▲ Physical Delays						
1	▲ Arrival Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.331	57	0.000	1.056
2	▲ Data						
1	IC		2	0.000	0	0.000	0.000
2	Cell		3	0.438	11	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		13	3.625	89	0.000	2.182
2	▲ Required Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.932	53	0.000	0.788



This indicates that the timing for the HMC pin might not be met. It might be necessary to shift the Latch clock with 180 Degrees instead of 90 Degrees to solve the remaining negative slack of -0.9 ns.

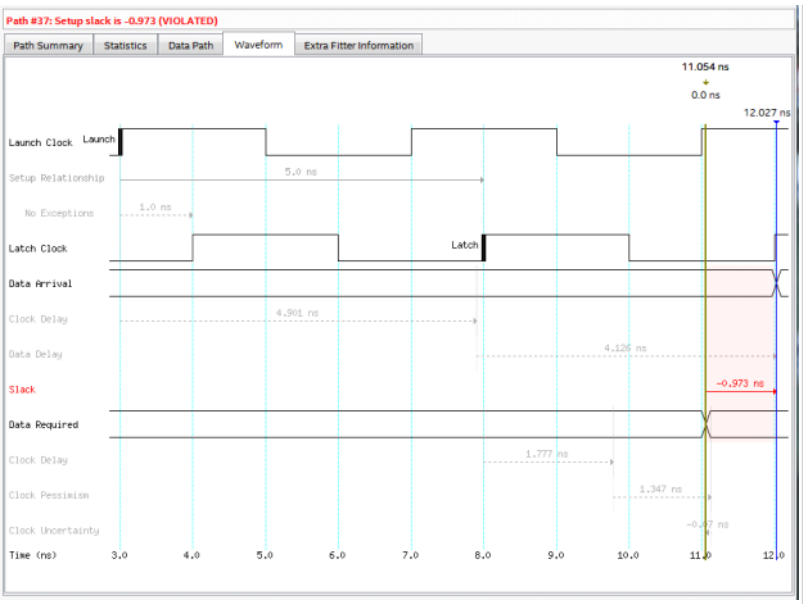
To see how the timing is after a rebuild, I built the design again (after project cleanup to clean previous results). Surprisingly I get quite different results now:

ADC_DI_DDR_data_h[3] (not a HMC pin) to VectorRegister[3]:

Path #37: Setup slack is -0.973 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.777					
3	Data Delay	4.126					
4	Number of Logic Levels		0				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.355	57	0.000	1.056
2	Data						
1	IC		1	0.002	0	0.002	0.002
2	Cell		2	0.711	17	0.099	0.612
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		19	3.413	83	0.000	0.593
2	Required Path						
1	Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.508	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.935	53	0.000	0.788



Somehow the Data Delay increased from 1.484 ns to 4.126 ns. The mean increase is in the Routing elements

Results based on recalculation with TimeQuest prior to rebuild:

Path #65: Setup slack is 1.657

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.789					
3	Data Delay	1.484					
4	Number of Logic Levels		1				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.355	57	0.000	1.056
2	Data						
1	IC		2	0.001	0	0.000	0.001
2	Cell		3	0.438	30	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		10	1.045	70	0.000	0.593
2	Required Path						
1	Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.935	53	0.000	0.788

Results after rebuild with multicycle path constraint

Path #37: Setup slack is -0.973 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

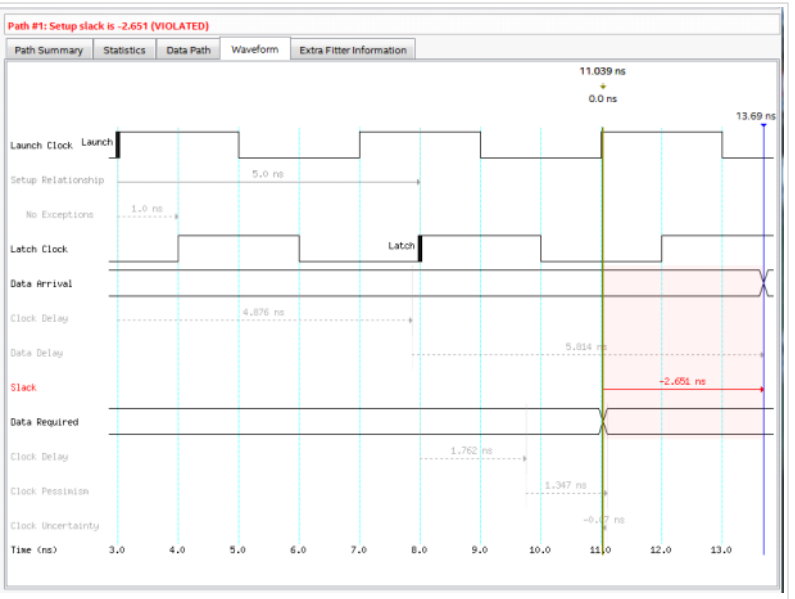
	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.777					
3	Data Delay	4.126					
4	Number of Logic Levels		0				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		6	0.001	0	0.000	0.001
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.355	57	0.000	1.056
2	Data						
1	IC		1	0.002	0	0.002	0.002
2	Cell		2	0.711	17	0.099	0.612
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		19	3.413	83	0.000	0.593
2	Required Path						
1	Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.508	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.935	53	0.000	0.788

ADC_DI_DDR_data_h[4] (HMC pin) to VectorRegister[4]:

Path #1: Setup slack is -2.651 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.767					
3	Data Delay	5.814					
4	Number of Logic Levels		0				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.331	57	0.000	1.056
2	Data						
1	IC		1	0.000	0	0.000	0.000
2	Cell		2	0.658	11	0.099	0.559
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		17	5.156	89	0.000	2.182
2	Required Path						
1	Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.932	53	0.000	0.788



For this signal the Data Delay also increased. The calculation in TimeQuest before rebuild showed a negative slack of -0.9 ns. With the build this increased to -2.651 ns.

Path #23: Setup slack is -0.900 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.767					
3	Data Delay	4.063					
4	Number of Logic Levels		1				
5	▲ Physical Delays						
1	▲ Arrival Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.331	57	0.000	1.056
2	▲ Data						
1	IC		2	0.000	0	0.000	0.000
2	Cell		3	0.438	11	0.077	0.262
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		13	3.625	89	0.000	2.182
2	▲ Required Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.932	53	0.000	0.788

Path #1: Setup slack is -2.651 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	5.000					
2	Clock Skew	-1.767					
3	Data Delay	5.814					
4	Number of Logic Levels		0				
5	▲ Physical Delays						
1	▲ Arrival Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	4.053	43	0.304	1.745
3	PLL Compensation		1	-4.508	0	-4.508	-4.508
4	Routing Element		41	5.331	57	0.000	1.056
2	▲ Data						
1	IC		1	0.000	0	0.000	0.000
2	Cell		2	0.658	11	0.099	0.559
3	uTco		1	0.000	0	0.000	0.000
4	Routing Element		17	5.156	89	0.000	2.182
2	▲ Required Path						
1	▲ Clock						
1	IC		6	0.000	0	0.000	0.000
2	Cell		5	3.496	47	0.279	1.466
3	PLL Compensation		1	-5.666	0	-5.666	-5.666
4	Routing Element		38	3.932	53	0.000	0.788

My questions are:

1. Why does adding the multicycle path constraint result in extra delay being added to the data path?
   This is not only the case with the HMC pin signals but also with 'normal' signals. With the HMC pin signals one could argue that the fitter has no knowledge of the extra delay caused by the HMC, but for non HMC pin signals this shouldn't be the case.

2. Am I doing something wrong? Am I using the wrong multicycle path constraint?