1.1 FT245 Synchronous FIFO Interface Mode Description

When channel A is configured in an FT245 Synchronous FIFO interface mode the IO timing of the signals used are shown in Figure Error**! No text of specified style in document.**.1, which shows details for read and write accesses. The timings are shown in

Name	Minimum	Typical	Maximum	Units	Description
t1		16.67	16.67	ns	CLKOUT period
t2	7.5	8.33	9.17	ns	CLKOUT high period
t3	7.5	8.33	9.17	ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to RXF#
t5	1		7.15	ns	CLKOUT to read DATA valid
t6	1		7.15	ns	OE# to read DATA valid
t7	8			ns	OE# Setup time
t8	0			ns	OE# Hold time
t9	8			ns	RD# Setup time
t10	0			ns	RD# Hold time
t11	1		7.15	ns	CLKOUT to TXE#
t12	8			ns	Write DATA Setup time
t13	0			ns	Write DATA Hold time
t14	8			ns	WR# Setup time
t15	0			ns	WR# Hold time

Table **Error! No text of specified style in document.**.1. Note that only a read or a write cycle can be performed at any one time. Data is read or written on the rising edge of the CLKOUT clock.

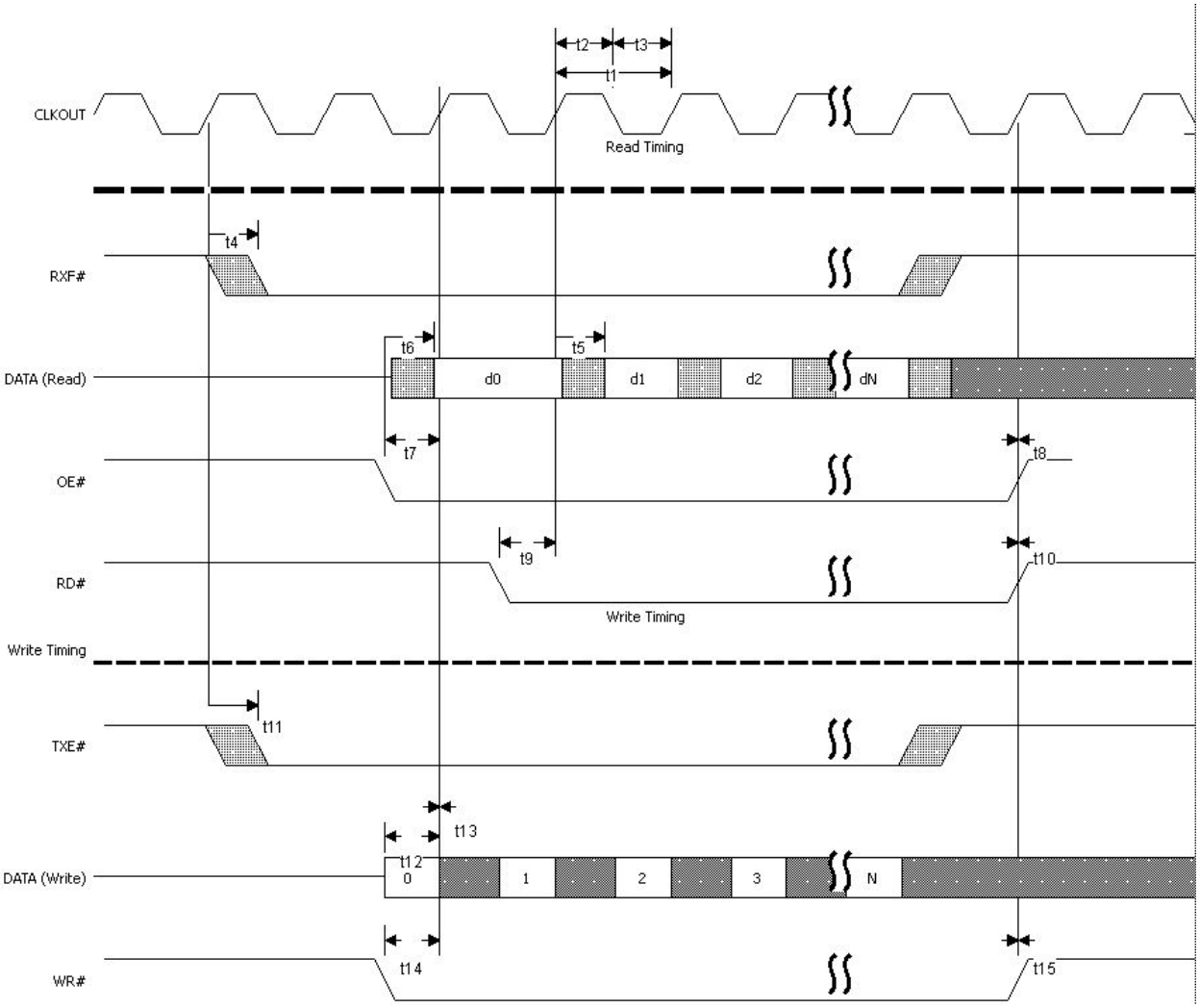

Figure Error! No text of specified style in document.**.1 FT245 Synchronous FIFO Interface Signal Waveforms**

Name	Minimum	Typical	Maximum	Units	Description
t1		16.67	16.67	ns	CLKOUT period
t2	7.5	8.33	9.17	ns	CLKOUT high period
t3	7.5	8.33	9.17	ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to RXF#
t5	1		7.15	ns	CLKOUT to read DATA valid
t6	1		7.15	ns	OE# to read DATA valid
t7	8			ns	OE# Setup time
t8	0			ns	OE# Hold time
t9	8			ns	RD# Setup time
t10	0			ns	RD# Hold time
t11	1		7.15	ns	CLKOUT to TXE#
t12	8			ns	Write DATA Setup time
t13	0			ns	Write DATA Hold time
t14	8			ns	WR# Setup time
t15	0			ns	WR# Hold time

Table Error! No text of specified style in document.**.1 FT245 Synchronous FIFO Interface Signal Timings**

This single channel mode uses a synchronous interface to get high data transfer speeds. The chip drives a 60 MHz CLKOUT clock for the external system to use.

Note that Asynchronous FIFO mode must be selected on both channels before selecting the Synchronous FIFO mode in software.

1.1.1 FT245 Synchronous FIFO Read Operation

A read operation is started when the chip drives RXF# low. The external system can then drive OE# low to turn around the data bus drivers before acknowledging the data with the RD# signal going low. The first data byte is on the bus after OE# is low. The external system can burst the data out of the chip by keeping RD# low or it can insert wait states in the RD# signal. If there is more data to be read it will change on the clock following RD# sampled low. Once all the data has been consumed, the chip will drive RXF# high. Any data that appears on the data bus, after RXF# is high, is invalid and should be ignored.

1.1.2 FT245 Synchronous FIFO Write Operation

A write operation can be started when TXE# is low. WR# is brought low when the data is valid. A burst operation can be done on every clock providing TXE# is still low. The external system must monitor TXE# and its own WR# to check that data has been accepted. Both TXE# and WR# must be low for data to be accepted.