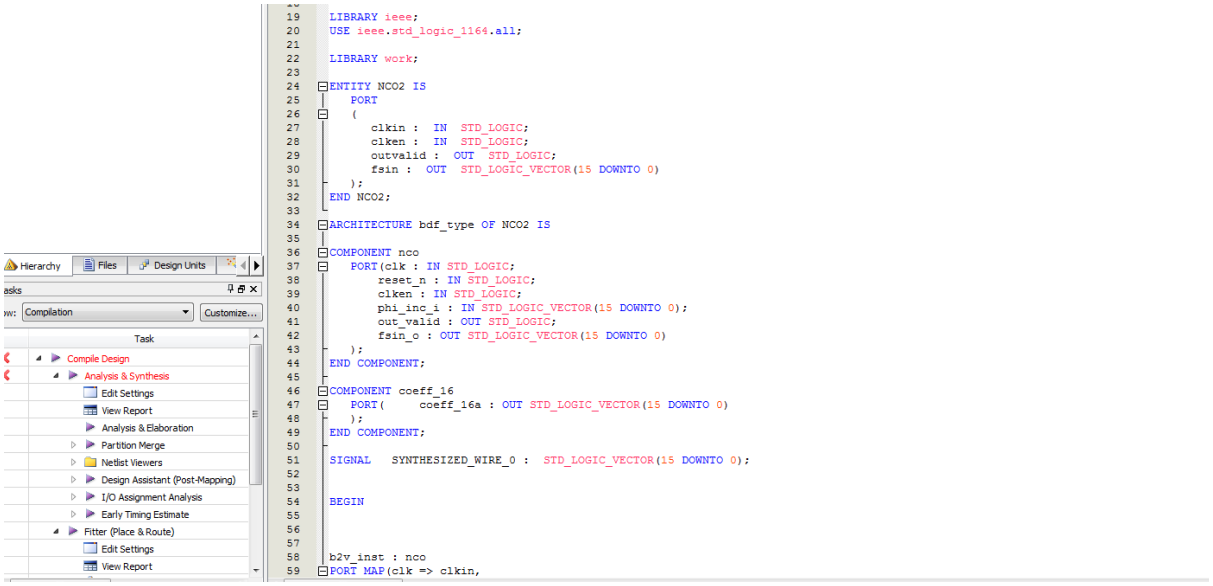
Vhdl code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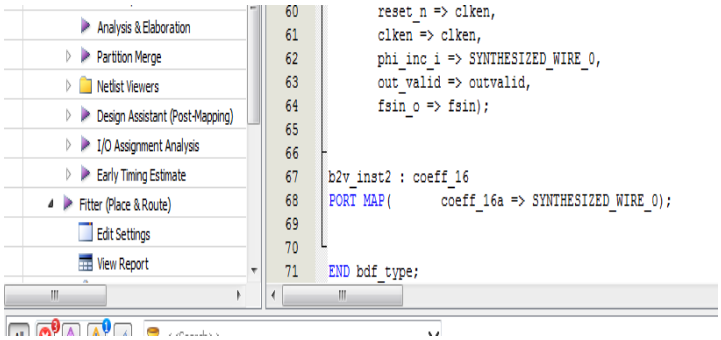
LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY work;
ENTITY NCO2 IS
PORT
(
clkin : IN STD_LOGIC;
clken : IN STD_LOGIC;
outvalid : OUT STD_LOGIC;
fsin : OUT STD_LOGIC_VECTOR(15 DOWNTO 0)
);
END NCO2;
ARCHITECTURE bdf_type OF NCO2 IS
COMPONENT nco
PORT(clk : IN STD_LOGIC;
reset_n : IN STD_LOGIC;
clken : IN STD_LOGIC;
phi_inc_i : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
out_valid : OUT STD_LOGIC;
fsin_o : OUT STD_LOGIC_VECTOR(15 DOWNTO 0)
);
END COMPONENT;
COMPONENT coeff_16
PORT(coeff_16a : OUT STD_LOGIC_VECTOR(15 DOWNTO 0)
);
END COMPONENT;
SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC_VECTOR(15 DOWNTO 0);
BEGIN
b2v_inst : nco
PORT MAP(clk => clkin,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reset_n => clken,
clken => clken,
phi_inc_i => SYNTHESIZED_WIRE_0,
out_valid => outvalid,
fsin_o => fsin);
b2v_inst2 : coeff_16
PORT MAP(coeff_16a => SYNTHESIZED_WIRE_0);
END bdf_type;