

File Summary

The legalizer interface is creating the following files in the output directory:

File	Description
root3_hnd	A MegaCore® function variation file, which defines a VHDL-level description of the custom MegaCore function. Reassemble the entity defined by this file inside of your design. Include this file when compiling your design in the Quartus ISE software.
root3_smp	A VHDL component declaration for the MegaCore function variation. Add the contents of this file to any VHDL architecture that reassembles the MegaCore function.
root3_hstf	Quartus® symbol file for the MegaCore function variation. You can use this file in the Quartus ISE block diagram editor.
root3_hstf	VHDL P functional simulation model.
root3_srv	Generated VHDL synthesizable model. This file is required for Quartus ISE synthesis. It will be added to your Quartus project.
root3_3a_hnd	VHDL Testbench.
root3_3a_hnd_synth	ModelSim-TL Script to run the VHDL P Functional Simulation model and generate VHDL Testbench in the ModelSim simulator software.
root3_variation	ModelSim Variation File.
root3_modelm	IACTLAB file describing a IACTLAB reference model.
root3_3a_m	IACTLAB Testbench.
root3_3a_hnd	Intel-FPGA-formal ROM initialization file.
root3_3a_hnd	Intel-FPGA-formal ROM initialization file.
root3_3a_hnd	Intel-FPGA-formal ROM initialization file.
root3_3a_hnd	Intel-FPGA-formal ROM initialization file.
root3_3a_hnd	Intel-FPGA-formal ROM initialization file.
root3_3a_hnd	Intel-FPGA-formal ROM initialization file.
root3_3a_hnd	Quartus ISE report file.
root3_3a_hnd	A JTAG description that can be used to assign hardware in simulation behavior settings to the Quartus project.
root3_syn_v	A timing and resource estimation model for use in some third-party synthesis tools.
root3_dsp	Contains Quartus project information for your MegaCore function variation.
root3_hndm	The MegaCore function report file.

MegaCore Function Variation File Ports

Name	Direction	Width
pll_in_1	INPUT	16
pll_o	OUTPUT	16
clk	INPUT	1
reset_n	INPUT	1
clocken	INPUT	1
out_jadd	OUTPUT	1
freq_out_1	INPUT	16

Generating MegaCore function top-level...

