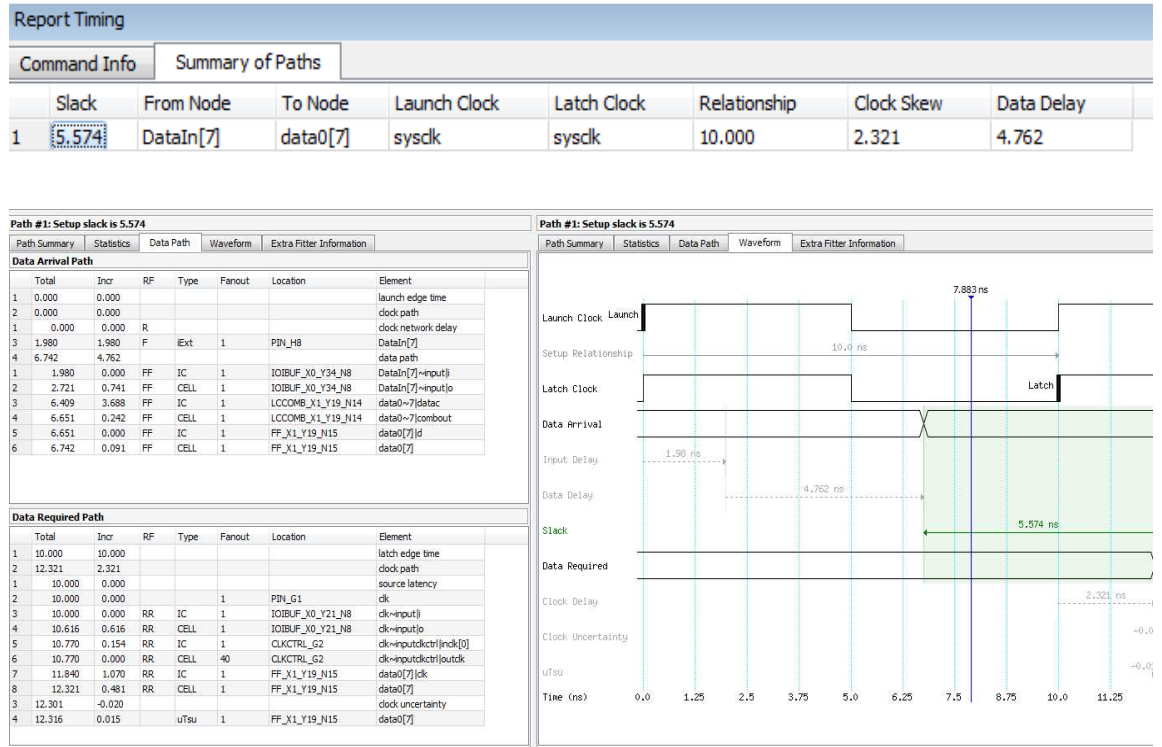1. Why are clock delay and data delay different even when selecting completely the same path for setup check and hold check ? See details below: (I'm using Test1 sample in Timequest folder)
    a. Setup check from DataIn[7] to data0[7]

Report Timing

		Command Info	Summary of Paths						
		Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1		5.574	DataIn[7]	data0[7]	sysclk	sysclk	10.000	2.321	4.762

Path #1: Setup slack is 5.574

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	0.000	0.000					clock path
1	0.000	0.000	R				clock network delay
3	1.980	1.980	F	iExt	1	PIN_H8	DataIn[7]
4	6.742	4.762					data path
1	1.980	0.000	FF	IC	1	IOIBUF_X0_Y34_N8	DataIn[7]~input|i
2	2.721	0.741	FF	CELL	1	IOIBUF_X0_Y34_N8	DataIn[7]~input|o
3	6.409	3.688	FF	IC	1	LCCOMB_X1_Y19_N14	data0~7|datac
4	6.651	0.242	FF	CELL	1	LCCOMB_X1_Y19_N14	data0~7|combout
5	6.651	0.000	FF	IC	1	FF_X1_Y19_N15	data0[7]|d
6	6.742	0.091	FF	CELL	1	FF_X1_Y19_N15	data0[7]

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.321	2.321					clock path
1	10.000	0.000					source latency
2	10.000	0.000			1	PIN_G1	clk
3	10.000	0.000	RR	IC	1	IOIBUF_X0_Y21_N8	clk~input|i
4	10.616	0.616	RR	CELL	1	IOIBUF_X0_Y21_N8	clk~input|o
5	10.770	0.154	RR	IC	1	CLKCTRL_G2	clk~inputclkctrl|inclk[0]
6	10.770	0.000	RR	CELL	40	CLKCTRL_G2	clk~inputclkctrl|outclk
7	11.840	1.070	RR	IC	1	FF_X1_Y19_N15	data0[7]|clk
8	12.321	0.481	RR	CELL	1	FF_X1_Y19_N15	data0[7]
3	12.301	-0.020					clock uncertainty
4	12.316	0.015		uTsu	1	FF_X1_Y19_N15	data0[7]

Path #1: Setup slack is 5.574

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

    b. Hold check from DataIn[7] to data0[7]

Report Timing

		Command Info	Summary of Paths						
		Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1		3.535	DataIn[7]	data0[7]	sysclk	sysclk	0.000	2.410	4.122

Path #1: Hold slack is 3.535

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	0.000	0.000					clock path
1	0.000	0.000	R				clock network delay
3	1.980	1.980	R	iExt	1	PIN_H8	DataIn[7]
4	6.102	4.122					data path
1	1.980	0.000	RR	IC	1	IOIBUF_X0_Y34_N8	DataIn[7]~input|i
2	2.556	0.576	RR	CELL	1	IOIBUF_X0_Y34_N8	DataIn[7]~input|o
3	5.812	3.256	RR	IC	1	LCCOMB_X1_Y19_N14	data0~7|datac
4	6.043	0.231	RR	CELL	1	LCCOMB_X1_Y19_N14	data0~7|combout
5	6.043	0.000	RR	IC	1	FF_X1_Y19_N15	data0[7]|d
6	6.102	0.059	RR	CELL	1	FF_X1_Y19_N15	data0[7]

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	2.410	2.410					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_G1	clk
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y21_N8	clk~input|i
4	0.616	0.616	RR	CELL	1	IOIBUF_X0_Y21_N8	clk~input|o
5	0.776	0.160	RR	IC	1	CLKCTRL_G2	clk~inputclkctrl|inclk[0]
6	0.776	0.000	RR	CELL	40	CLKCTRL_G2	clk~inputclkctrl|outclk
7	1.891	1.115	RR	IC	1	FF_X1_Y19_N15	data0[7]|clk
8	2.410	0.519	RR	CELL	1	FF_X1_Y19_N15	data0[7]
3	2.410	0.000					clock uncertainty
4	2.567	0.157		uTh	1	FF_X1_Y19_N15	data0[7]

Path #1: Hold slack is 3.535

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information