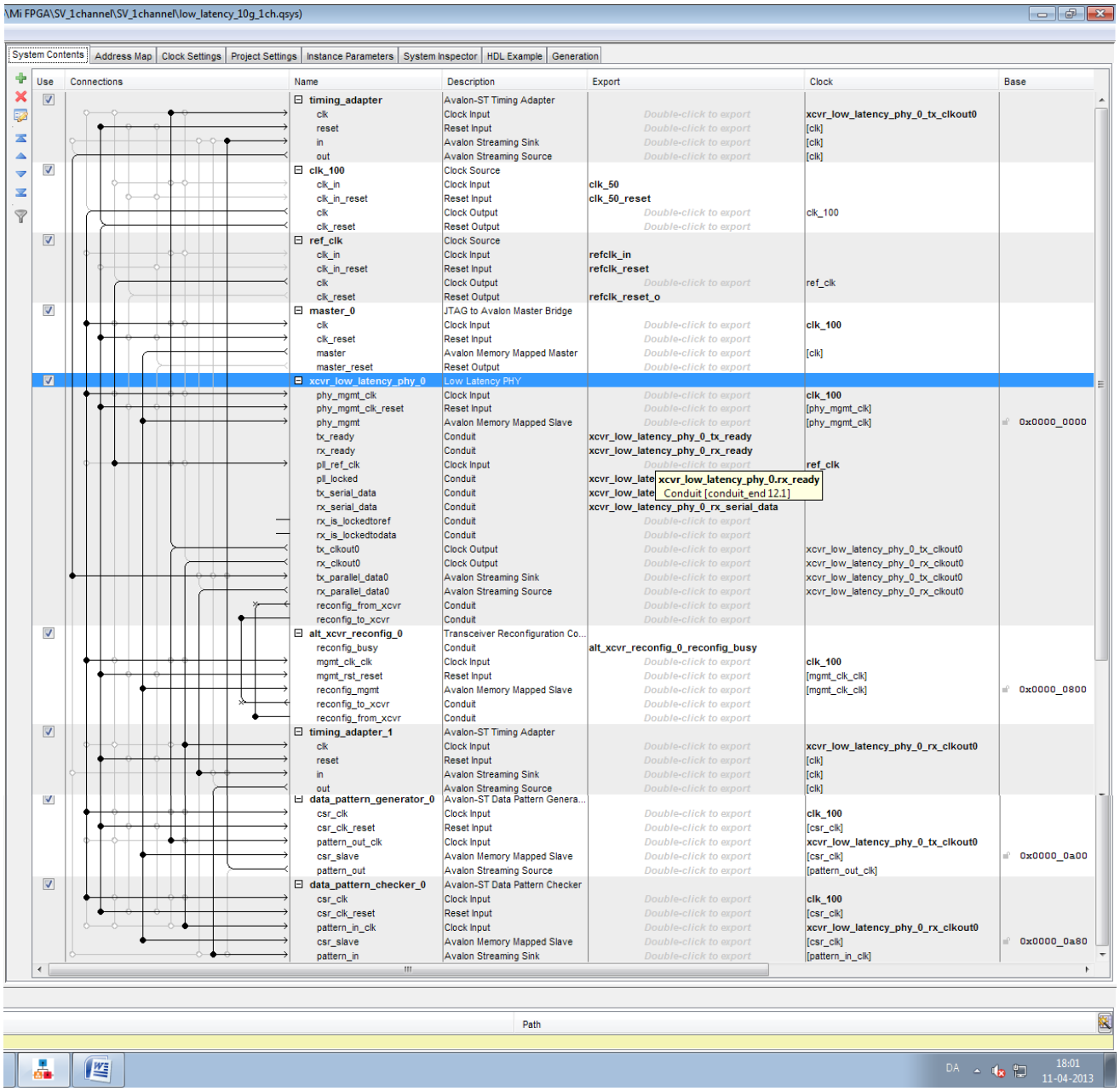
\Mi FPGA\SV_1channel\SV_1channel\low_latency_10g_1ch.qsys)
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
timing_adapter
Avalon-ST Timing Adapter
clk
Clock Input
Double-click to export
xcvr_low_latency_phy_0_tx_clkout0
reset
Reset Input
Double-click to export
[clk]
in
Avalon Streaming Sink
Double-click to export
[clk]
out
Avalon Streaming Source
Double-click to export
[clk]
clk_100
Clock Source
clk_in
Clock Input
clk_50
clk_in_reset
Reset Input
clk_50_reset
clk
Clock Output
Double-click to export
clk_100
clk_reset
Reset Output
Double-click to export
ref_clk
Clock Source
clk_in
Clock Input
refclk_in
clk_in_reset
Reset Input
refclk_reset
clk
Clock Output
Double-click to export
ref_clk
clk_reset
Reset Output
refclk_reset_o
master_0
JTAG to Avalon Master Bridge
clk
Clock Input
Double-click to export
clk_100
clk_reset
Reset Input
Double-click to export
master
Avalon Memory Mapped Master
Double-click to export
[clk]
master_reset
Reset Output
Double-click to export
xcvr_low_latency_phy_0
Low Latency PHY
phy_mgmt_clk
Clock Input
Double-click to export
clk_100
phy_mgmt_clk_reset
Reset Input
Double-click to export
[phy_mgmt_clk]
phy_mgmt
Avalon Memory Mapped Slave
Double-click to export
[phy_mgmt_clk]
0x0000_0000
tx_ready
Conduit
xcvr_low_latency_phy_0_tx_ready
rx_ready
Conduit
xcvr_low_latency_phy_0_rx_ready
pll_ref_clk
Clock Input
Double-click to export
ref_clk
pll_locked
Conduit
xcvr_low_late
xcvr_low_latency_phy_0.rx_ready
Conduit [conduit_end 12.1]
tx_serial_data
Conduit
xcvr_low_late
rx_serial_data
Conduit
xcvr_low_latency_phy_0_rx_serial_data
rx_is_lockedtoref
Conduit
Double-click to export
rx_is_lockedtodata
Conduit
Double-click to export
tx_clkout0
Clock Output
Double-click to export
xcvr_low_latency_phy_0_tx_clkout0
rx_clkout0
Clock Output
Double-click to export
xcvr_low_latency_phy_0_rx_clkout0
tx_parallel_data0
Avalon Streaming Sink
Double-click to export
xcvr_low_latency_phy_0_tx_clkout0
rx_parallel_data0
Avalon Streaming Source
Double-click to export
xcvr_low_latency_phy_0_rx_clkout0
reconfig_from_xcvr
Conduit
Double-click to export
reconfig_to_xcvr
Conduit
Double-click to export
alt_xcvr_reconfig_0
Transceiver Reconfiguration Co...
reconfig_busy
Conduit
alt_xcvr_reconfig_0_reconfig_busy
mgmt_clk_clk
Clock Input
Double-click to export
clk_100
mgmt_rst_reset
Reset Input
Double-click to export
[mgmt_clk_clk]
reconfig_mgmt
Avalon Memory Mapped Slave
Double-click to export
[mgmt_clk_clk]
0x0000_0800
reconfig_to_xcvr
Conduit
Double-click to export
reconfig_from_xcvr
Conduit
Double-click to export
timing_adapter_1
Avalon-ST Timing Adapter
clk
Clock Input
Double-click to export
xcvr_low_latency_phy_0_rx_clkout0
reset
Reset Input
Double-click to export
[clk]
in
Avalon Streaming Sink
Double-click to export
[clk]
out
Avalon Streaming Source
Double-click to export
[clk]
data_pattern_generator_0
Avalon-ST Data Pattern Genera...
csr_clk
Clock Input
Double-click to export
clk_100
csr_clk_reset
Reset Input
Double-click to export
[csr_clk]
pattern_out_clk
Clock Input
Double-click to export
xcvr_low_latency_phy_0_tx_clkout0
csr_slave
Avalon Memory Mapped Slave
Double-click to export
[csr_clk]
0x0000_0a00
pattern_out
Avalon Streaming Source
Double-click to export
[pattern_out_clk]
data_pattern_checker_0
Avalon-ST Data Pattern Checker
csr_clk
Clock Input
Double-click to export
clk_100
csr_clk_reset
Reset Input
Double-click to export
[csr_clk]
pattern_in_clk
Clock Input
Double-click to export
xcvr_low_latency_phy_0_rx_clkout0
csr_slave
Avalon Memory Mapped Slave
Double-click to export
[csr_clk]
0x0000_0a80
pattern_in
Avalon Streaming Sink
Double-click to export
[pattern_in_clk]
Path
DA
18:01
11-04-2013