```
LIBRARY IEEE;
USE IEEE.std logic 1164.ALL;
USE IEEE.numeric std.ALL;
ENTITY transfer fixpt IS
                                 : IN real; -- double
: IN real; -- double
: OUT real; -- double
 PORT ( num 1
      deno 1
      h re
      h im
                                 : OUT real -- double
      );
END transfer fixpt;
ARCHITECTURE rtl OF transfer fixpt IS
BEGIN
 --HDL code generation from MATLAB function: transfer fixpt
응
           Generated by MATLAB 9.2 and Fixed-Point Designer 5.4
응
h re <= 0.00096287158489771828;
 h im <= 0.00019286361239814089;
END rtl;
```