

1. In QSYS I selected NIOS II (CLASSIC ) processor ,UART,ON CHIP MEMORY,EPCQ CONTROLLER.
2. Base address are following

[-] epcq_controller_0	Altera Serial Flash Controller							
→ clock_sink	Clock Input	Double-click to export	clk_0					
→ reset	Reset Input	Double-click to export	[clock_sink]					
→ avl_csr	Avalon Memory Mapped Slave	Double-click to export	[clock_sink]	# 0x0100_5020	0x0100_503f			
→ avl_mem	Avalon Memory Mapped Slave	Double-click to export	[clock_sink]	# 0x0000_0000	0x00ff_ffff			
< interrupt_sender	Interrupt Sender	Double-click to export	[clock_sink]					
[-] onchip_memory2_0	On-Chip Memory (RAM or ROM)							
→ clk1	Clock Input	Double-click to export	clk_0					
→ s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	# 0x0100_2000	0x0100_3fff			
→ reset1	Reset Input	Double-click to export	[clk1]					
[-] nios2_qsys_0	Nios II (Classic) Processor							
clk	Clock Input	Double-click to export	clk_0					
reset_n	Reset Input	Double-click to export	[clk]					
data_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
d_irq	Interrupt Receiver	Double-click to export	[clk]				IRQ 0	IRQ 31
jtag_debug_module_r...	Reset Output	Double-click to export	[clk]					
jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x0100_4800	0x0100_4fff			
custom_instruction_m...	Custom Instruction Master	Double-click to export	[clk]					

Qsys - flash1.qsys (D:\hsr\_prp\flash1\flash1.qsys)

File Edit System Generate View Tools Help

System Contents Address Map Interconnect Requirements

System: flash1 Path: clk\_0

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opcode Name
		clk_in	Clock Input	clk	exported					
		clk_in_reset	Reset Input	reset						
		clk	Clock Output	Double-click to export	clk_0					
		clk_reset	Reset Output	Double-click to export						
		[-] epcq_controller_0	Altera Serial Flash Controller							
		clock_sink	Clock Input	Double-click to export	clk_0					
		reset	Reset Input	Double-click to export	[clock_sink]					
		avl_csr	Avalon Memory Mapped Slave	Double-click to export	[clock_sink]	# 0x0100_5020	0x0100_503f			
		avl_mem	Avalon Memory Mapped Slave	Double-click to export	[clock_sink]	# 0x0000_0000	0x00ff_ffff			
		interrupt_sender	Interrupt Sender	Double-click to export	[clock_sink]					
		[-] onchip_memory2_0	On-Chip Memory (RAM or ROM)							
		clk1	Clock Input	Double-click to export	clk_0					
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	# 0x0100_2000	0x0100_3fff			
		reset1	Reset Input	Double-click to export	[clk1]					
		[-] uart_0	UART (RS-232 Serial Port)							
		clk	Clock Input	Double-click to export	clk_0					
		reset	Reset Input	Double-click to export	[clk]					
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x0100_5040	0x0100_505f			
		external_connection	Conduit							
		irq	Interrupt Sender	Double-click to export	[clk]					
		[-] nios2_qsys_0	Nios II (Classic) Processor							
		clk	Clock Input	Double-click to export	clk_0					
		reset_n	Reset Input	Double-click to export	[clk]					
		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
		d_irq	Interrupt Receiver	Double-click to export	[clk]			IRQ 0		
		jtag_debug_module_r...	Reset Output	Double-click to export	[clk]					
		jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x0100_4800	0x0100_4fff			
		custom_instruction_m...	Custom Instruction Master	Double-click to export	[clk]					

Current filter:

0 Errors, 1 Warning

nios2\_qsys\_0.custom\_instruction\_master  
Custom Instruction Master [nios\_custom\_instruction\_master17.0]  
Associated clock: None (asynchronous)

Generate HDL... Finish

12:31 PM  
12/29/2017

Step2: IN reset vector memory I selected EPCQ CONTROLLER , in exception vector memory ,I selected onchipmemory and reset vector and exception vector address taking automatically by default .

**Reset Vector**

Reset vector memory:

Reset vector offset:

Reset vector:

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**Exception Vector**

Exception vector memory:

Exception vector offset:

Exception vector:

System: flash1 Path: nios2\_qsys\_0

**Nios II (Classic) Processor**

altera\_nios2\_qsys

Nios II Core:

- Nios II/e
- Nios II/s
- Nios II/f

	Nios II/e	Nios II/s	Nios II/f
<b>Nios II</b> Selector Guide	RISC 32-bit	RISC 32-bit Instruction Cache Branch Prediction Hardware Multiply Hardware Divide	RISC 32-bit Instruction Cache Branch Prediction Hardware Multiply Hardware Divide Barrel Shifter Data Cache Dynamic Branch Prediction
Memory Usage (e.g Stratix IV)	Two M9Ks (or equiv.)	Two M9Ks + cache	Three M9Ks + cache

**Hardware Arithmetic Operation**

Hardware multiplication type:

Hardware divide

**Reset Vector**

Reset vector memory:

Reset vector offset:

Reset vector:

**Exception Vector**

Exception vector memory:

Exception vector offset:

Exception vector:

0 Errors, 1 Warning

Generate HDL... Finish

IN QUARTUX2 compiled successfully ,when I creating BSP in eclipse nios2 than following error coming.

**Error coming while I am creating bsp for project.**

Entry section mapping not created because reset memory location not located at base address 0x1011040.

Error :altera hal linker generator :the section mapping entry is missing.

Error :altera hal linker generator :Required linker section mapping do not exist:[entry].



