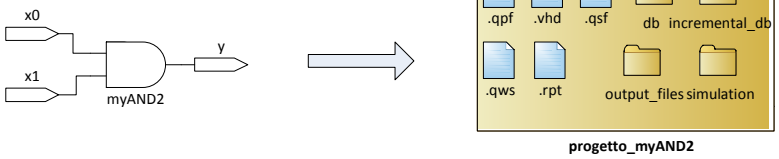
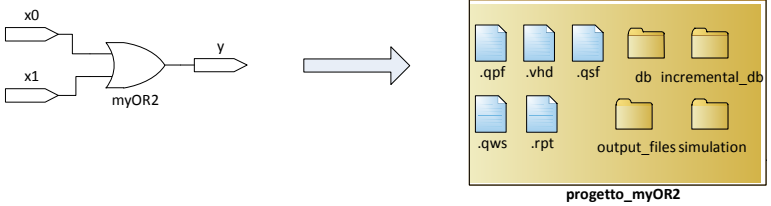
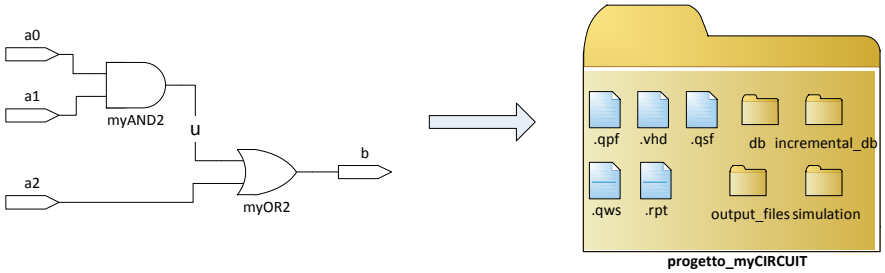


progetto_myAND2



progetto_myOR2



progetto_myCIRCUIT

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all  ;

ENTITY myCIRCUIT  IS
   PORT(
      a: in std_logic_vector(2 downto 0);
      b: out std_logic
      );
END myCIRCUIT;

ARCHITECTURE struct OF myCIRCUIT IS
   SIGNAL u   :  STD_LOGIC ;

   COMPONENT myAND2
      GENERIC (
       delay  : DELAY_LENGTH := 0 ns);
      PORT (
       y  : out STD_LOGIC ;
       x1  : in STD_LOGIC ;
       x2  : in STD_LOGIC );
   END COMPONENT myAND2;

   COMPONENT myOR2
      GENERIC (
      delay  : DELAY_LENGTH := 0 ns);
      PORT (
      y  : out STD_LOGIC ;
      x1  : in STD_LOGIC ;
      x2  : in STD_LOGIC );
   END COMPONENT myOR2;

BEGIN
   g1: component myAND2 port map (x1=>a(0), x2=>a(1), y=>u);
   g2: component myOR2 port map (x1=>u, x2=>a(2), y=>b);

END  ARCHITECTURE struct;
```

compile & elaboration

Error (12006): Node instance "g1" instantiates undefined entity "myAND2". Ensure that required library paths are specified correctly, define the specified entity, or change the instantiation. If this entity represents Intel FPGA or third-party IP, generate the synthesis files for the IP.

Error (12006): Node instance "g2" instantiates undefined entity "myOR2". Ensure that required library paths are specified correctly, define the specified entity, or change the instantiation. If this entity represents Intel FPGA or third-party IP, generate the synthesis files for the IP.

Error: Quartus Prime Analysis & Elaboration was unsuccessful. 2 errors, 1 warning

How to do , in QUARTUS PRIME (LITE edition), in order to reference the components describes in architecture and execute a proper simulation?